Overview and latest updates of PSP and L-UTSOI standard model

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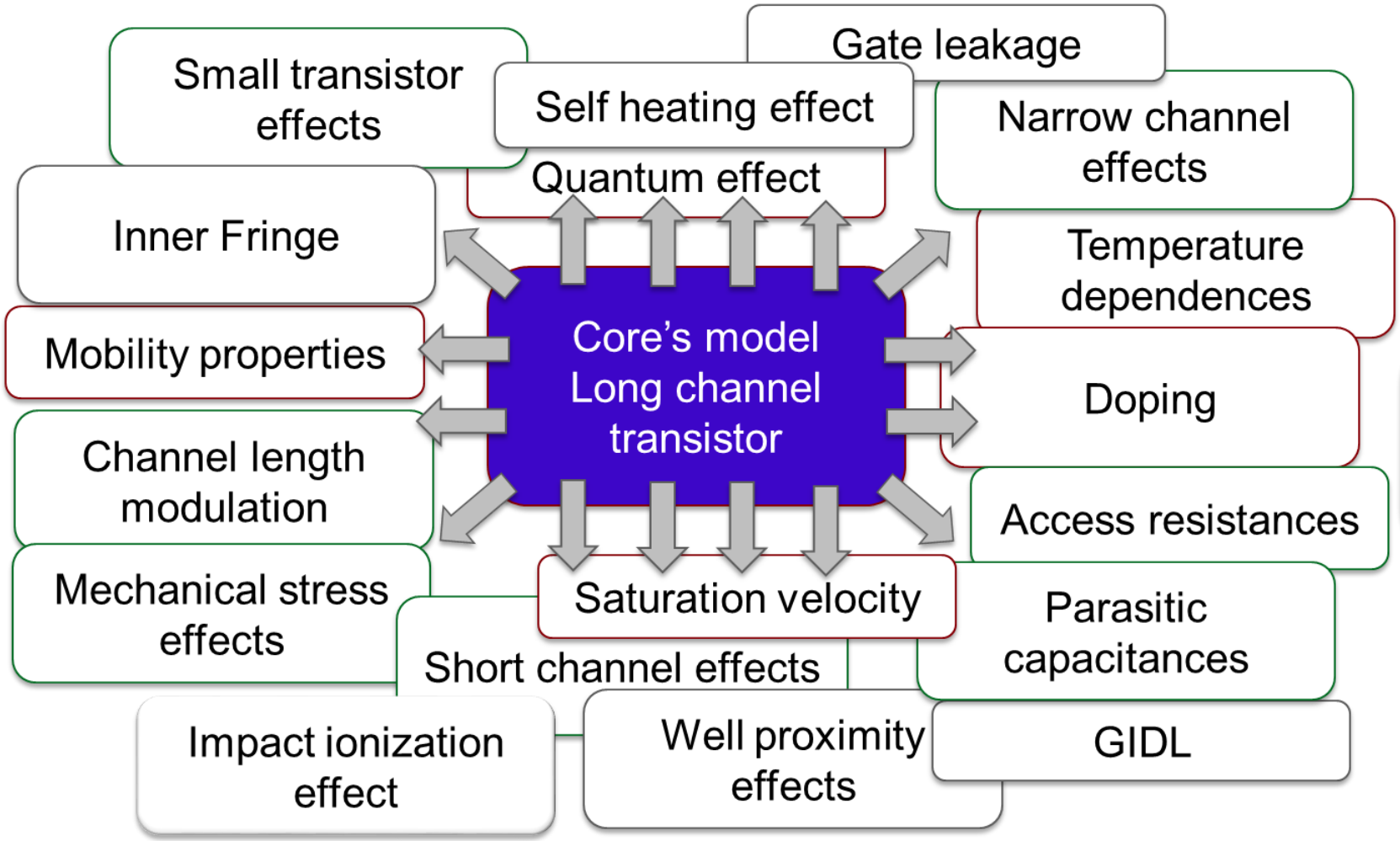
W5: MOS-AK: Compact Modeling Support for OpenPDK and FOSS IC Designs

Outline

- **Introduction**
- PSP 104.0 new non backward compatible model
  - Summary of PSP version
  - PSP104 - Revise OP-output
  - PSP104 - Vdsat for long channel
  - PSP104 - Improved symmetry for low AX value
  - PSP104 - Improved Q-model in short channels
- L-UTSOI recent feature:
  - Summary of L-UTSOI version
  - L-UTSOI Computational Cryo issue & solution
  - Introduction of band edge defects
  - Cryo.: some illustrations
  - Leakages induced by edge transistors
  - Q-model decoupling
- Conclusion

Compact model real life



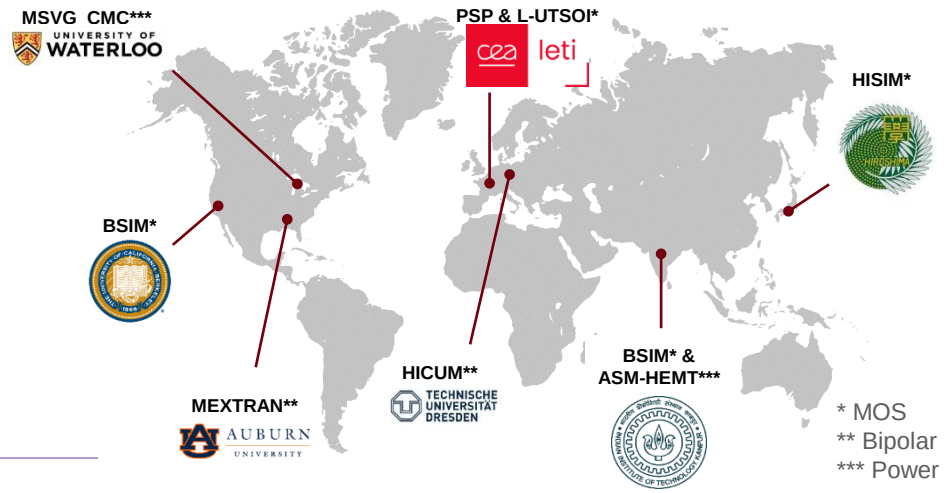
Following industrial expectation, compact model is continually improves.

[1] O. Rozeau et al "Surface potential based MOSFET model for iC simulation".

From equation to "standard model": CMC

- **Why do we need device's model (MOSFET, Bipolar …)?**

- **What does "*standard model*" means?**
  - ☑ Continual Improvement
  - ☑ Quality Assurance
  - ☑ EDA tools Availability
- **Why do we need CMC (Compact Model Coalition)?**
  - ☑ Standarization process management
  - ☑ Worlwide collaborative working groups
  - ☑ IC Manufacturers / EDA editors / Model developers
- **Who are the developers around the world (transistor)?**



Transistor Model: * MOSFET-like model; ** Bipolar; *** Power model Other model is dvp. By CMC (diode, ESD …)

Si Compact Model Coalition

CMC ensure proven model simulation aligned with industrial expectation (through Quality Assurance test and Verilog-A checker VAMPyRE).

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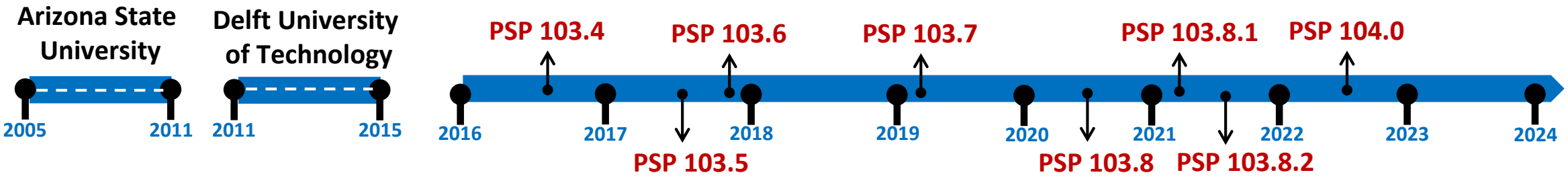
PSP model

- PSP is a surface potential based model for deep-submicron bulk MOSFET. JUNCAP is a diode models part of PSP package.
- In December 2005, PSP has been elected a new industrial standard model by the CMC. This initial version was based on MM11 (from NXP Semiconductors) and SP (from Pennsylvania State University and later at Arizona State University).
- PSP meets numerical requirements for Digital, Analog-Mixed Signal, and RF circuit designs, in particular continuous derivation of currents and charges is insured.
- Since 2015 CEA-LETI is in charge of model update.



Summary of PSP version

Date	Release PSP	Major improvements/features
08/2016	103.4	- Update JUNCAP 200.5 - Add SWEDGE for edge transistor. - Add SWIGN for induced gate noise. - Add short channel effect (PSCE …).
08/2017	103.5	- Introduction of exponent dependence of CS (THECS).
12/2017	103.6	- Introduction of non-uniform DIT.
02/2019	103.7	- Introduction of new parameter for gate leakage current. - Add SWQPART for charge partitioning between source and drain.
07/2020	103.8	- Introduction of inner fringe charge model. - Introduction of extra overlap charge model.
04/2021	103.8.1	- Update JUNCAP 200.6 - TRISE, DTEMP and TREF.
06/2022	103.8.2	- Add SWFIX for fix non physical behavior.
09/2023	104.0	- 5th model version including JUNCAP 200.6. - New DIBL model based on quasi-fermi level correction including screening effect in inversion. - Add new parameter to improve gm description in saturation: THESATT. - Capacitance reciprocity improvement using CTG/CTB parameters. - New calculation of the drain saturation voltage for long channel transistor. - Improvement of S/D symmetry with introduction of new linear-saturation transition. - Remove effective doping bias-dependence effect: VSUB, NSLP, DNSUB. - New binning equation with "hybrid" approach. - Revised DC operating output.

Presentation today focus on the last release

PSP104 - Revise OP-output

- Motivations:
  - Reduce the number of .OP variables (256 in PSP103 -> 101 in PSP104)
  - Updated list of .OP variables provided by the WG members (STM, NXP)
  - Configurable OP information with switches:
    - Convention (SWOPPMOS flag):
      - PMOS → All voltages and currents have signs related to the circuit simulation (e.g. pmos Vth is negative)
      - NMOS → All voltages and currents are represented as for nmos (cf. PSP103)
    - S/D interchange (SWOPDRAIN flag):
      - The drain is considered to be the electrical drain (e.g. Vds is always positive for nmos)
      - The drain is considered to be the first terminal of the model in a netlist
    - Effects of access resistances (SWOPREXT flag):
      - OP variables include the impact of Rd/Rg/Rs
      - OP variables don't include the impact of Rd/Rg/Rs

PSP104 - Vdsat for long channel 1/2

Saturation drain voltage in PSP103

Considering the equation of the channel current without saturation velocity effect :

$$I_d = -\frac{W}{L_{eff}} \cdot C'_{ox} \cdot \mu_{eff} \cdot \left((q_{i,s} + \alpha \cdot \phi_T) \cdot \psi_{ds} - \frac{\alpha}{2} \cdot {\psi_{ds}}^2 \right)$$

and using the condition: $\left.\frac{\partial I_d}{\partial x_{ds}}\right|_{\psi_{ds}=\psi_{inf}} = 0$

$$\psi_{inf} = \frac{q_{i,s}}{\alpha} + \Phi_T$$

Saturation drain voltage in PSP104

Another condition, valid in all regimes, is considering the Poisson's equation and the boundary conditions:

Simp. SP @ Source:
$$(V_g - \psi_d)^2 = {G_f}^2 \cdot \left(\psi_d - \Phi_T - \Phi_T \cdot \exp\left(\frac{\psi_d - V_{db}}{\Phi_T} \right) \right)$$

Negligible in saturation

Simp. SP @ Drain:
$$(V_g - \psi_s)^2 = {G_f}^2 \cdot \left(\psi_s - \Phi_T - \Phi_T \cdot \exp\left(\frac{\psi_s - V_{sb}}{\Phi_T} \right) \right)$$

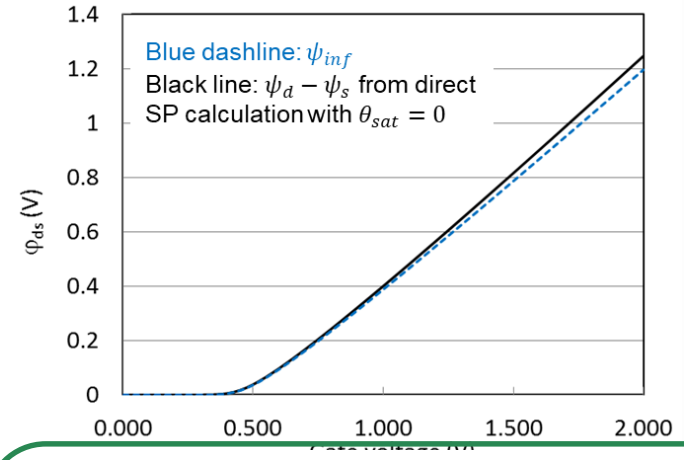
$$\psi_{inf} = \Phi_T \cdot a_{sat} \cdot \left(1 - \sqrt{1 - \frac{{G_f}^2 \cdot \exp\left(\frac{\psi_s - V_{sb}}{\Phi_T} \right)}{{a_{sat}}^2}} \right)$$

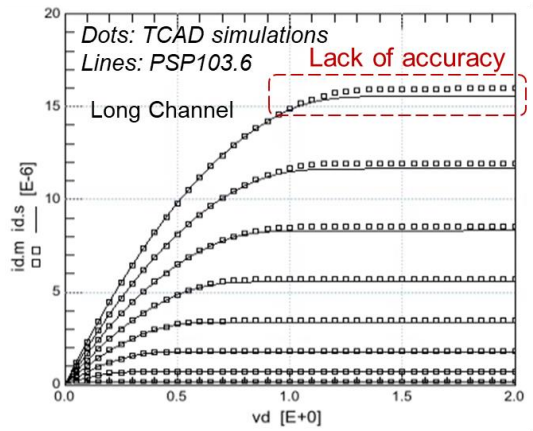
PSP104 - Vdsat for long channel 2/2

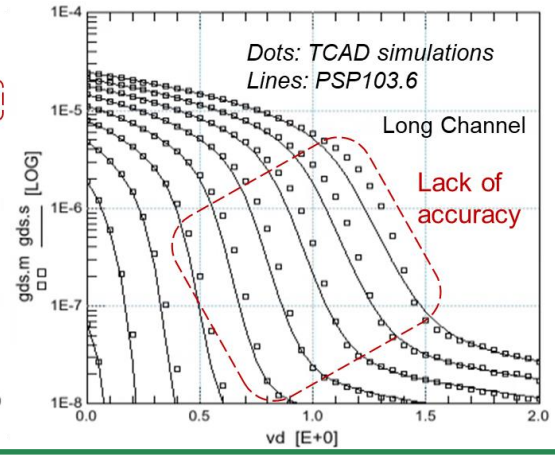
- Improve the accuracy of drain current in saturation for long channel MOSFET.

PSP 103:
VDSAT for long channel used derivative condition

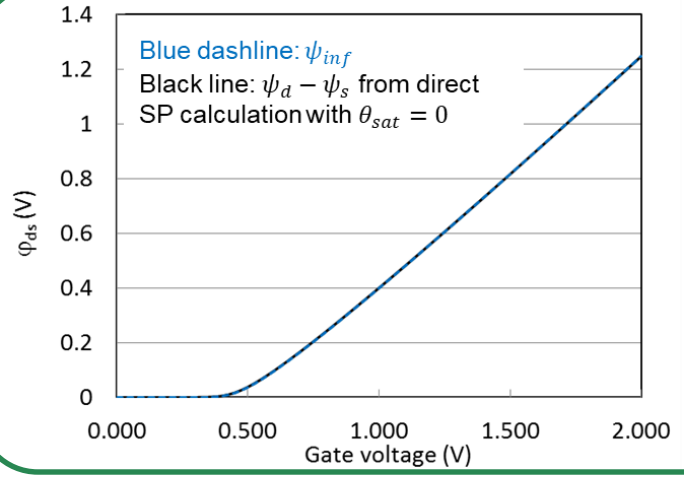
$$\left.\frac{\partial I_d}{\partial x_{ds}}\right|_{\psi_{ds}=\psi_{inf}} = 0$$

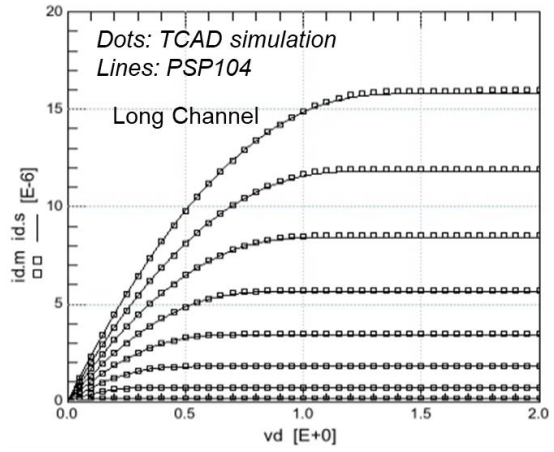


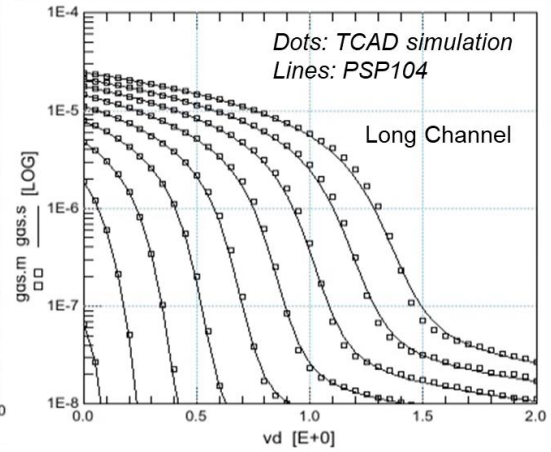




PSP 104:
Solved by the use of a new calculation sequence of Vdsat







PSP104 - Improved symmetry for low AX value

- PSP 103 limitation: V_{dse} function is not C∞ in regards to Gummel test for low AX-value
- PSP104: use a new mathematical function with C∞ function (from K. Xia *et al.* TED 2020)

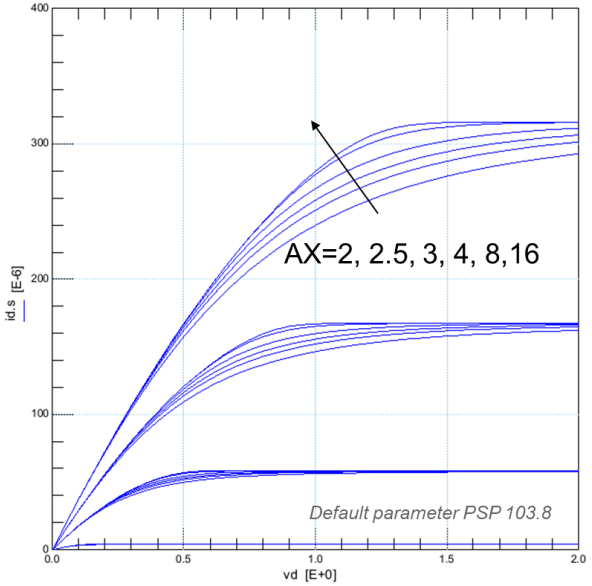
PSP 103

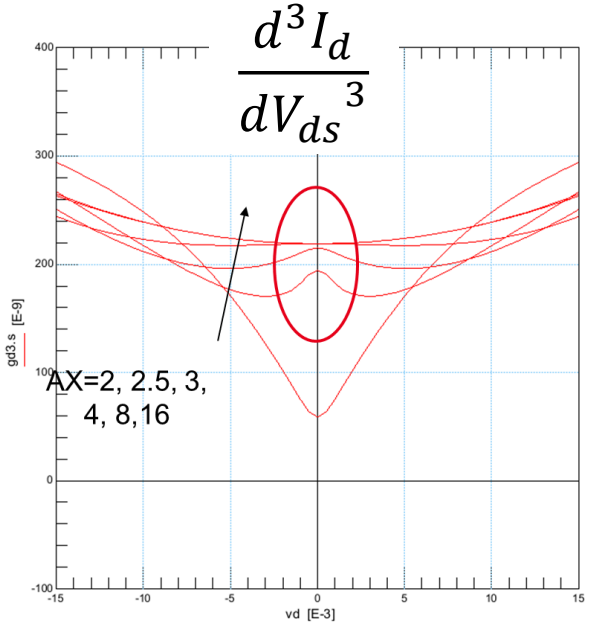
$$V_{dse} = \frac{V_{ds}}{\left(1 + \left(\frac{V_{ds}}{V_{dssat}}\right)^{AX}\right)^{\frac{1}{AX}}}$$

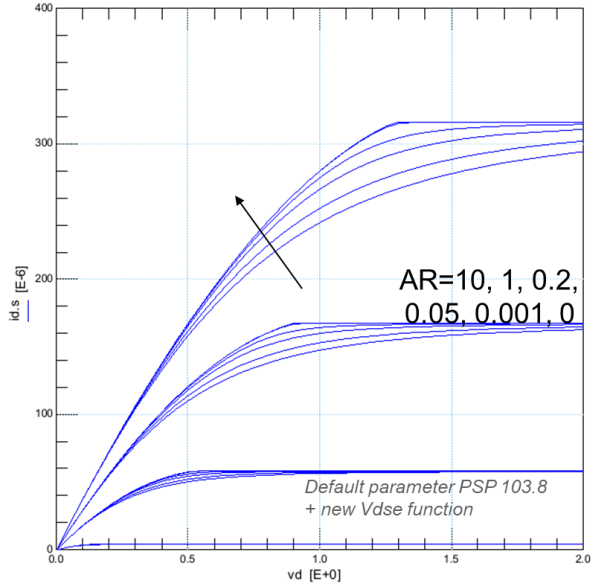
→ PSP 104

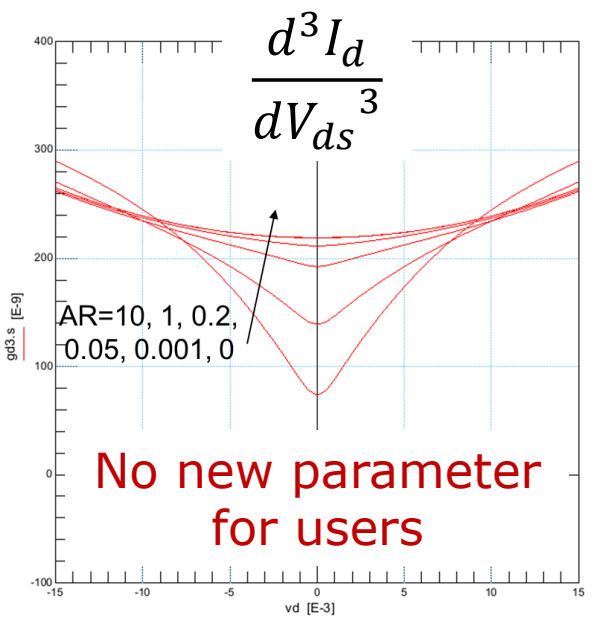
$$V_{dse} = \frac{2.\sqrt{1+AR}.V_{ds}}{\sqrt{\left(\frac{\sqrt{1+AR}.V_{ds}}{V_{dssat}} - 1\right)^2 + AR} + \sqrt{\left(\frac{\sqrt{1+AR}.V_{ds}}{V_{dssat}} + 1\right)^2 + AR}}$$

w. $$AR = \frac{\left((2)^{-\frac{2}{AX}} - 1\right)^2}{2.(2)^{-\frac{2}{AX}} - 1}$$





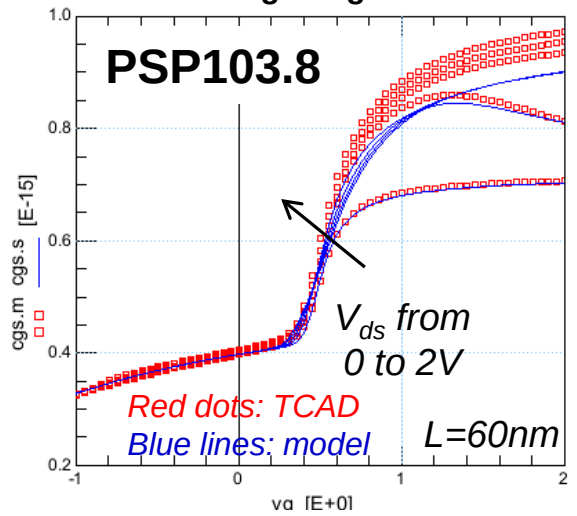


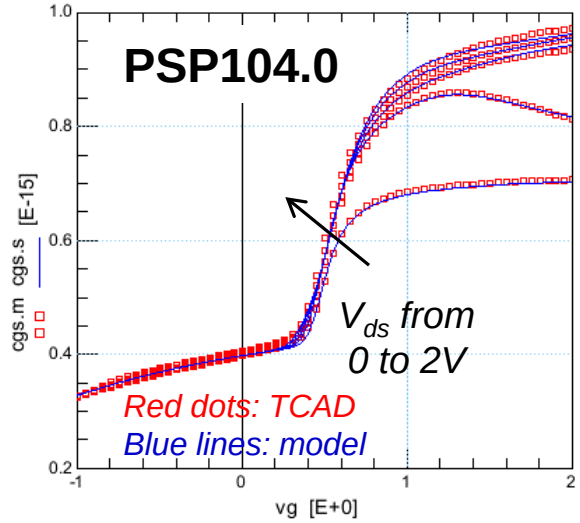


PSP104 - Improved Q-model in short channels

- Motivation: PSP 103.0 Q-model's limitation in short channel
  - Artefact on CV in accumulation induced by DIBL model: requires to set CFAC=0
  - Underestimation of V_{DSAT} for CV: requires THESATAC<THESAT
  - The lin-sat transition on CV is smoother compared to the one of IV: requires AXAC<AX
  - Partial depletion of overlaps: Cgd is overestimated in saturation. Requires a "negative" CLM
- For PSP104.0.0 release:
  - Revisited DIBL model
  - Addition of flexibility on CLM parameters (ALP can be negative) for Q-model
  - <u>No new parameters for users</u>

$C_{gs}(V_{gs})$





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  - **Cryo.: some illustrations**
  - **Leakages induced by edge transistors**
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L-UTSOI model

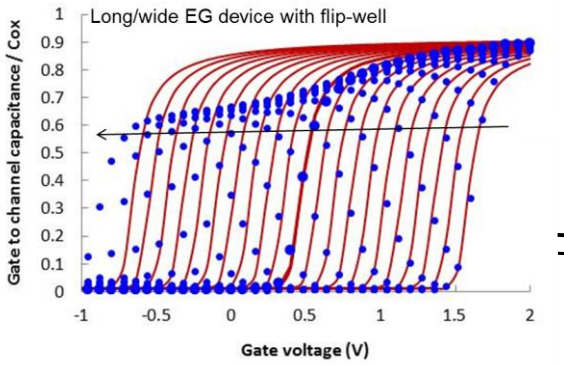
- L-UTSOI is a surface potential based model dedicated to FDSOI technology.

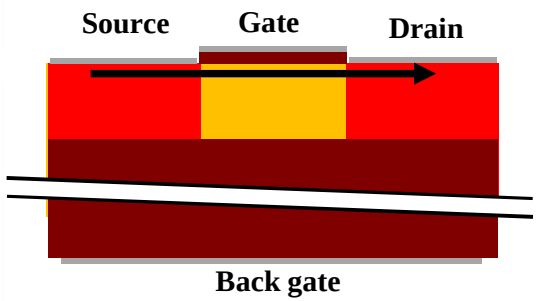
Leti-UTSOI 1.x.x
Back interface assumed depleted/weakly inverted

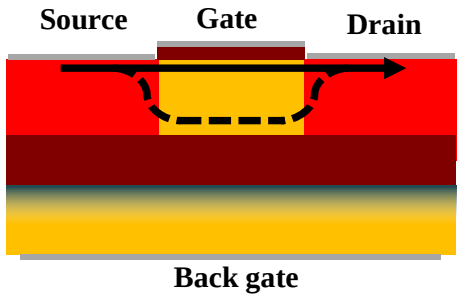
Leti-UTSOI 2.x.x
No assumption on back interface regime

L-UTSOI
New model name within CMC

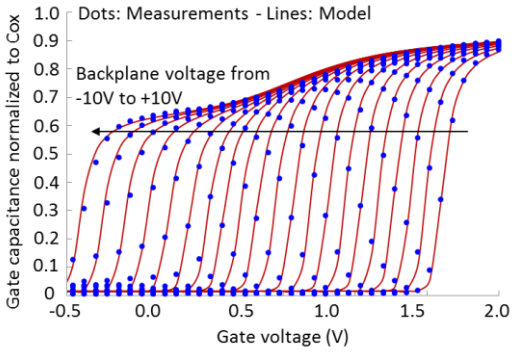
Wo. back interface

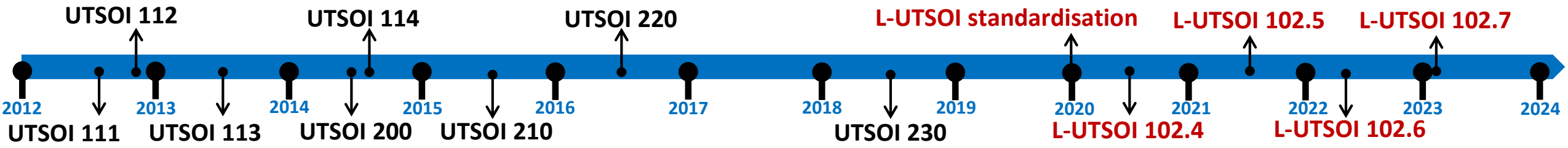






W. back interface





Summary of L-UTSOI version

Date	Release L-UTSOI	Major improvements/features
01/2020	102.4	- Introduction of impact ionization model (Samsung request). - Introduction of extra gate to overlap current (STm request).
01/2021	102.5	- Introduction of Gate Poly-Depletion model (Qualcomm request). - Enhancement of substrate depletion (STm request).
03/2022	102.6	- Introduction of RTA NOS model (Samsung request).
02/2023	102.7	- Introduction of cryogenic model (All request).
06/2024	102.8	- Introduction of edge transistor (Samsung request). - Charge decoupling for RF application (Samsung request).

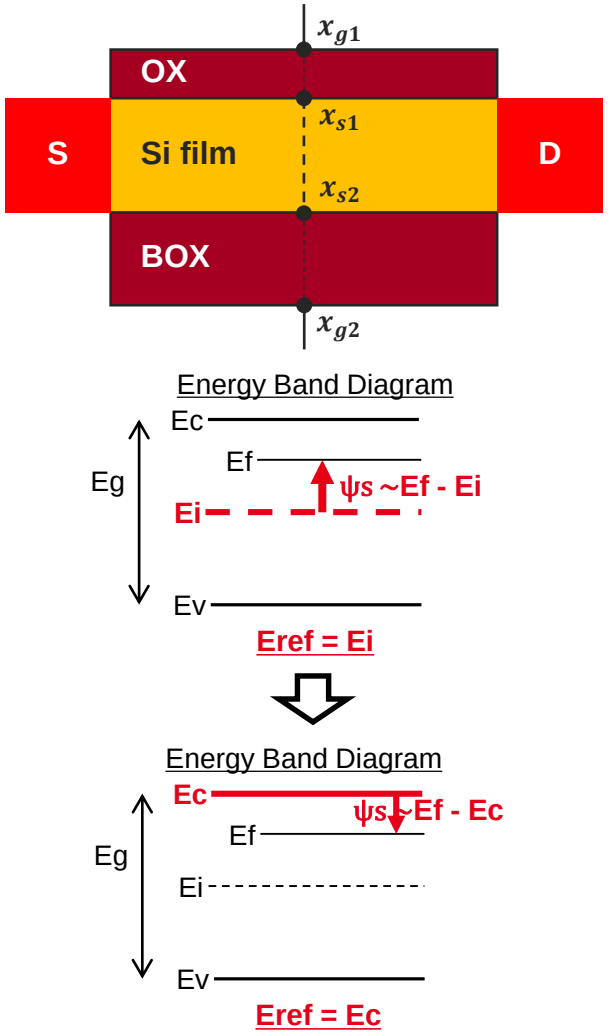
Presentation today focus on the last release

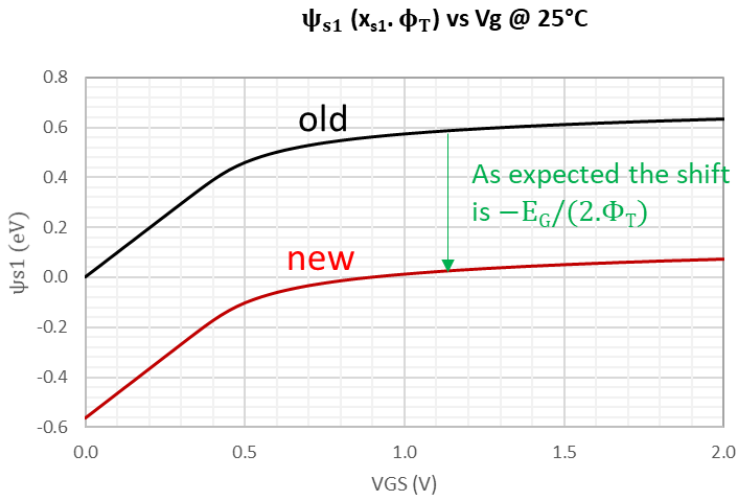
L-UTSOI Computational Cryo & solution 1/2

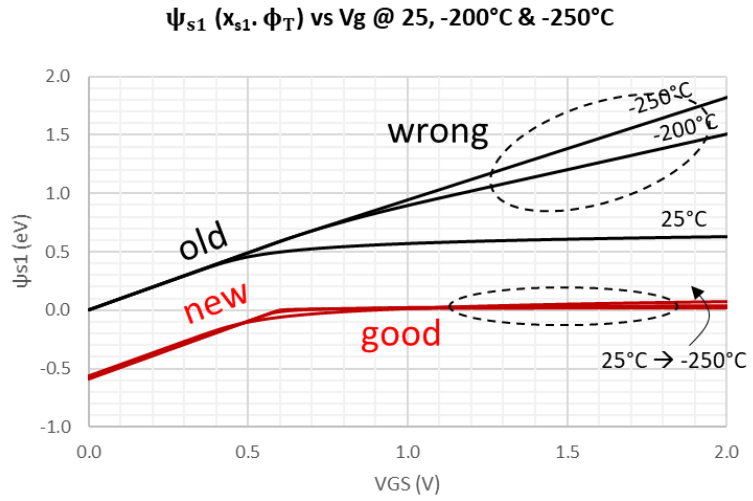
- L-UTSOI SPE:

$$\begin{cases} q^2 = k_1^2\left(x_{g1} - x_{s1}\right)^2 - A_0 e^{x_{s1}} e^{-x_n} \\ q^2 = k_2^2\left(x_{g2} - x_{s2}\right)^2 - A_0 e^{x_{s2}} e^{-x_n} \\ \frac{q}{2} + \coth^{-1}\left(\frac{k_1(x_{g1}-x_{s1})}{q}\right) - \coth^{-1}\left(\frac{k_2(x_{g2}-x_{s2})}{q}\right) = 0 \end{cases}$$

	L-UTSOI 102.6	L-UTSOI 102.7
Energy Reference	E_i	E_c
$A_0 \propto n_0$	$\sqrt{N_C N_V}\, e^{-\frac{E_g}{2k_B T}}$	$\propto \sqrt{N_C N_V}$
x_{s1} (strong inversion)	$\sim \frac{E_g}{2k_B T}$	~ 0
$\lim_{T\to 0} A_0\, e^{x_{s1}}$	$0 \times \infty = ?$	$\sqrt{N_C N_V}$





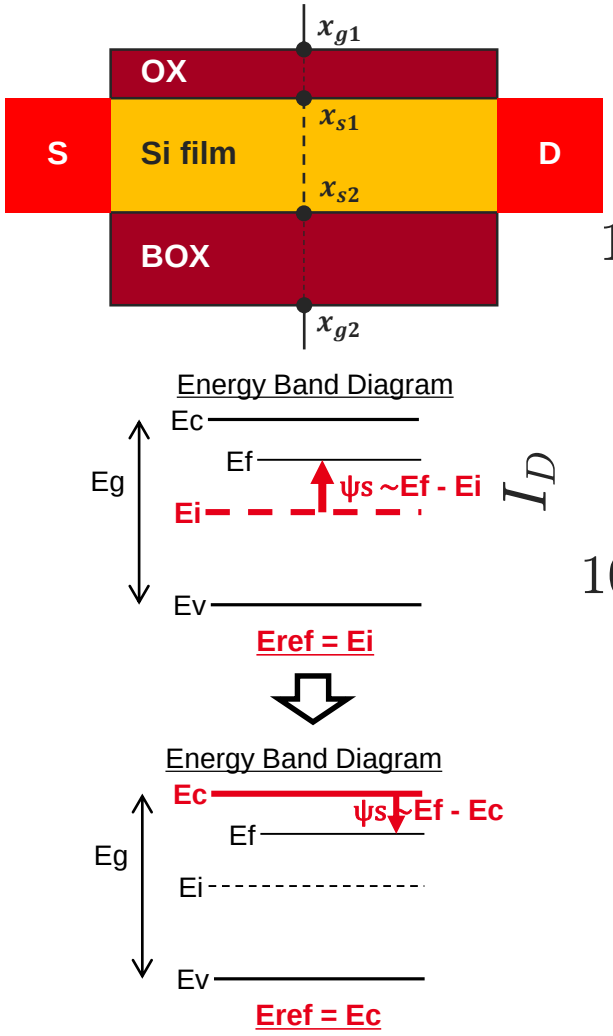


L-UTSOI Computational Cryo & solution 2/2

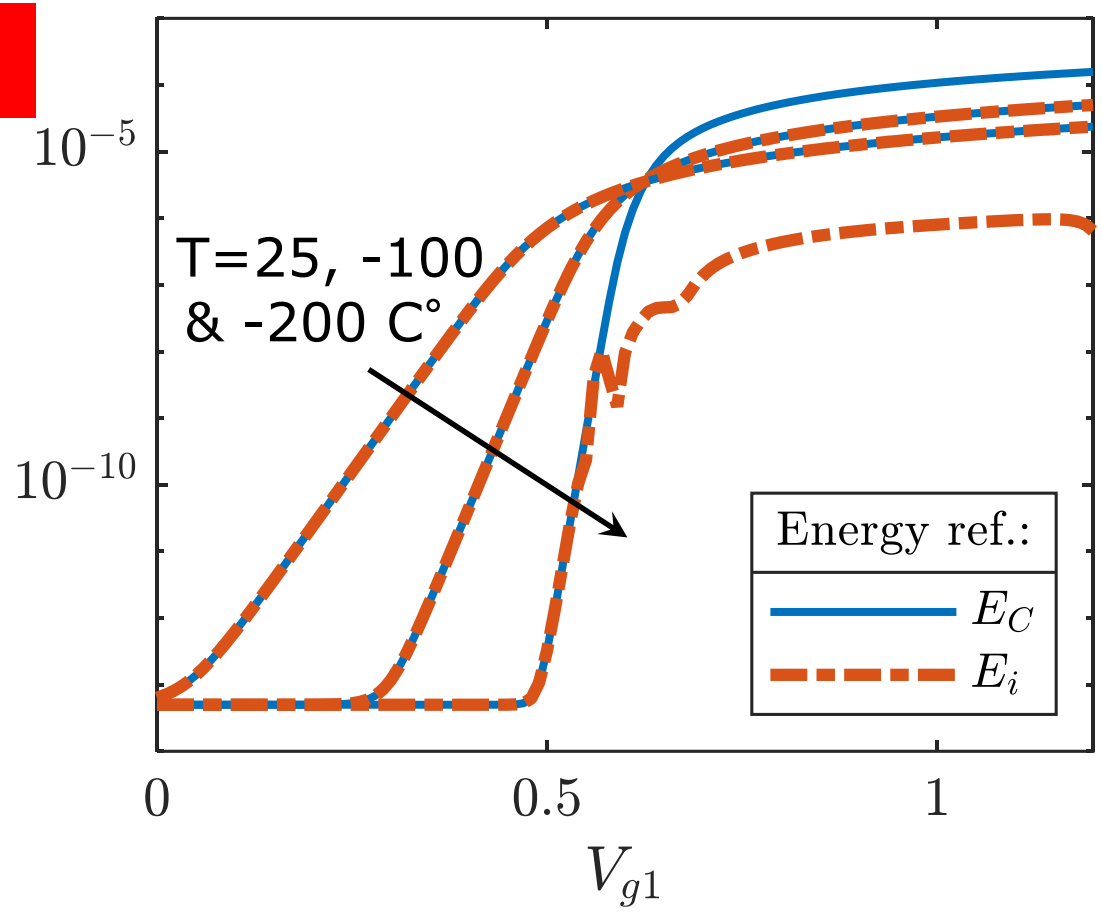
- L-UTSOI SPE:

$$\begin{cases} q^2 = k_1^2\left(x_{g1} - x_{s1}\right)^2 - A_0 e^{x_{s1}} e^{-x_n} \\ q^2 = k_2^2\left(x_{g2} - x_{s2}\right)^2 - A_0 e^{x_{s2}} e^{-x_n} \\ \frac{q}{2} + \coth^{-1}\left(\frac{k_1(x_{g1}-x_{s1})}{q}\right) - \coth^{-1}\left(\frac{k_2(x_{g2}-x_{s2})}{q}\right) = 0 \end{cases}$$

	L-UTSOI 102.6	L-UTSOI 102.7
Energy Reference	E_i	E_c
$A_0 \propto n_0$	$\sqrt{N_C N_V} e^{-\frac{E_g}{2k_B T}}$	$\propto \sqrt{N_C N_V}$
x_{s1} (strong inversion)	$\sim \frac{E_g}{2k_B T}$	~ 0
$\lim_{T\to 0} A_0 e^{x_{s1}}$	$0 \times \infty = ?$	$\sqrt{N_C N_V}$

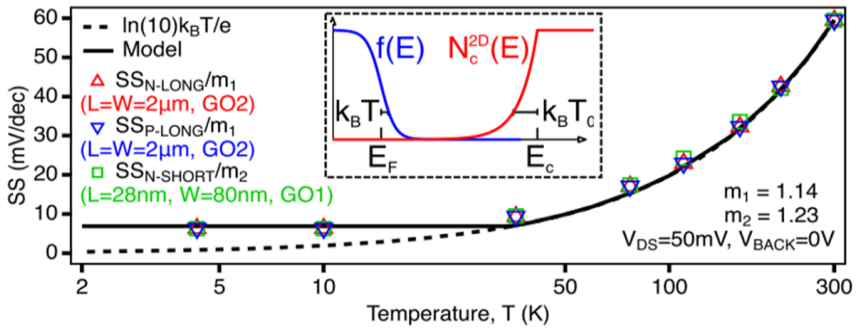


IdVg @ diff. Temp.

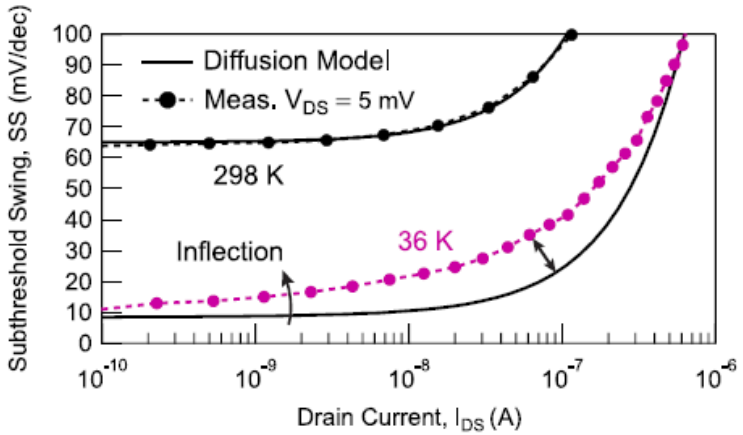


Introduction of band edge defects

- SS Saturation as the temperature decreases. Mechanism: Localized Band tail states acting as interface traps.



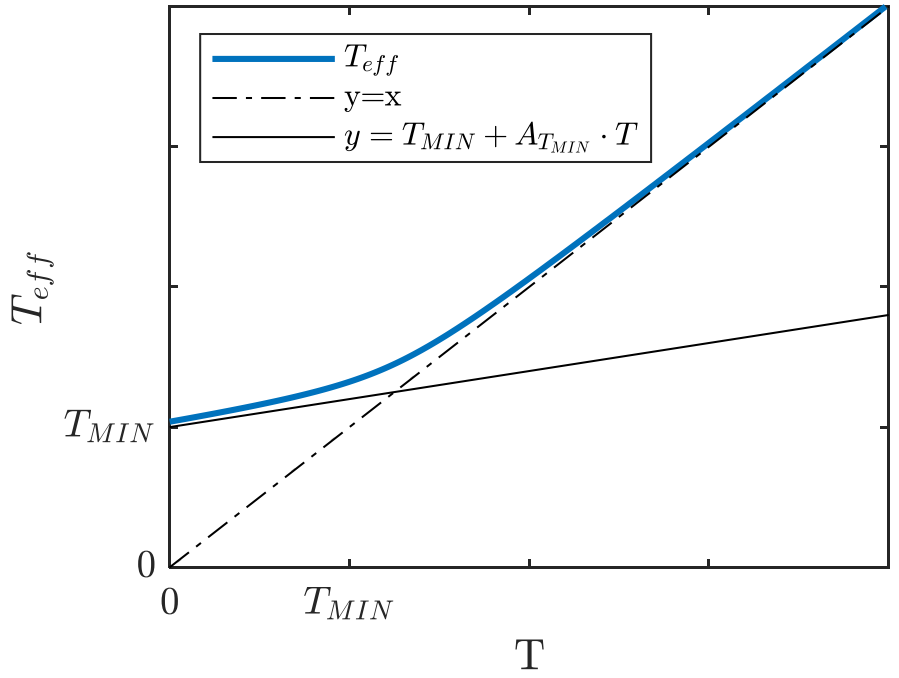
H. Bohuslavskyi et al EDL - 2019



Beckers et al. TED - 2020

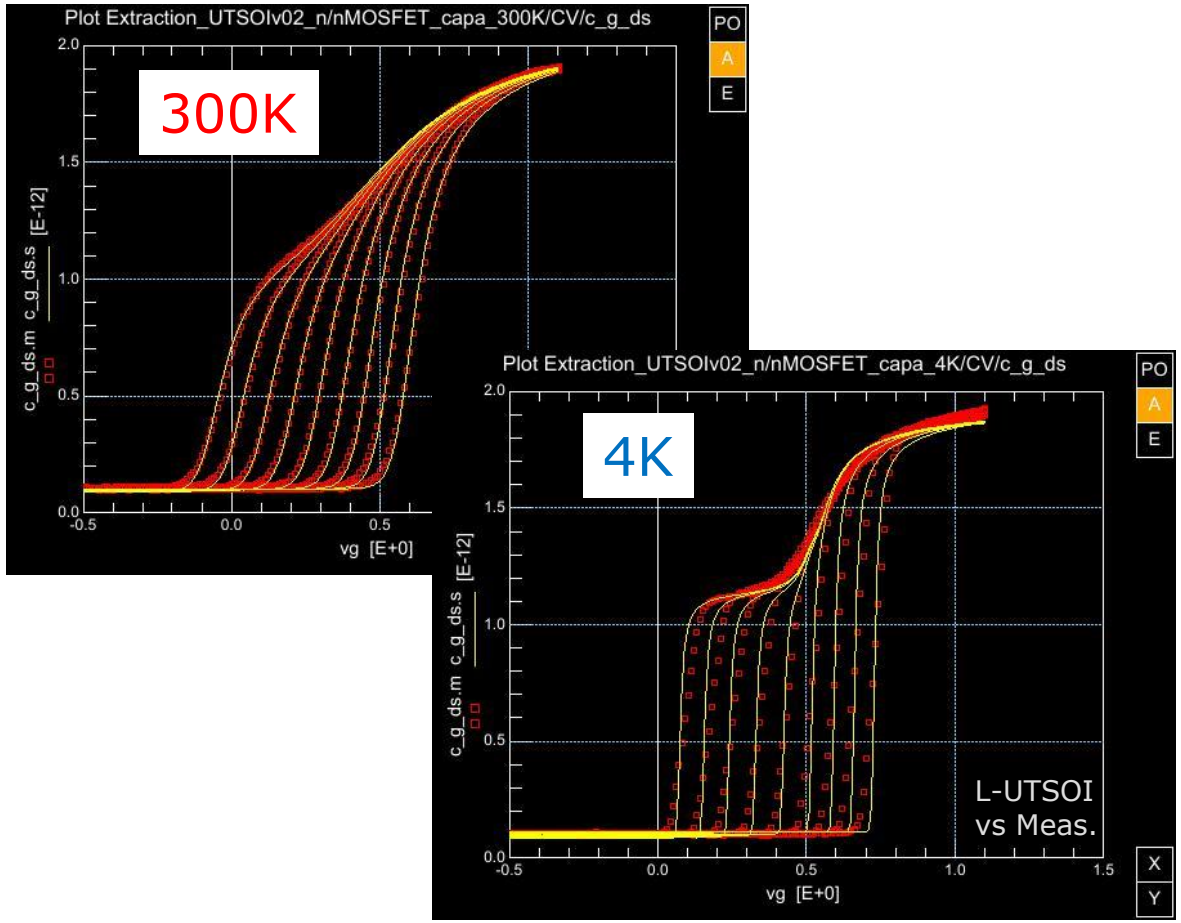
- **L-UTSOI: implementation temperature pinning:**

$$T_{eff} = \frac{T+T_0+\sqrt{(T-T_0)^2+B_{T_{MIN}}^2}}{2} \text{ w. } T_0 = T_{MIN} + A_{T_{MIN}} \cdot T$$

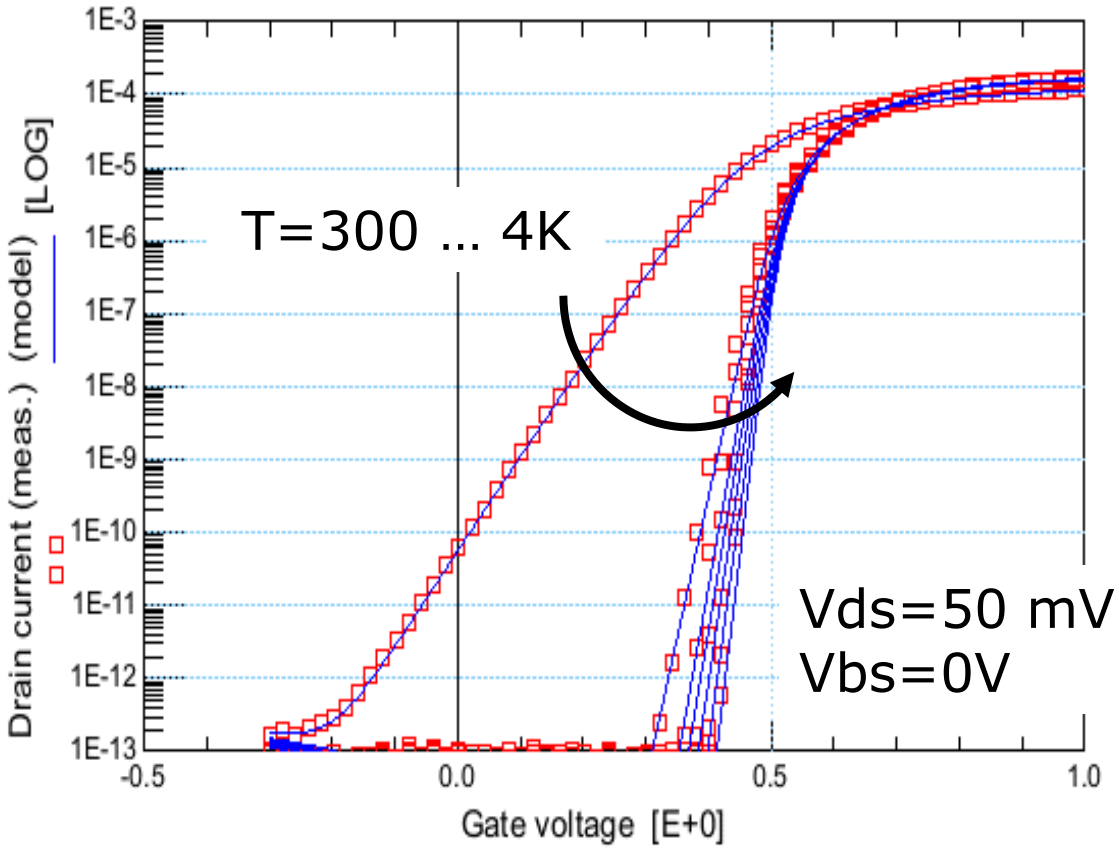


Cryo.: some illustrations

C-V @ diff. Temp. (mod. Vs exp.)



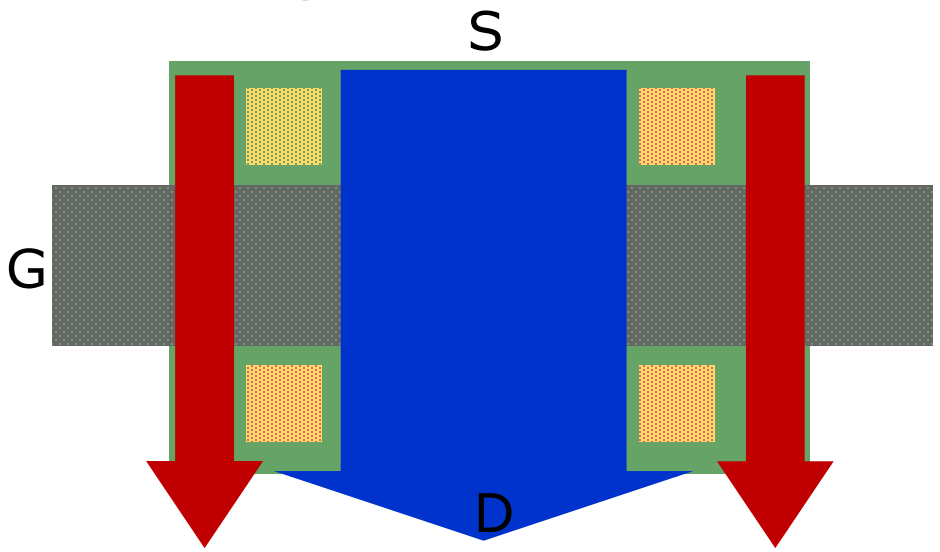
IdVg @ diff. Temp. (mod. Vs exp.)

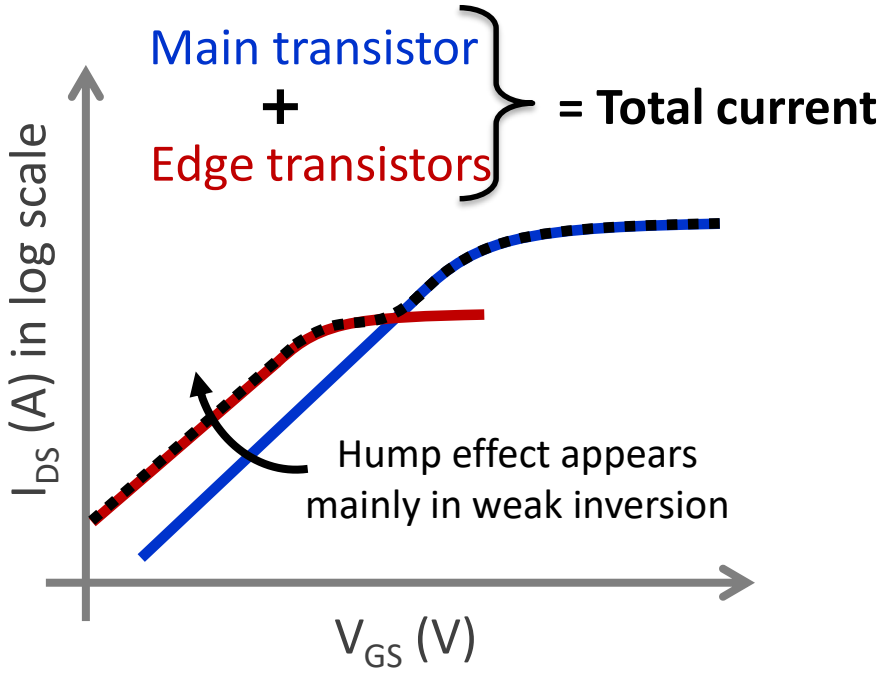


EDGE transistor

- Parasitic edge transistor is well known in bulk MOSFET

Effect of edge transistors on main one [1]





[1] K. Sakakibara et al. JJAP, May 2014.

Leakages induced by edge transistors 1/3

- Short model description

Goal: accurate model in weak and moderate inversions with limited degradation of the CPU run-time

Charge calculation

$$\begin{cases} q_i = q_{i,WI0} \cdot e^{-q_i} \cdot e^{-x_n} \\ q_i = \mathcal{W}_0\left(\frac{q_{i,WI0} \cdot e^{-x_n}}{nfactor}\right) \end{cases}$$

Simplified channel current calculation

$$\rightarrow \quad I_d = -I_{do}\left[\frac{1}{2}\left(q_{i,d}^2 - q_{i,s}^2\right) + \left(q_{i,d} - q_{i,s}\right)\right]$$

with: $I_{do} = \frac{W}{L} \cdot C'_{ox} \cdot \mu_{eff} \cdot {\phi_T}^2$

Notice: V_{dsat} is the one of main transistor

Id vs Vg @ Vd=50mV for Vb=-2 .. 2V with or without edge transistor

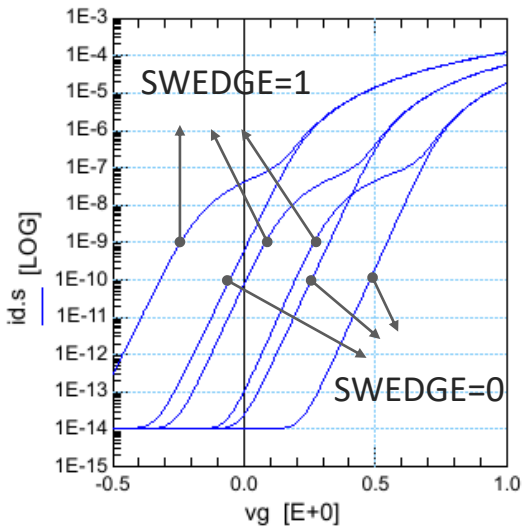
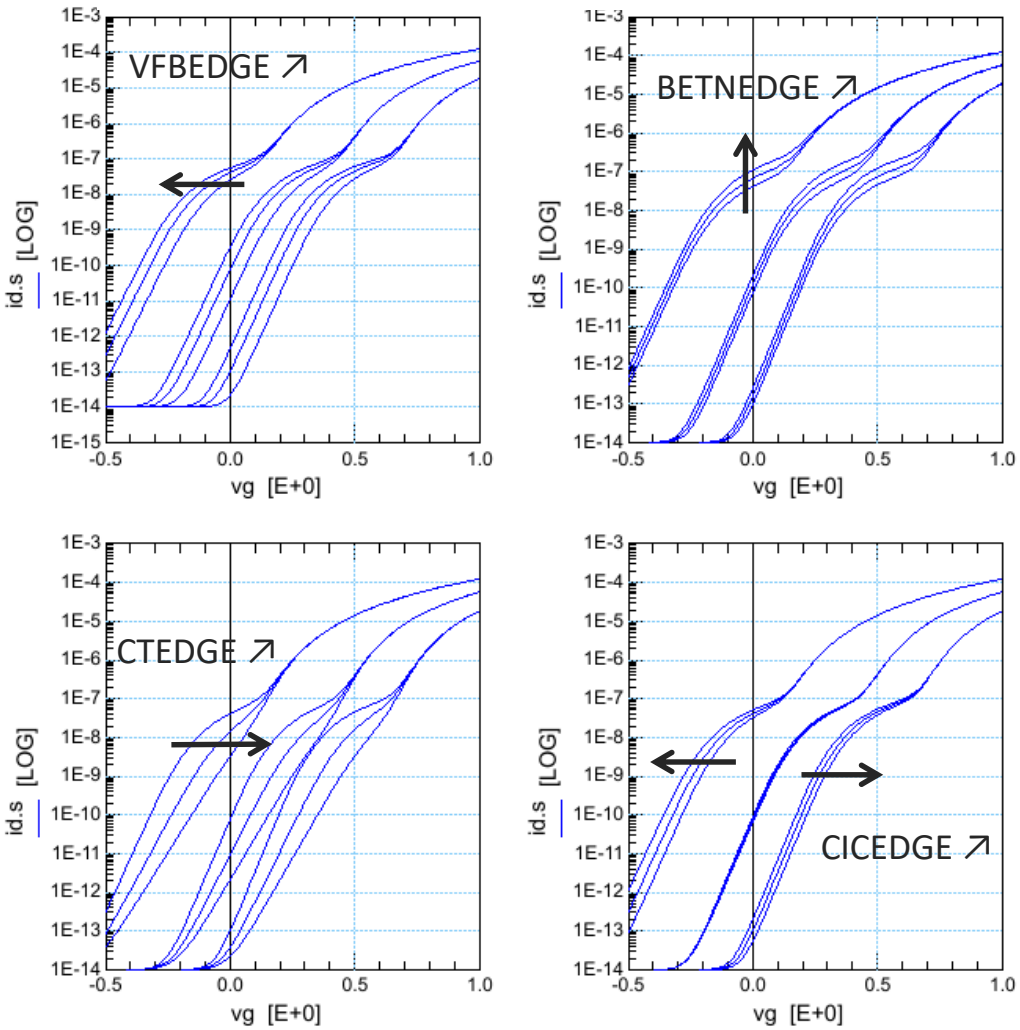


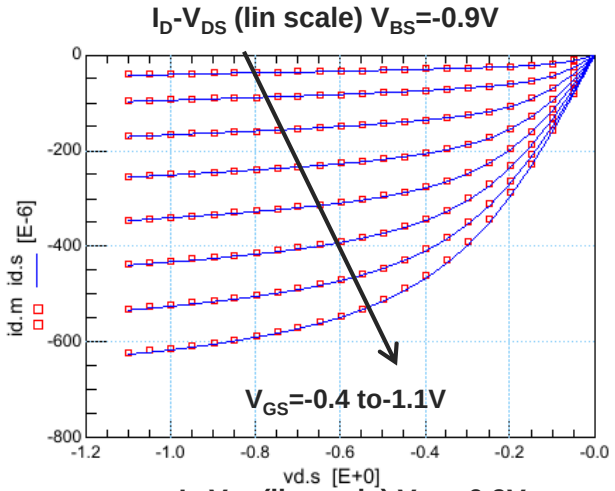
Illustration of model parameters effects
Id vs Vg @ Vd=50mV for Vb=-2 .. 2V

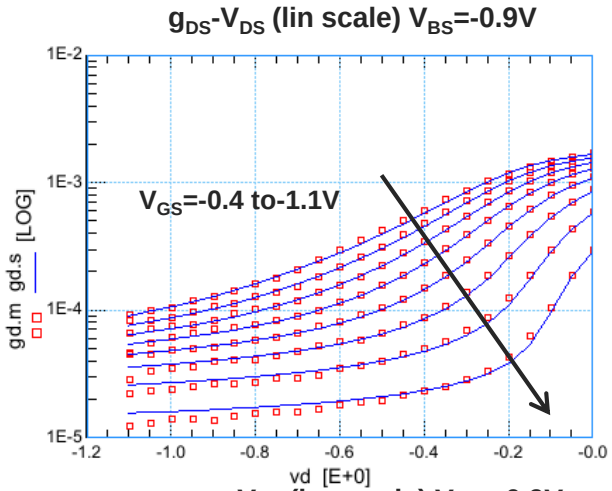


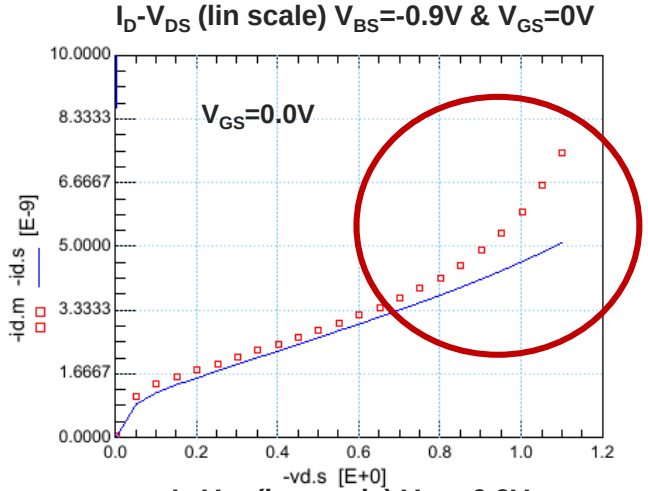
Leakages induced by edge transistors 2/3

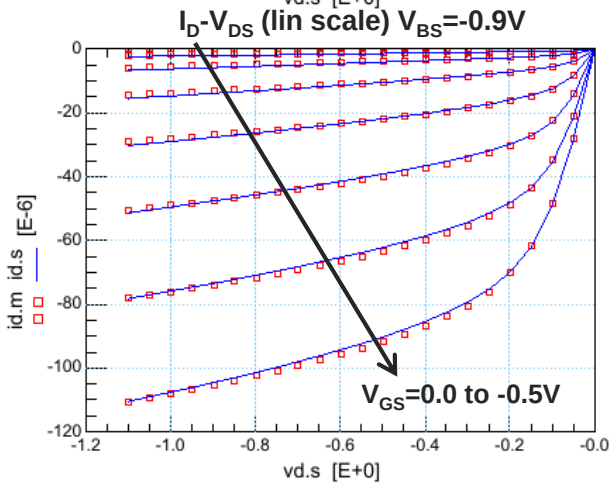
- Issue: difficulty to fit experimental data at negative Vbs

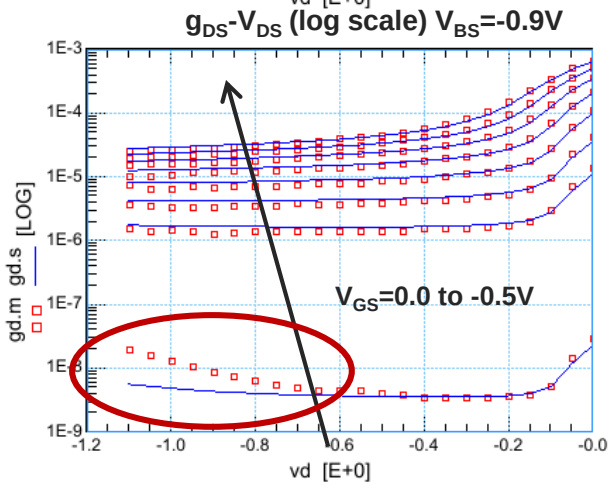
Short & Narrow device

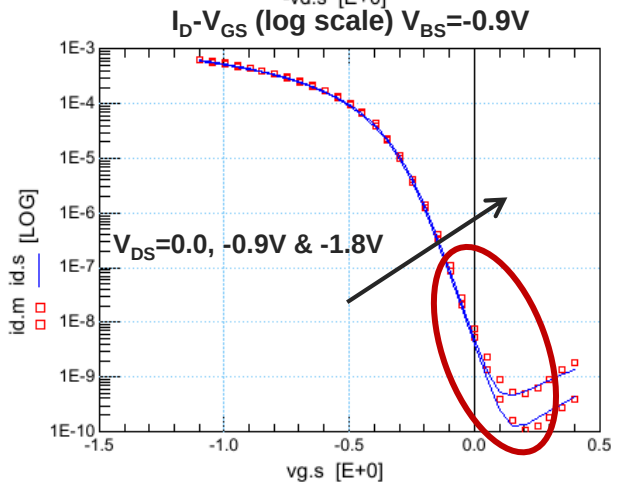








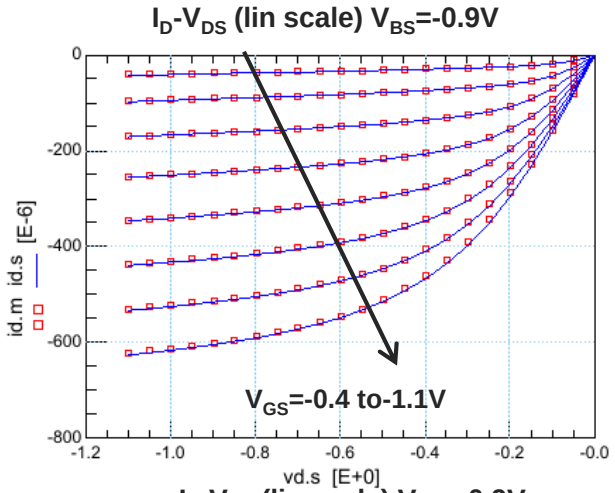


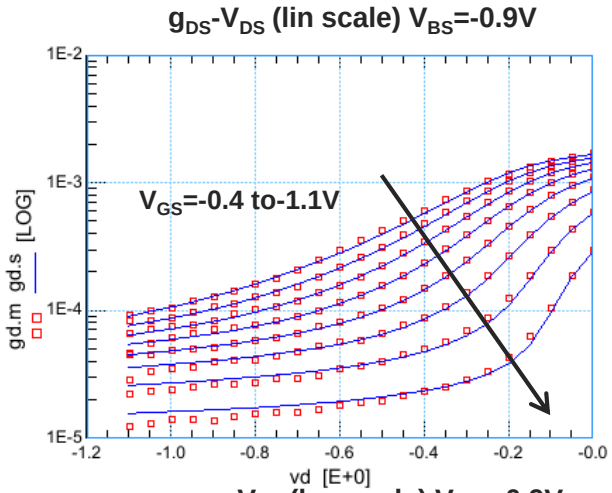


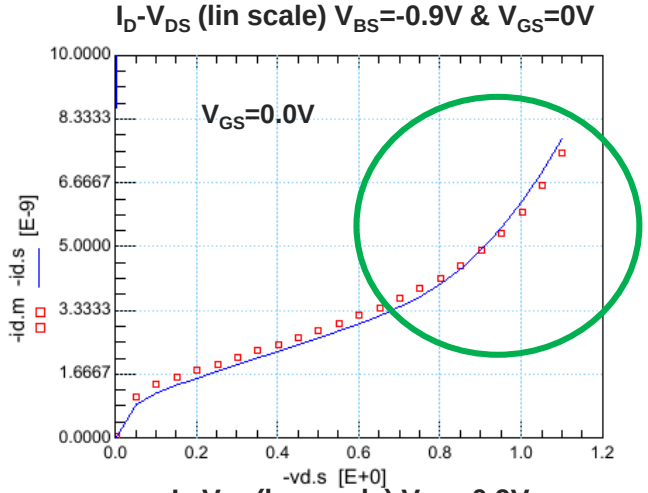
Leakages induced by edge transistors 3/3

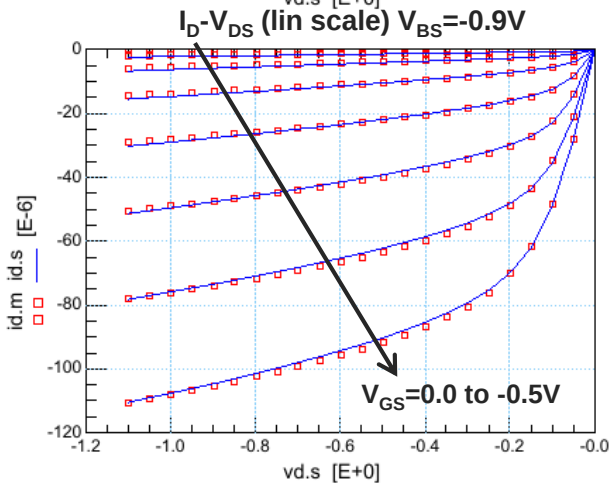
- Validation on experimental data

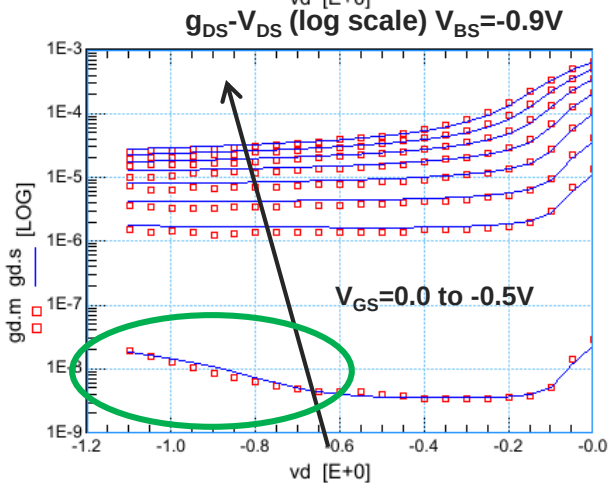
Short & Narrow device

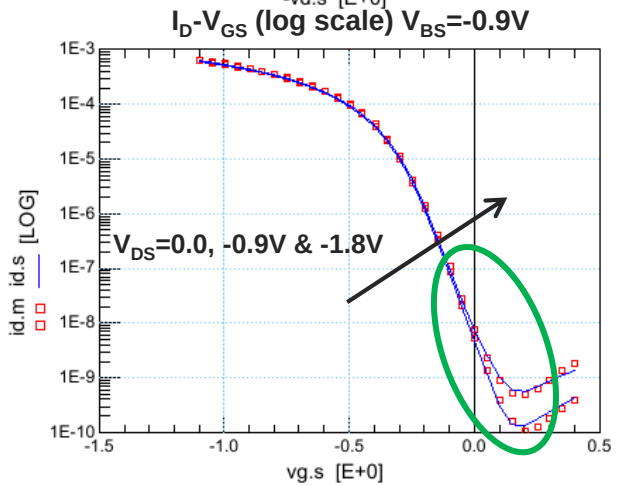








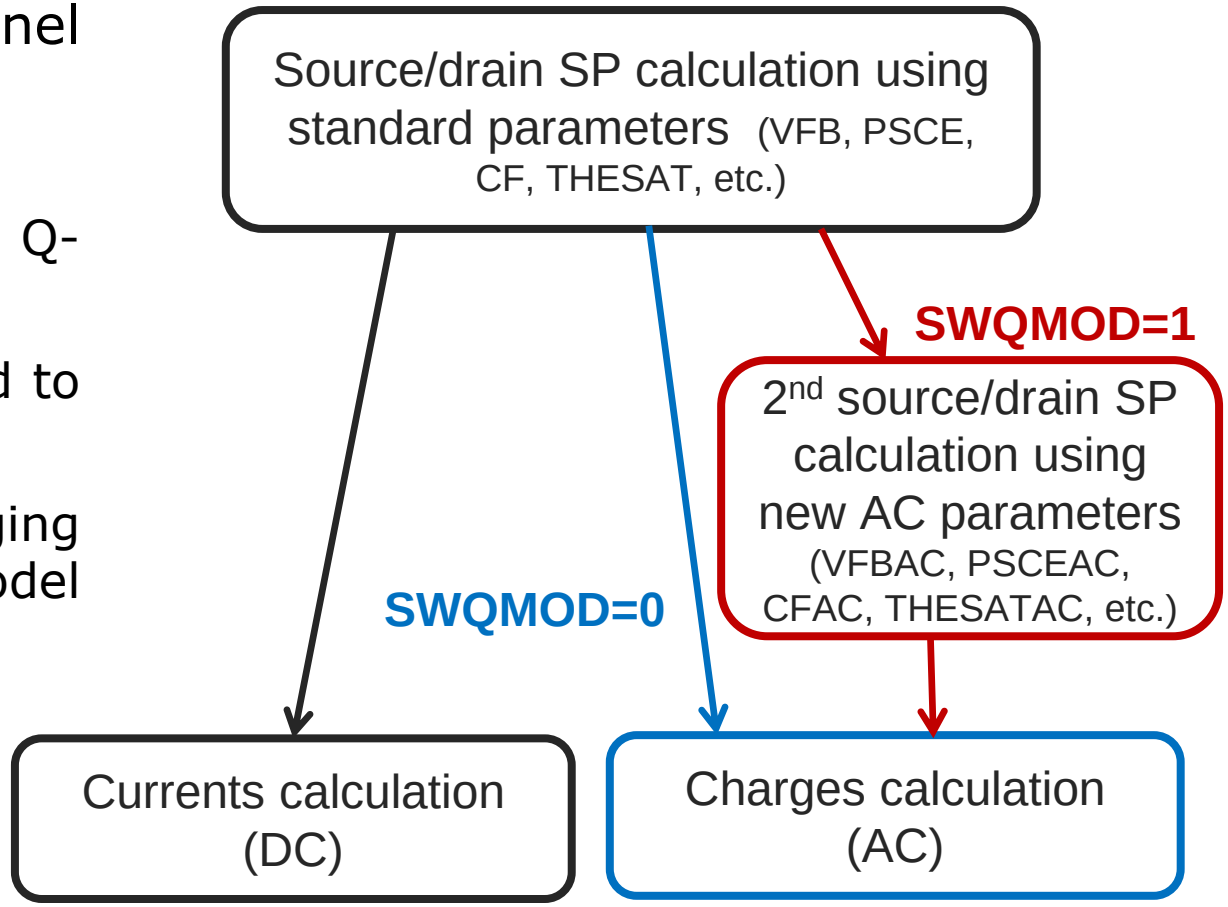




Q-model decoupling

- Issue: Q-model shows accuracy limitations in saturation regime for short channel transistors.
- Solution for L-UTSOI 102.8:
  - Introduction of new switch SWQMOD for Q-model decoupling.
  - Addition of new model parameters dedicated to Q-model
  - This solution requires significant code changing (charges are calculated twice when Q-model decoupling is activated)

Q-model decoupling is activated if SWQMOD=1



Outline

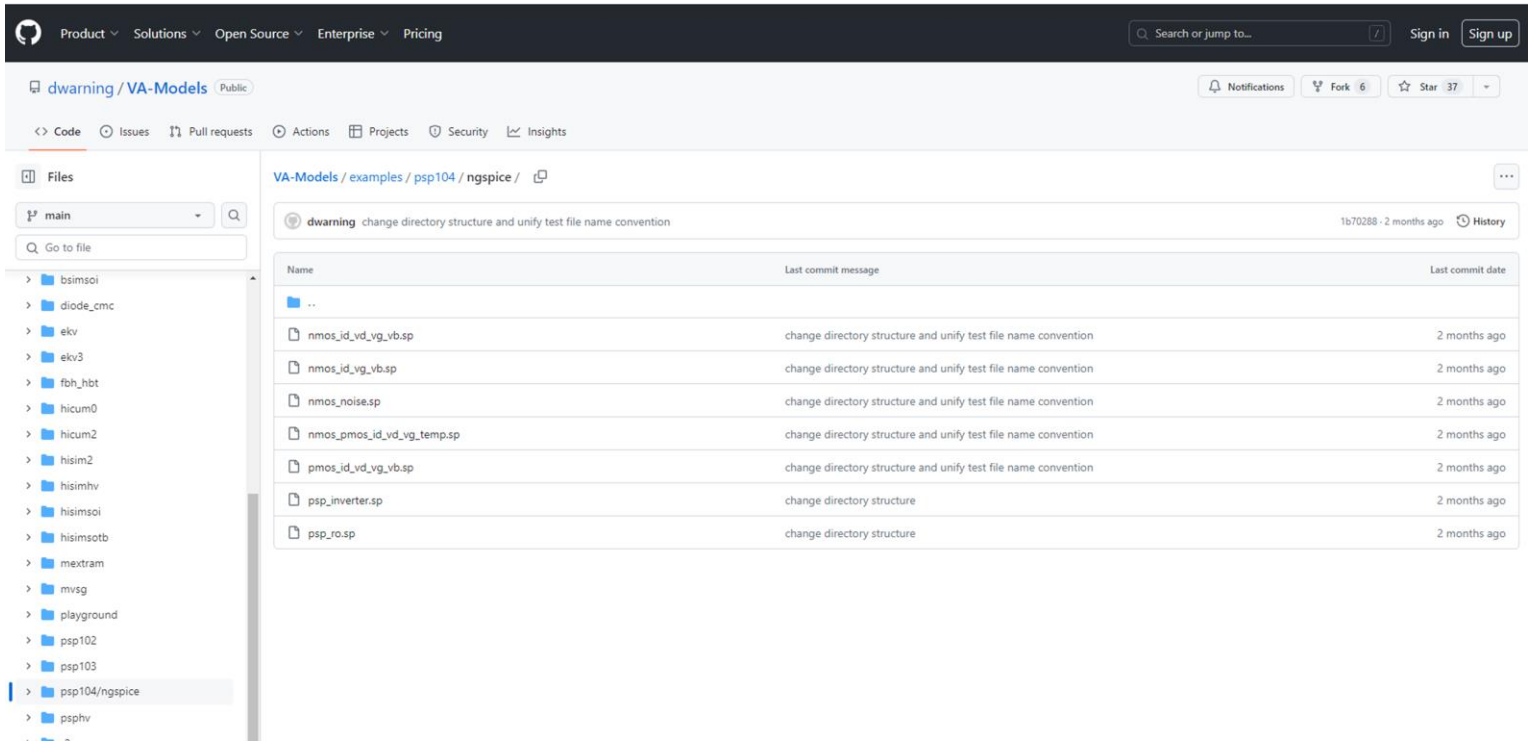
- Introduction
- PSP 104.0 new non backward compatible model
  - Summary of PSP version
  - PSP104 - Revise OP-output
  - PSP104 - Vdsat for long channel
  - PSP104 - Improved symmetry for low AX value
  - PSP104 - Improved Q-model in short channels
- L-UTSOI recent feature:
  - Summary of L-UTSOI version
  - L-UTSOI Computational Cryo issue & solution
  - Introduction of band edge defects
  - Cryo.: some illustrations
  - Leakages induced by edge transistors
  - Q-model decoupling
- **Conclusion**

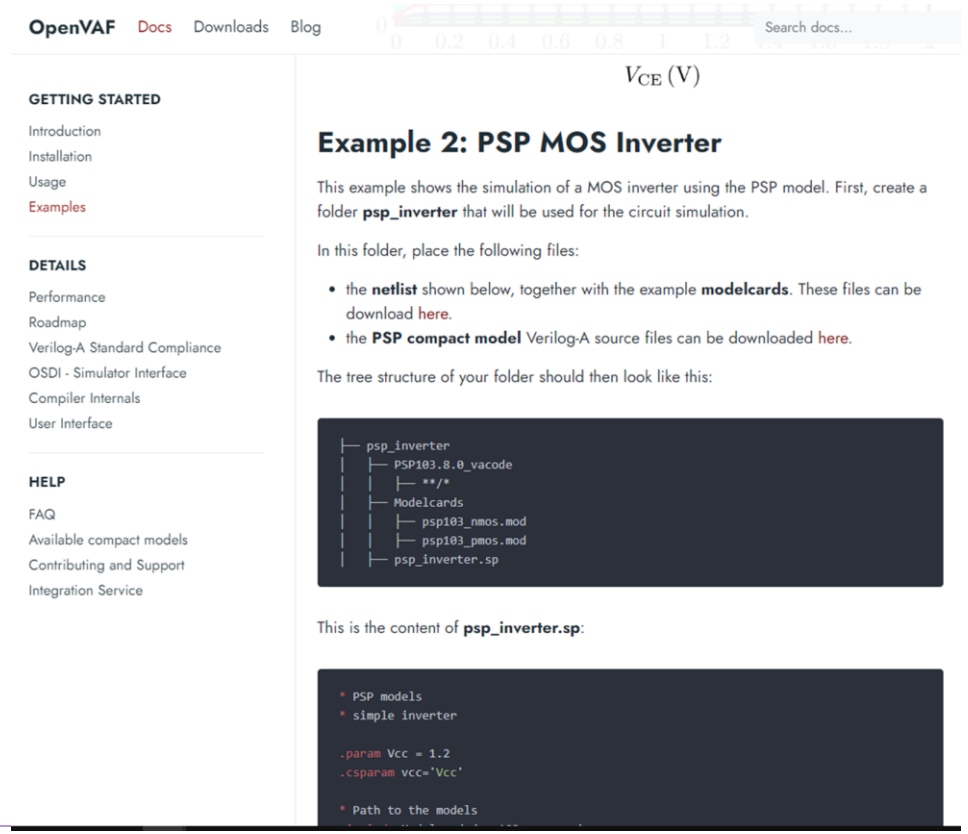
PSP & L-UTSOI is used by different community

- Here some example of input file using PSP or L-UTSOI with code: https://github.com/dwarning/VA-Models/tree/main/examples

we would to thanks the participants of these websites

- Here OPEN VAF website with PSP example: https://openvaf.semimod.de/docs/getting-started/examples/





Conclusion: Compact modeling @ CEA-LETI

- Our team is a developer of the CMC (Compact Model Coalition) for 2 SPICE models: standardization process, implementation in commercial IC simulators, strong interaction with users.
  - L-UTSOI compact model is dedicated to FDSOI technologies:

    https://www.cea.fr/cea-tech/leti/l-utsoisupport

  - PSP is a surface potential based model for deep-submicron bulk MOSFET:

    https://www.cea.fr/cea-tech/leti/pspsupport

  - Our website contains: Release information, Model documentation for PSP and L-UTSOI and Downloadable Verilog-A codes.

  - Acknowledgement: Gert-J. Smit (NXP), A. Scholten (NXP), H. Lee (Samsung), P. Scheer (ST) and all people that gives us feedback on our models to improve it.

- Code are also available through CMC link: *https://si2.org/download-links/*

- *L-UTSOI paper in ESSERC: "Cryogenic L-UTSOI Model for 22nm pMOS FD-SOI, Including Stress Effects",* *Miltiadis Alepidis, Sylvie Jarjayes, Thomas Bédécarrats, Sébastien Martinie, Mikaël Cassé, Christian Witt, Olivier Rozeau.*

Merci/thanks

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PSP104 - Improved binning rules

- New binning equations for PSP104: “hybrid” approach
  - New generic binning equation template

$$YYY = f_{scaling} \cdot \left(POYYY + PLYYY \cdot \frac{L_{EN}}{L_E} + PWYYY \cdot \frac{W_{EN}}{W_E} + PLWYYY \cdot \frac{L_{EN}}{L_E} \cdot \frac{W_{EN}}{W_E} \right)$$

Equation: type I

$f_{scaling}$ captures the dominant first order scaling trend (differs between parameters). Binning rule is always type-I

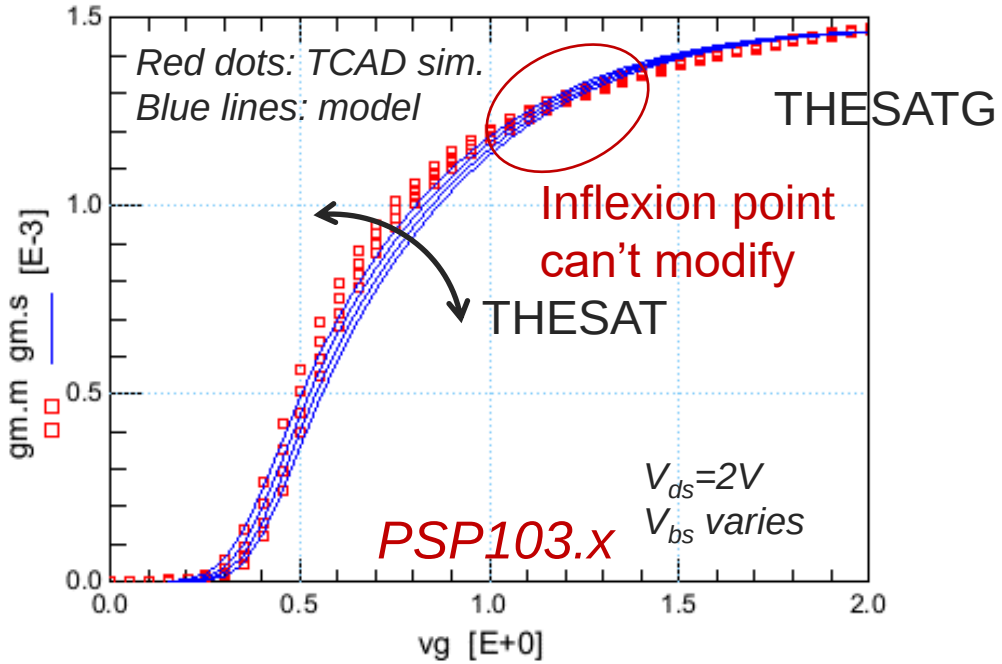
- Examples:

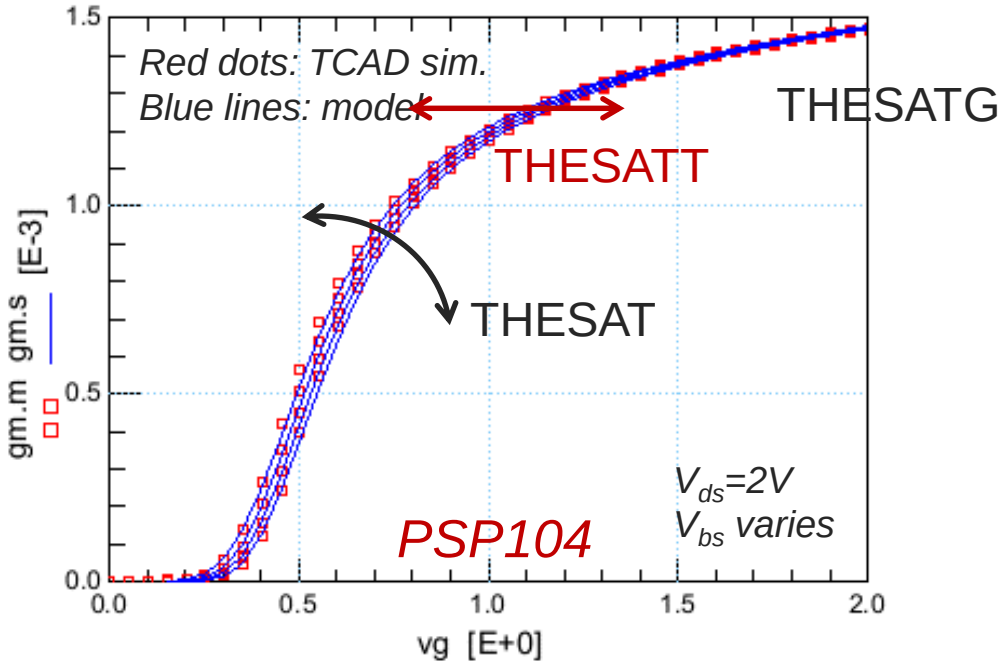
$$ALP = \frac{L_{EN}}{L_E} \cdot \left(POALP + PLALP \cdot \frac{L_{EN}}{L_E} + PWALP \cdot \frac{W_{EN}}{W_E} + PLWALP \cdot \frac{L_{EN}}{L_E} \cdot \frac{W_{EN}}{W_E} \right)$$

$$IGINV = \frac{L_E \cdot W_E}{L_{EN} \cdot W_{EN}} \cdot \left(POIGINV + PLIGINV \cdot \frac{L_{EN}}{L_E} + PWIGINV \cdot \frac{W_{EN}}{W_E} + PLWIGINV \cdot \frac{L_{EN}}{L_E} \cdot \frac{W_{EN}}{W_E} \right)$$

PSP104 - Improvement of G_m in saturation

- Issue: need flexibility to adjust gm in saturation
- Solution for PSP104: introduce a new parameter (THESATT) to adjust gate bias dependence of V_{DSAT}





Definition for low temp: generic example

The present Poisson equation is not representative of L-UTSOI model. This is just to illustrate the concept with more manageable equation.

$x_s = \frac{\psi_s}{kT/q}$: norm. electrostatic potential

Poisson equation

$$\frac{d^2x}{dy^2} = -\frac{q\,(p - n - N_a + N_d)}{\Phi_T\,\varepsilon_{Si}}$$

Using Boundary Condition …

$$(x_g - x_s)^2 = G^2 \exp(x_s)$$

	Usual def.	New def.
n_i	$\sqrt{N_c.N_V}.e^{\frac{-E_g}{2.\Phi_T}}$	$\sqrt{N_c.N_V}$
x_g	x_g	$x_g - \frac{E_g}{2.\Phi_T}$
G	$\frac{1}{C_{ox}}.\sqrt{\frac{2.q.n_i.\varepsilon_{ch}}{\Phi_T}}$	$\frac{1}{C_{ox}}.\sqrt{\frac{2.q.n_{inew}.\varepsilon_{ch}}{\Phi_T}}$