The IHP OpenPDK Initiative

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Outline

- IHP short introduction
- Short Story on Open Source Design / Motivation
- IHP Open Source EDA Flows
- Free MPW Runs 2024 & 2025

IHP at a Glance

- IHP is the **European research and innovation centre** for **silicon-based systems**, ultrahigh-frequency circuits and technologies
- The research focuses on **socially relevant topics** such as communication, mobility, health & environment, industry & agriculture, sustainability and security.
- **Unique selling point** of a **200mm pilot line** for state-of-the-art BiCMOS technologies, operated under **industry-like conditions, 24/7**, for the provision of prototypes and low-volume production runs.
- **Qualified technological platform** with direct access for science and industry

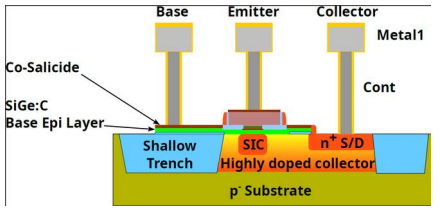
Vision

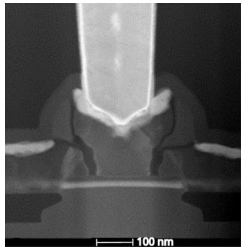
"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalised and networked world as well as for the sustainable preservation of our natural living conditions."

IHP at a Glance

	SG13S	SG13G2	SG13G3Cu
SiGe-HBT f_t / f_{max}	250 / 340 GHz	350 / 450 GHz	**470 / 650 GHz**
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	**130 nm**		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

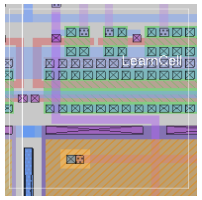
- Target are **high end applications** for RF & Terahertz frequencies, cryo, space
- SG13G2 is qualified and ready for **Low Volume of high end products** it was selected for the development of an **open PDK**
- SG13G3Cu is early access - qualification scheduled 2025





Open EDA cycle to push open hardware development

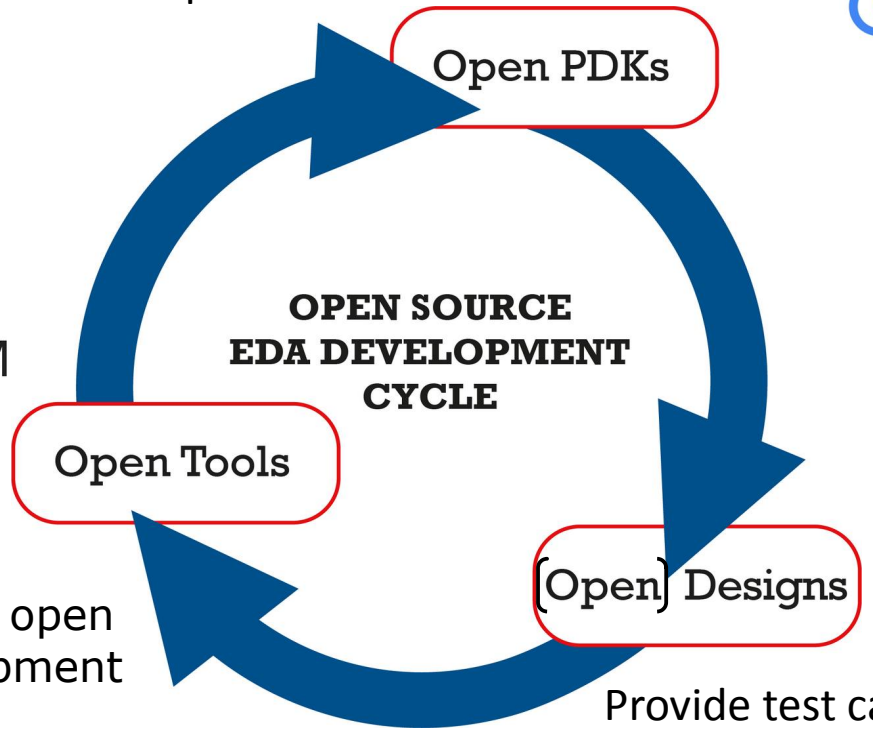
Enable open and worldwide collaboration on development of the PDK, co-development of tools and PDK features



Qucs

NGSPICE

XSCHEM



Google + skywater

Google + GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

IHP-Open-PDK

Provides platform for open EDA software development and possibility for collaborative design projects

Provide test cases, regression tests, benchmarks, use cases, user stories, feedback & error reports

RISC-V®

Open Source in a Nutshell

- Open-source - Open-access, exchange, collaboration, transparency on source code
- Benefits
  - No legal issues related to the NDA, ...
  - Collaboration, sharing efforts, enables re-use
  - Improves productivity, managing complexity
  - There is a lot of space for research
  - Lowers entry barriers
  - Promotes educations

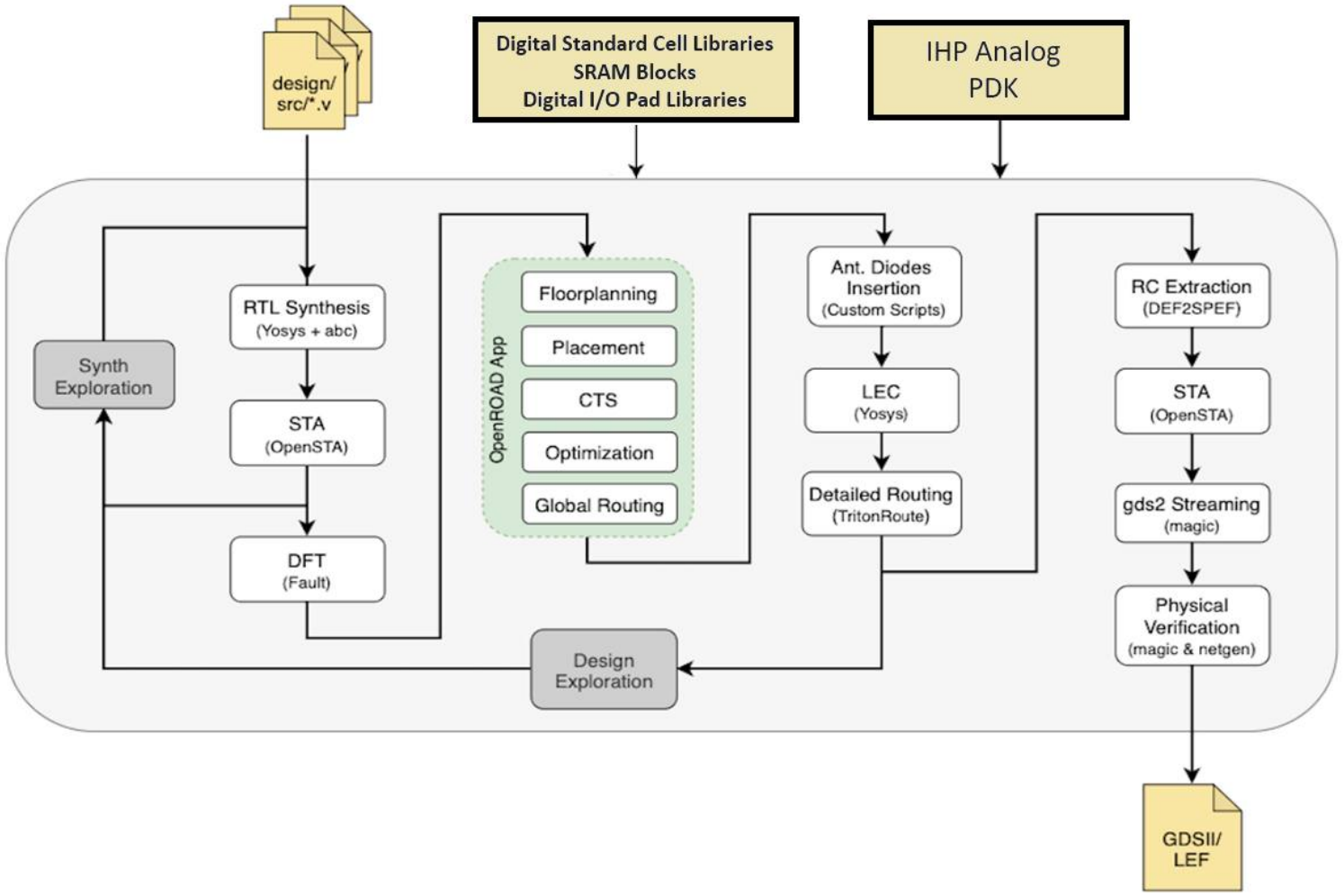
- Open source does not mean for “free”
  - You can make money with open-source (Google Android, RedHat, ChatGPT)
  - Proprietary vs. open-source (NOT: commercial vs. open-source)

Motivation for IHP’s open PDK initiative

- **Simplify access to education** materials for chip designers and to attract young people to get into chip design process
- Provide **low threshold (cost/technological) access to technology & PDK** for chip designer, academic projects
- Initiate cooperation's and joint projects with open source community
- **Be a pioneer** in demonstrating the possibilities of open source EDA software
- To **convince commercial fabs** to support the open source approach

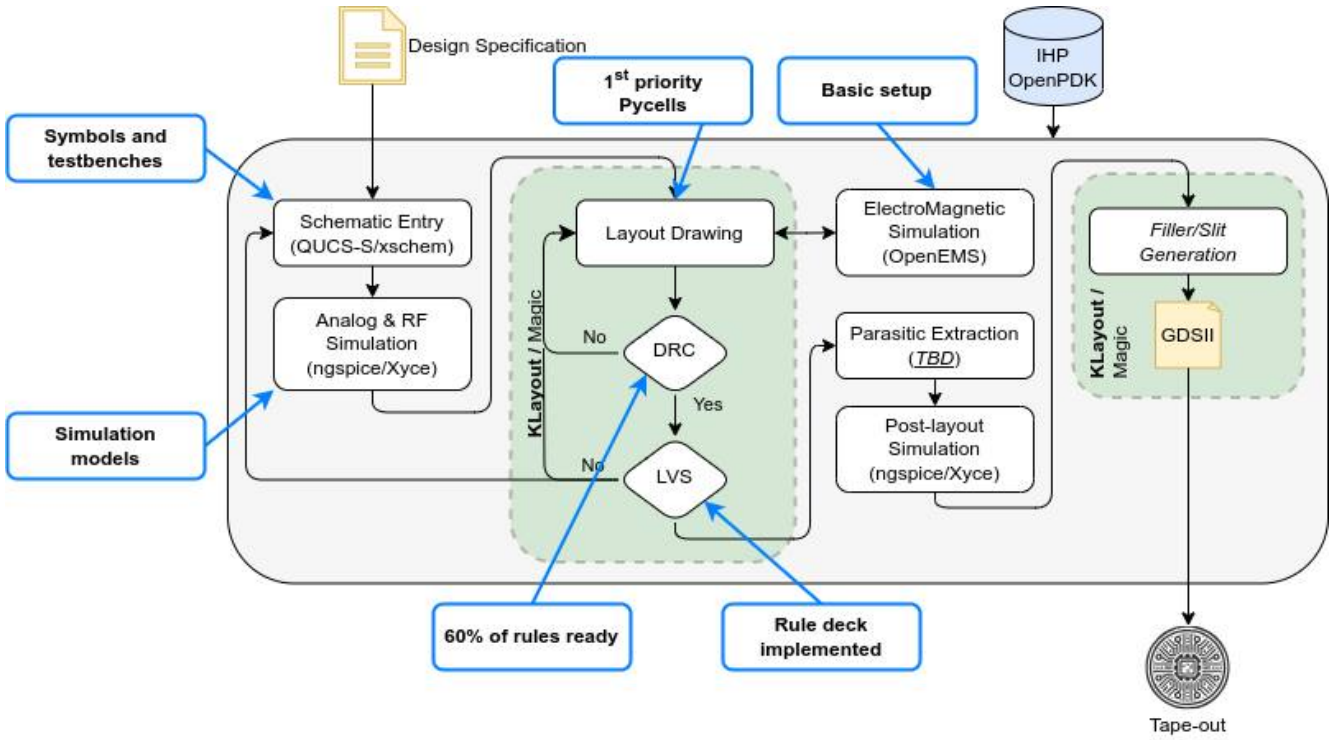
- Support chip design possibilities for **advance IC design projects** by **StartUp, SMEs and companies**

Digital Open Source Design Flow



- Analog PDK (Basics)
- Open Lane Apps
- Open Road Apps
- Digital Libraries

Analog/RF Open Design Flow - Challenges



- Interface development is crucial
- Lack of a complete open analog/RF design flow
- Open EDA Tools often handled by individual enthusiasts or small groups
- Open IC designs needed to improve Open EDA tools and foster its developments
- No other Open PDK available in EU
- No European concept for sustainable maintenance of the Open PDKs and Open EDA tools

Free MPW Runs - support open-source PDK & design

- The table provides schedule of MPW Runs for FMD-QNC project in 2024 and 2025

Tape out date	22/05/24	11/11/24	22/11/24	01/03/25	09/05/25	18/07/25	15/09/25
Technology	SG13G2	SG13CMOS	SG13G2	SG13G2	SG13G2	SG13G2	SG13CMOS
Area [mm^2]	10	220	20	140	30	30	220

- Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others
- A concept for sustainable provision of free or low-cost MPW area for the open source community from 2026 is under development. First details at FSIC 2024:
  wiki.f-si.org/index.php?title=Update_on_IHP_open_source_PDK_initiative_%26_how_to_submit_free_open_source_designs_in_IHP_technology

Criteria for design IP selection from open community

Mandatory criteria for IP selection

- Completeness of IP data (all data need to be open source)
- DRC error free designs
- Area below 2 mm2 preferred (larger designs only if area is available)
- Potential export restrictions

Additional criteria for IP selection

- First time submission (preferred)
- Design should use open source tools supported by IHP open PDK
- For SG13G2 runs designs using SiGe (preferred)
- Documentation quality
- Uniqueness, not yet seen designs (i.e. if there were no ADCs before, an ADC design would get a higher point)

Flow to upload designs for open MPW

- Before a design can be considered for fabrication start a pull request at https://github.com/IHP-GmbH/IHP-Open-DesignLib <- this can change
- All design data need to be submitted at least 2 weeks before TAPE OUT
- Europractice will check designs regarding mandatory criteria

- Selected GDS files will be used for TAPE OUT by IHP
- IHP can rent samples for joint evaluation under certain agreement, which need to be signed
- Evaluation results need to be published: https://github.com/IHP-GmbH/IHP-Open-DesignLib
- Evaluation to provide permanent samples are under evaluation

Goal is to build an open source design library for future projects

Outlook

- Development of digital certified design course Q4 2024
- Development of analog design course Q2 2025
- BmbF initiative : Design tools for sovereign chip development with open source (DE:Sign) started May/June 24
  - Flowspace – Radiation hard library, aging models, 1/f noise (ngspice)
  - Demico – 60 GHz Design, improvement of EM solver (open EMS)
  - SignHep – SRAM generator, RoT elements, OTP, RRAM module for neuronal …
  - OCDCpro – Develop design challenge on secure designs

Acknowledgment

- Thanks to open source community SemiMod, ETH Zurich, Uni Linz, ChipFlow, Staf Verhaegen (PDKMaster), M. Koefferlein (klayout), D. Warning, H. Vogt (ngspice), M. Brinson (Qucs-S), and many more …
- Thanks to different public founded German projects:

  VE-HEP (16KIS1339K) https://elektronikforschung.de/projekte/ve-hep-1

  IHP Open130-G2 (16ME0852)https://www.elektronikforschung.de/projekte/ihp-open130-g2

  FMD-QNC (16ME0831) https://www.elektronikforschung.de/projekte/fmd-qnc

  Design tools for sovereign chip development with open source (DE:Sign) started May 24

  Flowspace, OCDCpro, SignHep, Demico