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Physics-Based Analytical Model of Nanowire Tunnel-FETs

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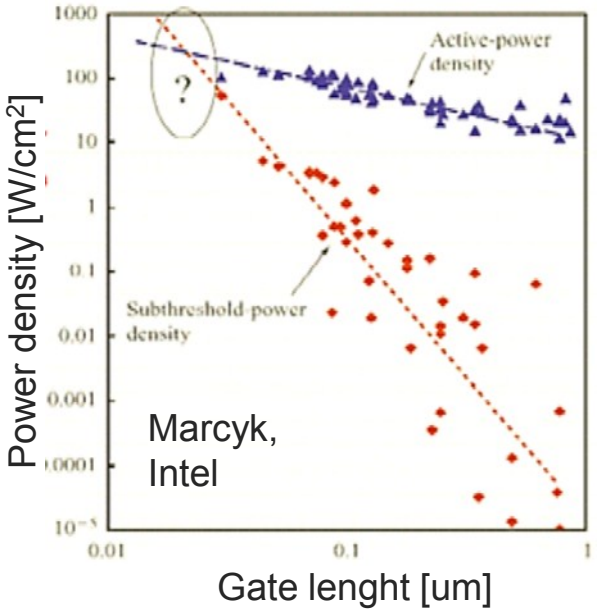
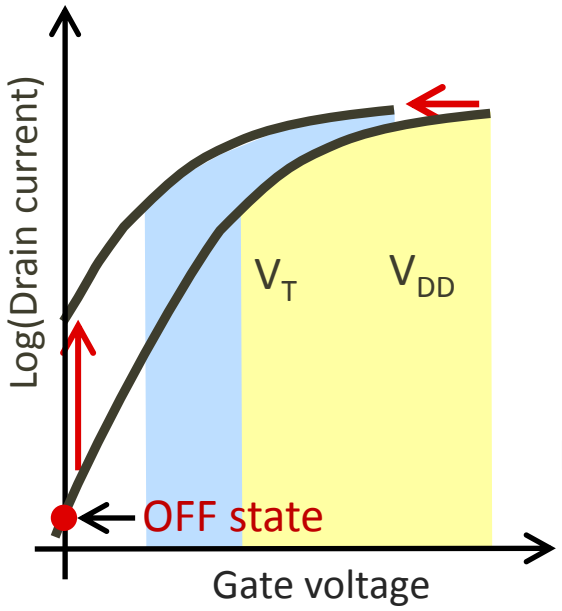
Outline

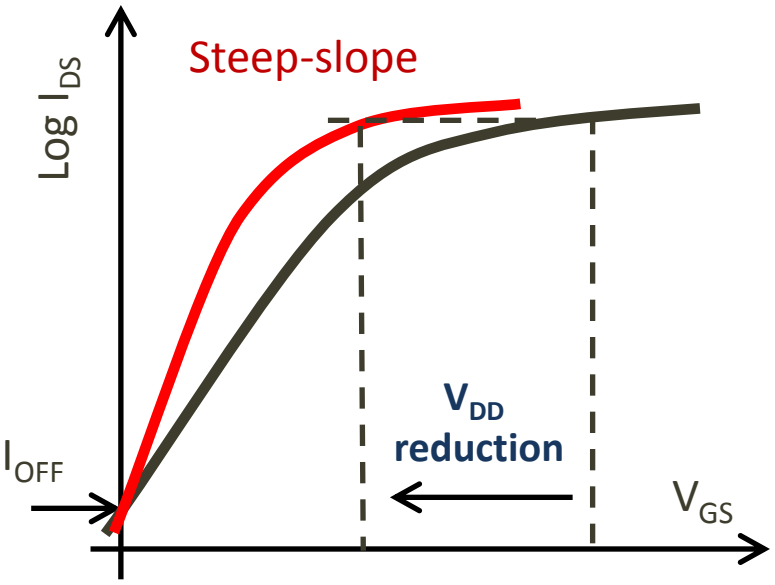
- Introduction and motivation
- Band-to-band Tunnel FETs
- Analytical model
  - drain current;
  - output conductance at zero V_{DS};
  - transconductance → SS
- Device optimization
- Conclusions

Motivation

- 10% (800TWh) of the global energy consumption is due to electronic devices, mostly for ICT and CE.
- Minimizing power consumption without compromising performance creates a new set of challenges.
- V_{DD} scaling implies a proportional V_T scaling → exponential growth of the leakage current

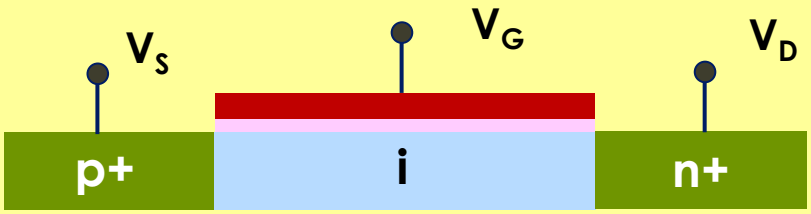






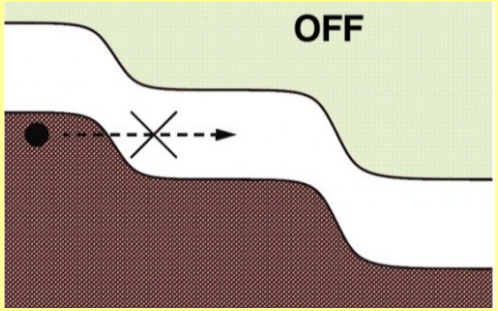
Novel device concept: the Tunnel FET

filter high-energies



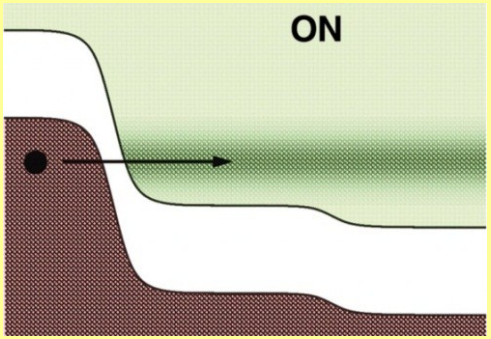
OFF-state

- V_d = positive
- V_g = 0
- **no current flows**



ON-state

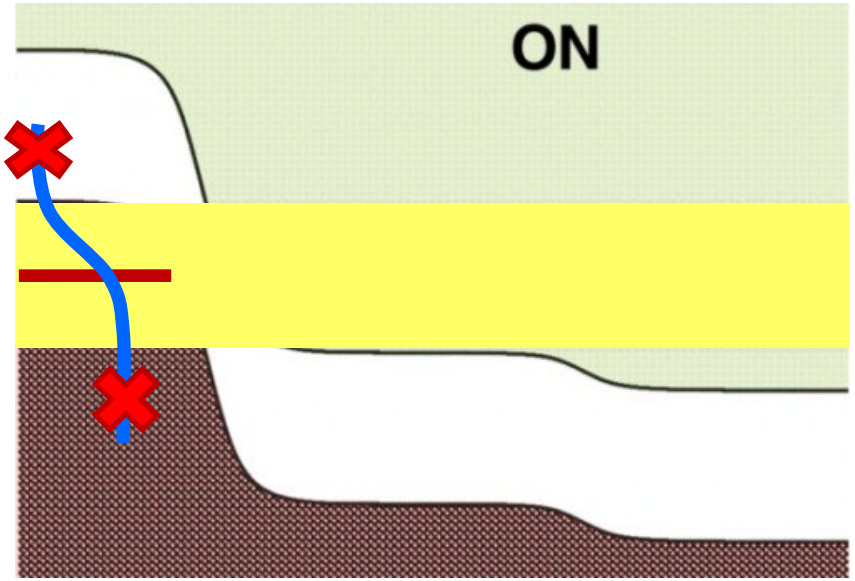
- V_d = positive
- V_g = positive
- **barrier thin, current flows**



BTBT acts as bandpass filter cutting off the tails of the Fermi function

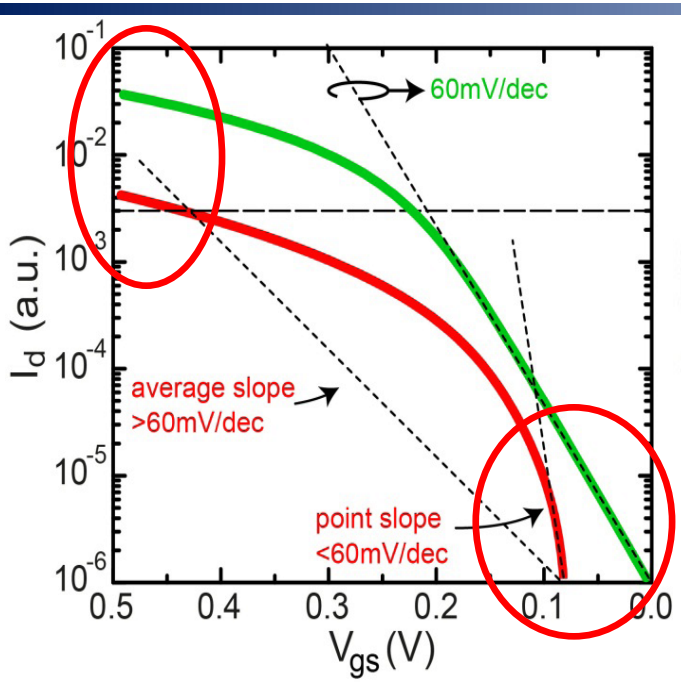
➔ effective cooling down the system

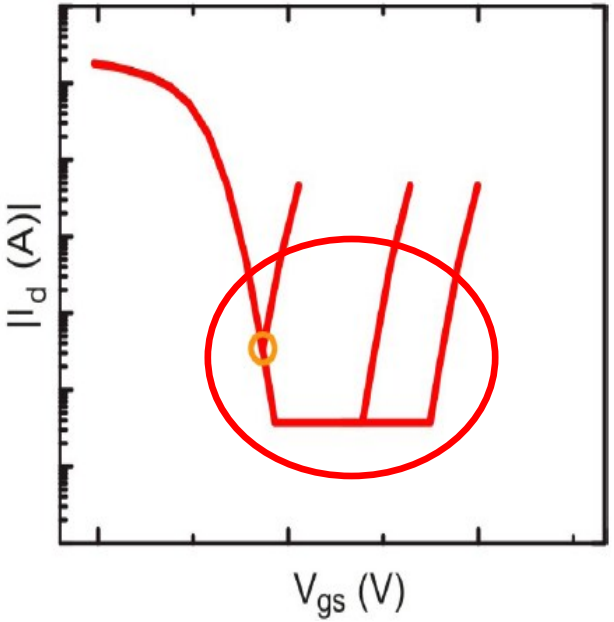
➔ S < 60 mV/dec possible

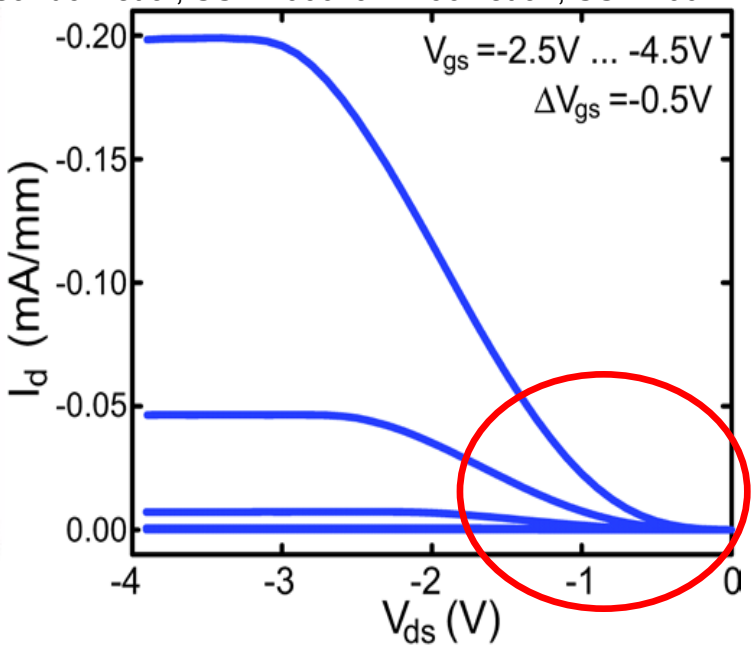


Unsolved deficiencies

C. Sandow et al, SSE 2009. J. Knoch et al., SSE 2007.



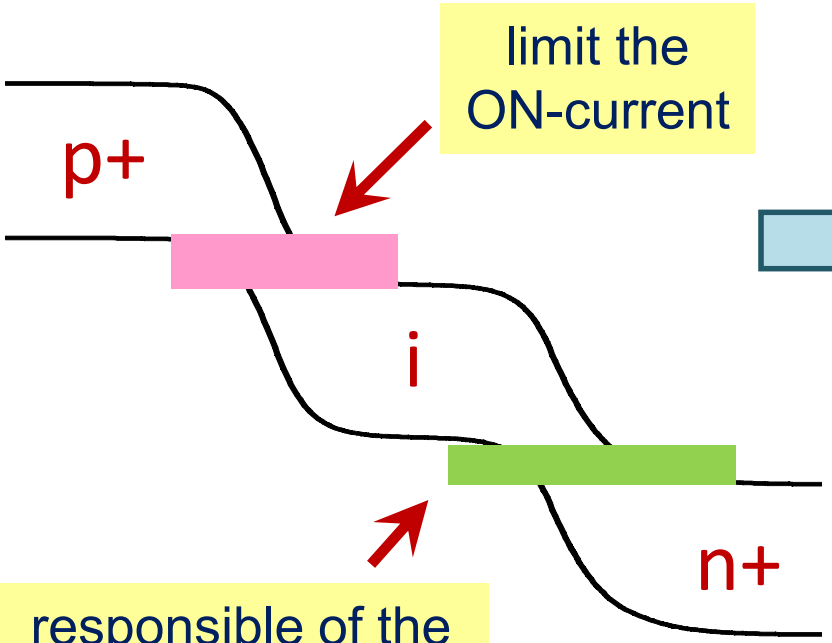


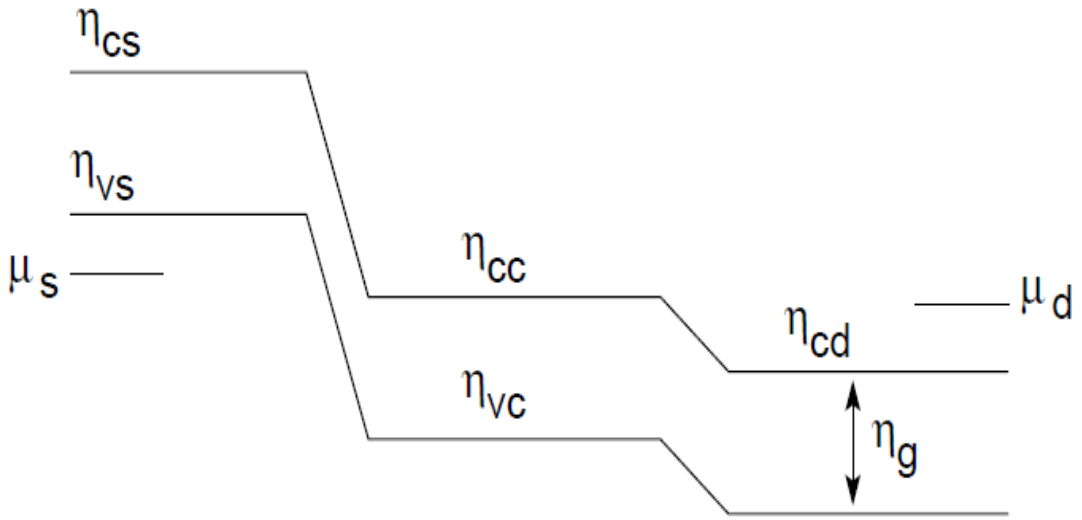


- ON-currents typically much smaller than standard CMOS FETs;
- SS < 60mV/dec only in small V_{gs} range → average slope > 60mV/dec;
- ambipolar effect → it degrades SS and the I_{ON}/I_{OFF} ratio.
- exponential increase of $I_d - V_{ds}$ curves at low drain voltages;

analytical model to gain a deeper insight into the device properties and to work out an optimal device design

Ballistic current for NW-TFETs





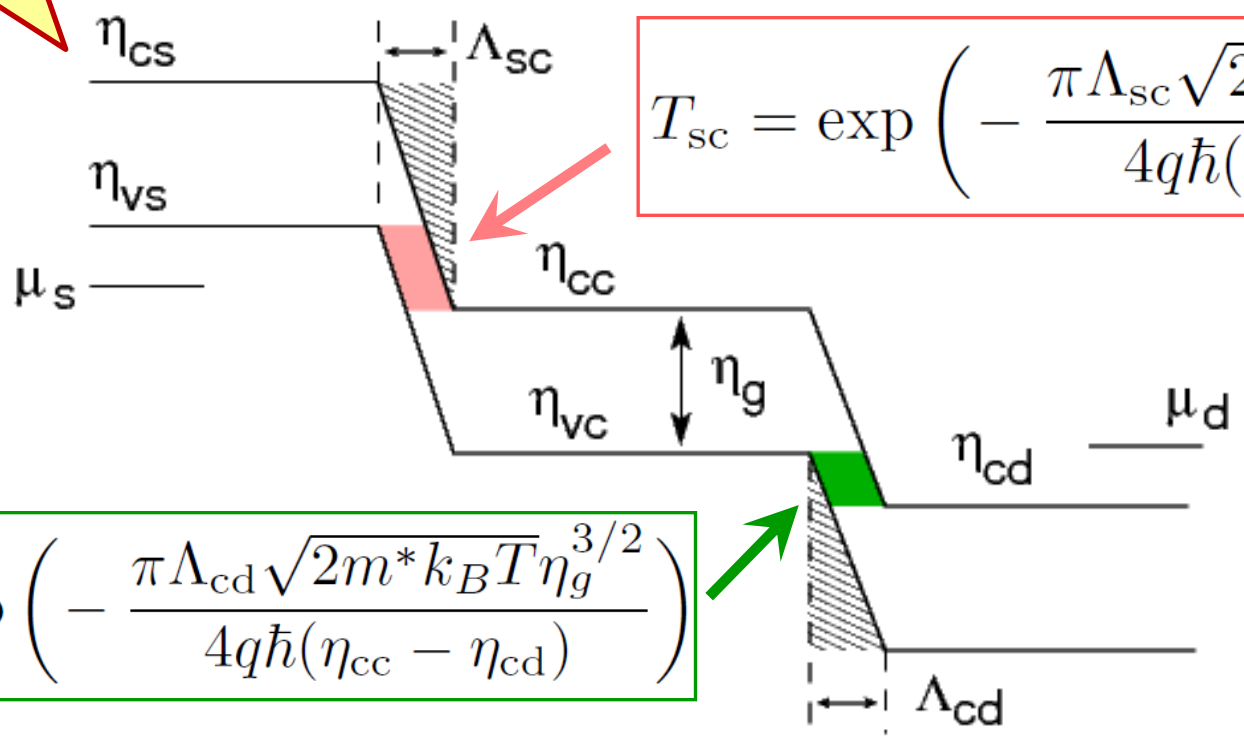
$$I_D = \frac{2qk_BT}{h}\int_{-\infty}^{\infty} T_p(\eta)\left[f(\eta-\mu_s)-f(\eta-\mu_d)\right]\mathrm{d}\eta$$

!! tunneling probability !!

WKB + Flietner's energy band expression

$$T = \exp\left\{-2\int_{x_1}^{x_2}\kappa(\varepsilon)dx\right\} \quad + \quad E\left(1-\frac{E}{E_G}\right) = \frac{\hbar^2 k^2}{2m^*}$$

constant field



$$T_{sc} = \exp\left(-\frac{\pi\Lambda_{sc}\sqrt{2m^* k_B T}\eta_g^{3/2}}{4q\hbar(\eta_{cs}-\eta_{cc})}\right)$$

$$T_{cd} = \exp\left(-\frac{\pi\Lambda_{cd}\sqrt{2m^* k_B T}\eta_g^{3/2}}{4q\hbar(\eta_{cc}-\eta_{cd})}\right)$$

Drain current model

The drain current is expressed as the sum of the two contributions:

$$I_D = I_D^{\mathrm{sc}} + I_D^{\mathrm{cd}}$$

$$I_D^{\mathrm{sc}} = \frac{2qk_BT}{h} T_{\mathrm{sc}} \left\{ \ln\left(\frac{1+\exp\left(\mu_s - \eta_{\max}\right)}{1+\exp\left(\mu_s - \eta_{\mathrm{vs}}\right)} \right) - \ln\left(\frac{1+\exp\left(\mu_d - \eta_{\max}\right)}{1+\exp\left(\mu_d - \eta_{\mathrm{vs}}\right)} \right) \right\} \theta(\eta_{\mathrm{vs}} - \eta_{\max})$$

$$I_D^{\mathrm{cd}} = \frac{2qk_BT}{h} T_{\mathrm{cd}} \left\{ \ln\left(\frac{1+\exp\left(\mu_s - \eta_{\mathrm{cd}}\right)}{1+\exp\left(\mu_s - \eta_{\mathrm{vc}}\right)} \right) - \ln\left(\frac{1+\exp\left(\mu_d - \eta_{\mathrm{cd}}\right)}{1+\exp\left(\mu_d - \eta_{\mathrm{vc}}\right)} \right) \right\} \theta(\eta_{\mathrm{vc}} - \eta_{\mathrm{cd}})$$

➔ Depending on the gate and drain voltages, the bandgap and the source and drain degeneracy levels, each contribution can vanish, if the argument of the step function $\theta(\eta)$ becomes negative.

Drain conductance at zero V_{DS}

If V_{DS} is vanishingly-small we can compute the drain conductance:

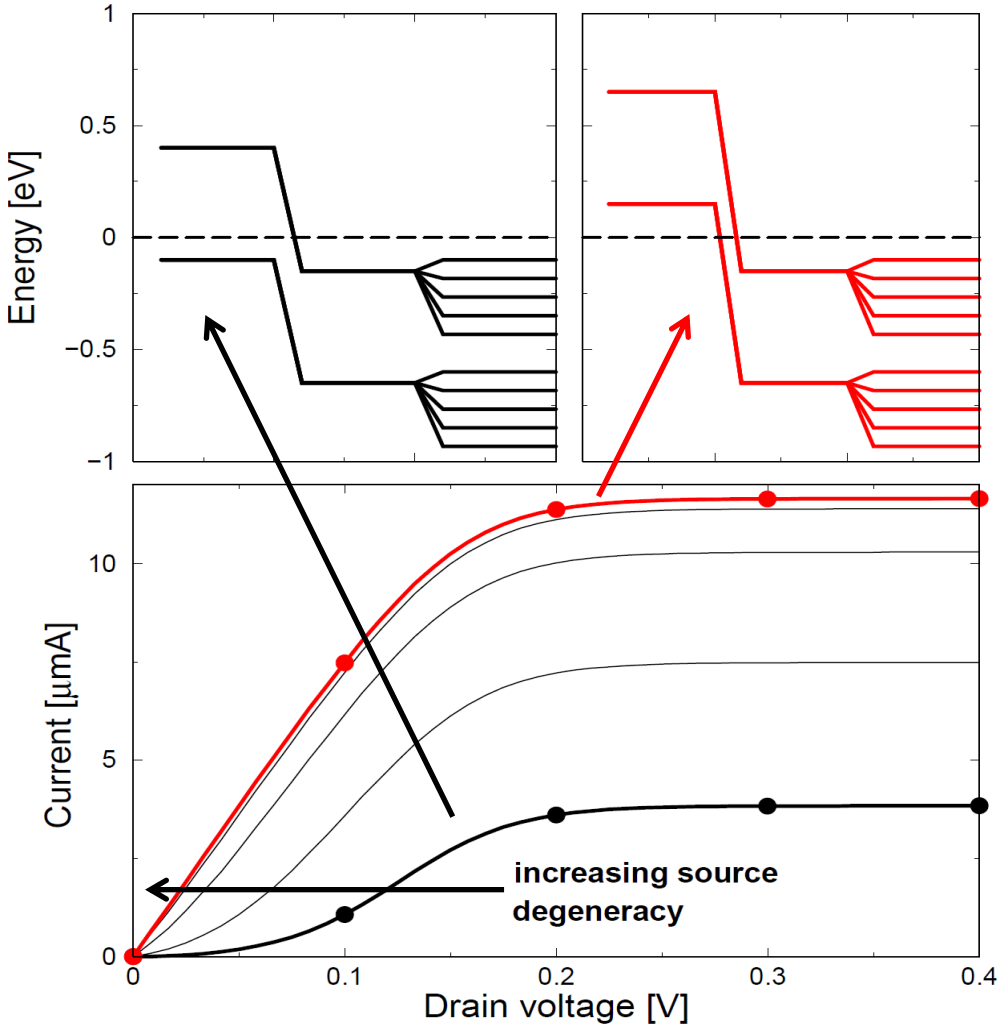
$$g_d = \frac{2q^2}{h} T_{sc} \left[f(\eta_{cd}^{(0)} - \mu_s) - f(\eta_{vs} - \mu_s) \right] \theta(\eta_{vs} - \eta_{cd})$$

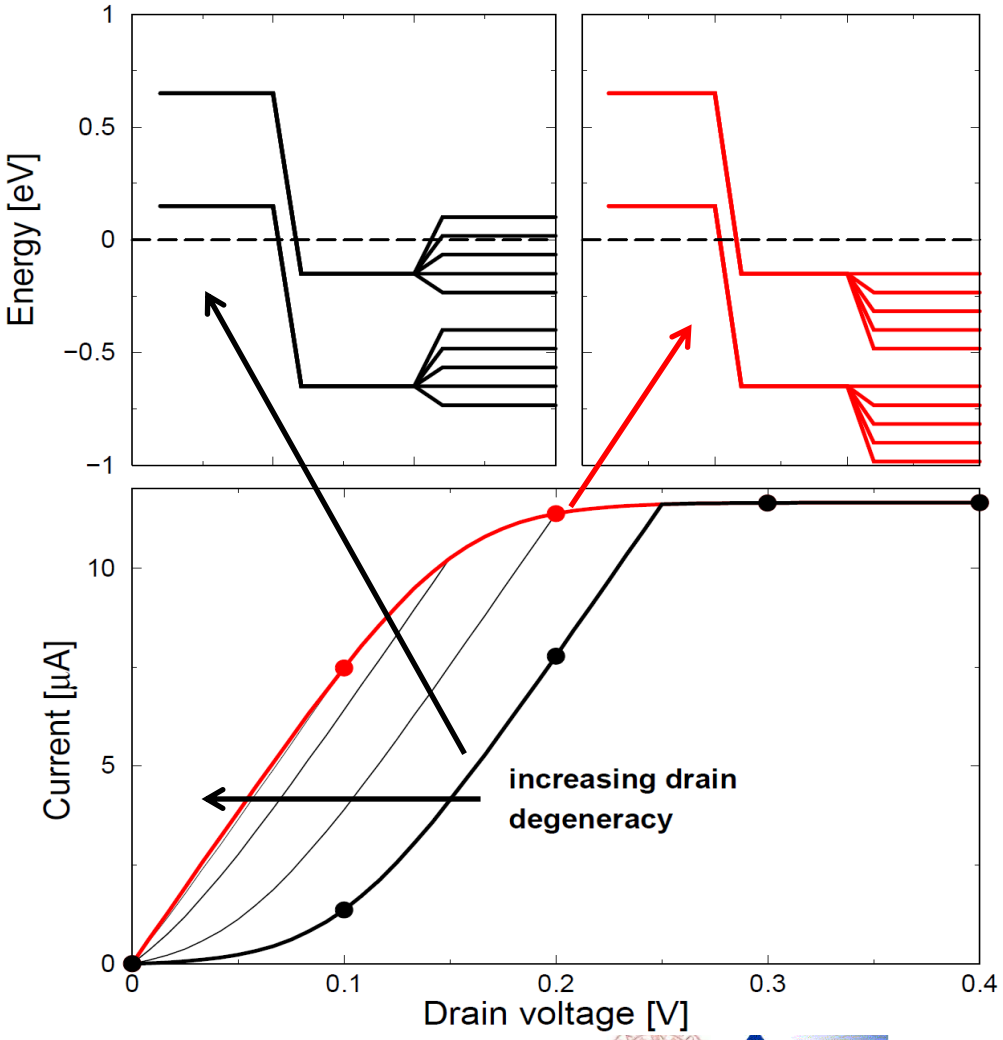
g_d can approach $(2q^2/h)T_{sc}$ if $\mu_s - \eta_{cd}^{(0)} \gg 1$ and $\eta_{vs} - \mu_s \gg 1$

- ➔ These conditions require that both the source and drain regions be heavily degenerate.
- ❑ If either the source or the drain are not degenerate, g_d drops down and may even fall close to zero if the two Fermi functions cancel out.
- ❑ Real devices typically exhibit thermal current so that the actual g_d will never be exactly zero.

Effect of source & drain degeneracies – I

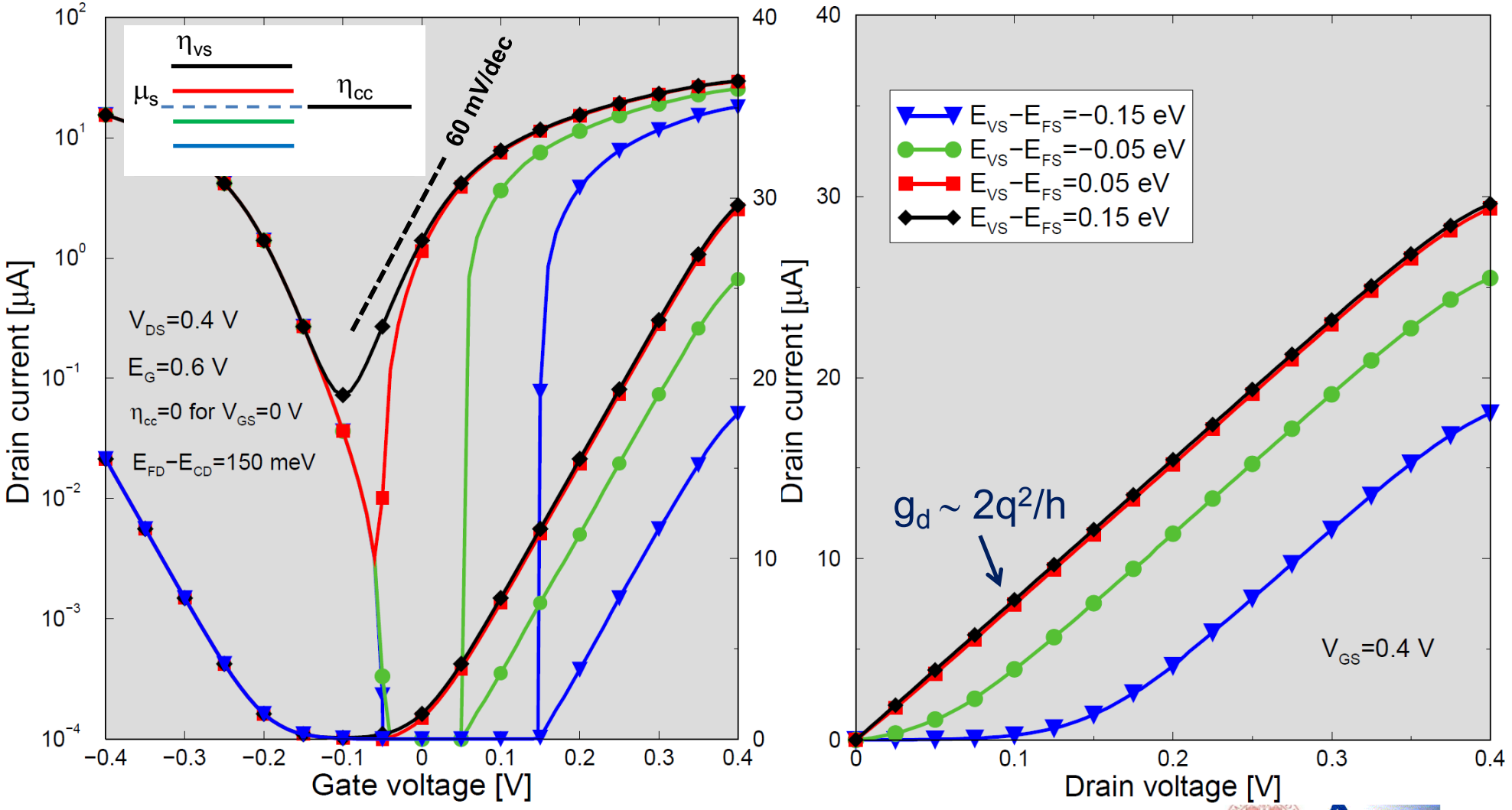
We assume T = 1 within the tunneling windows and T = 0 elsewhere





Effect of source & drain degeneracies – II

We assume T = 1 within the tunneling windows and T = 0 elsewhere



Device optimization

The device optimization can be achieved by selecting the semiconductor material, V_{DD} and source and drain doping densities

- High drain conductance at low V_{DS} → source and drain degeneracy levels at least at 3-4 k_BT.
  - we accept a 10% degradation of the drain conductance but enforce the current falloff at $V_{GS} = V_T - 3k_BT/q$.
- To prevent the ambipolar effect:

$$V_{DD} < E_G - (E_{VS} - E_{FS}) - (E_{FD} - E_{CD})$$

  - If we target a V_{DD} = 400 mV a minimum E_G of 0.6 V is needed.

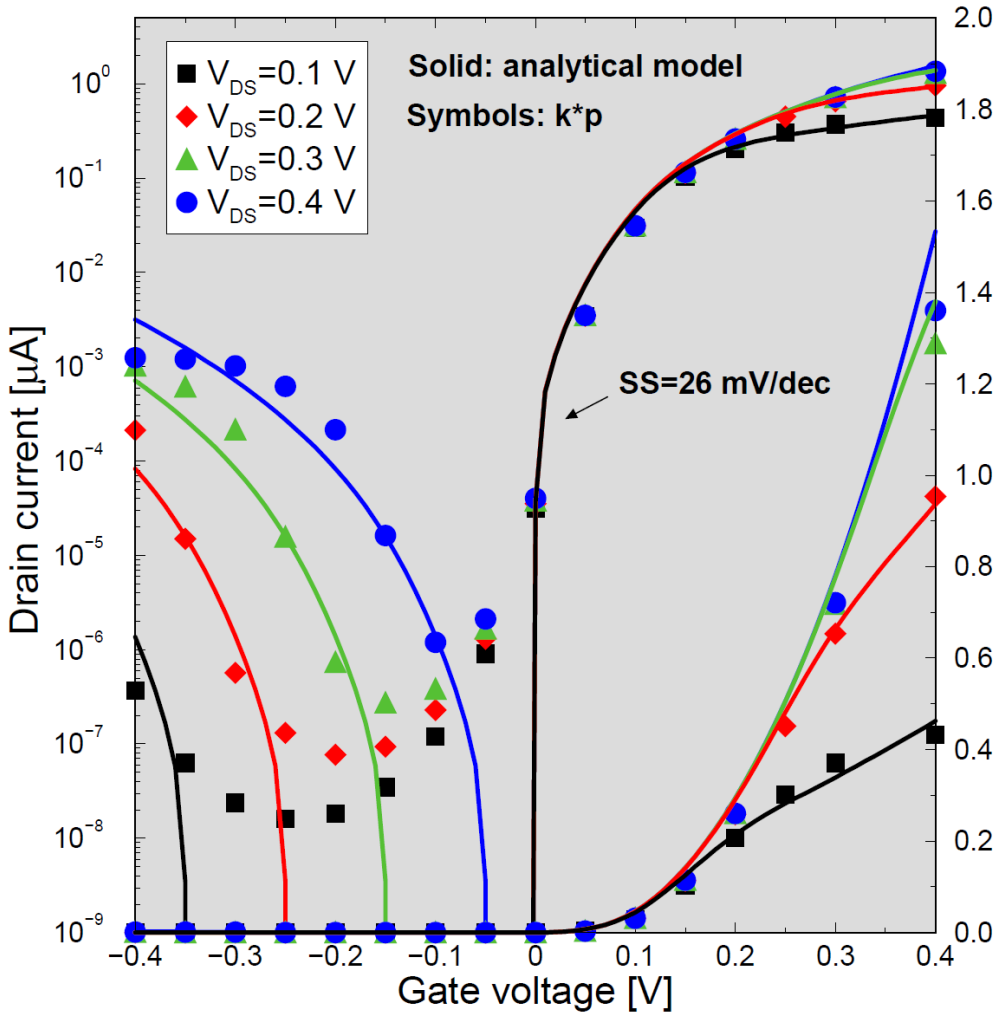
The choice of InAs is suggested by the small m* and E_G, which can be tuned to the desired value by a suitable choice of the NW size

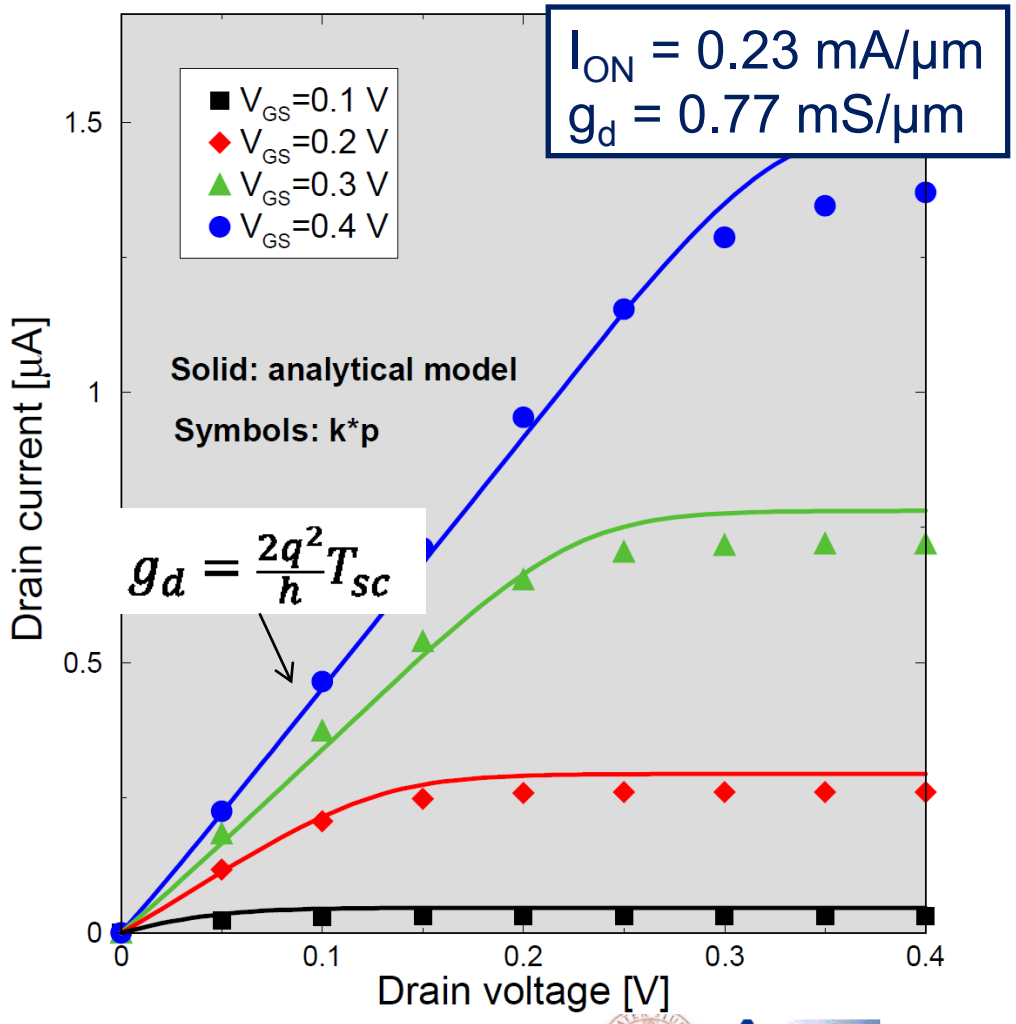
InAs n-type Tunnel FET

6x6 nm² → E_G = 0.614 eV

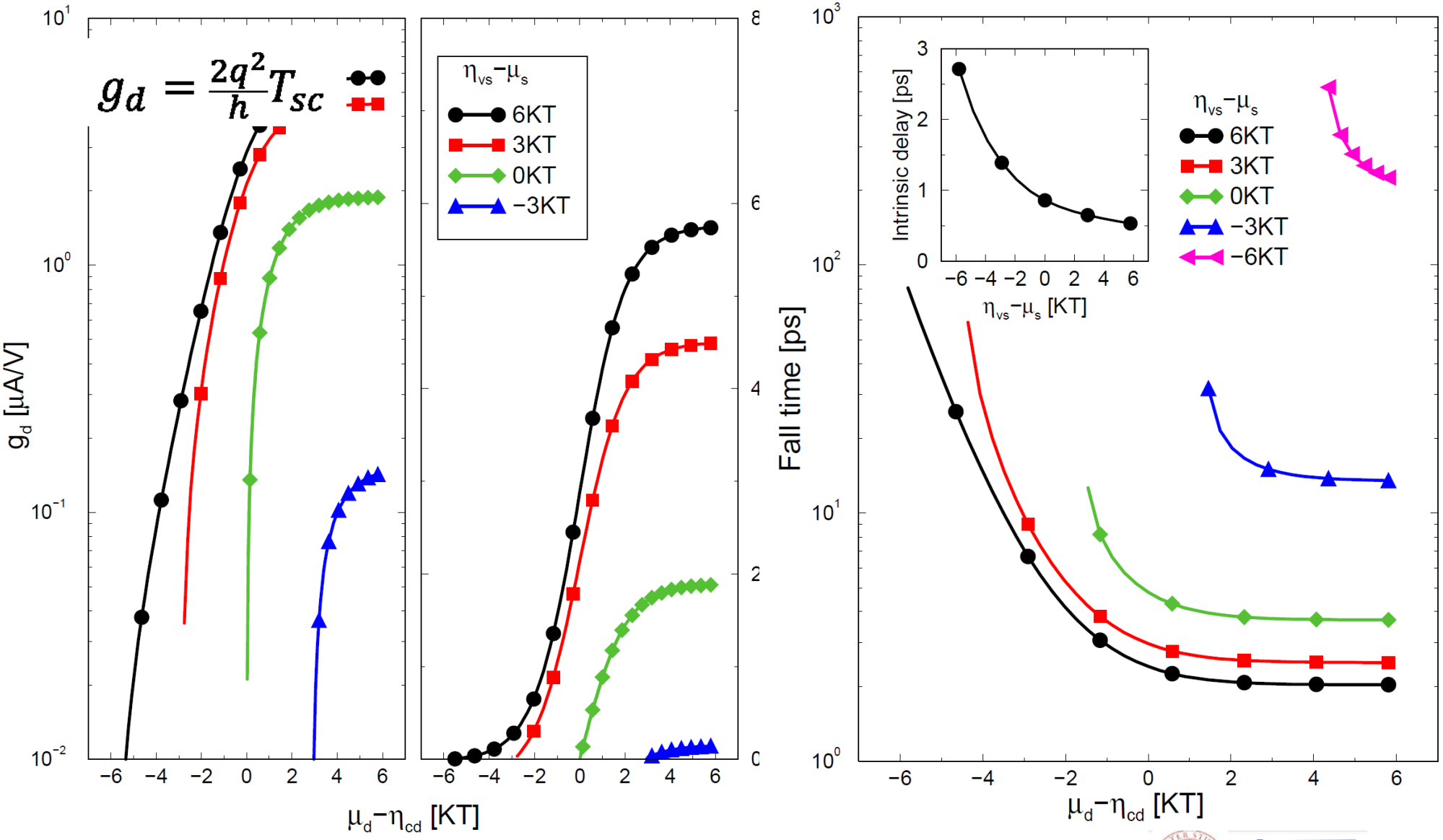
$E_{VS}-E_{FS}$ = 80 meV

$E_{FD}-E_{CD}$ = 90 meV

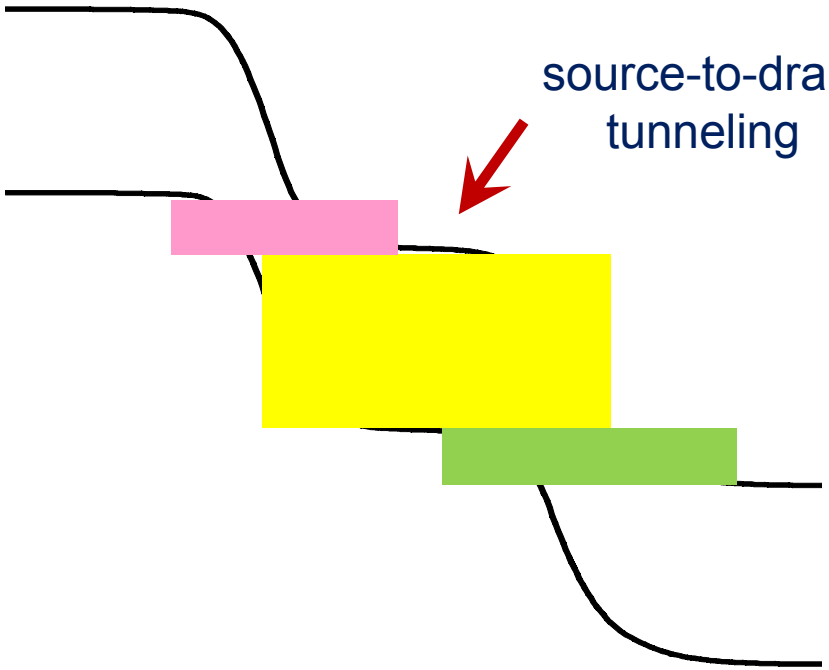


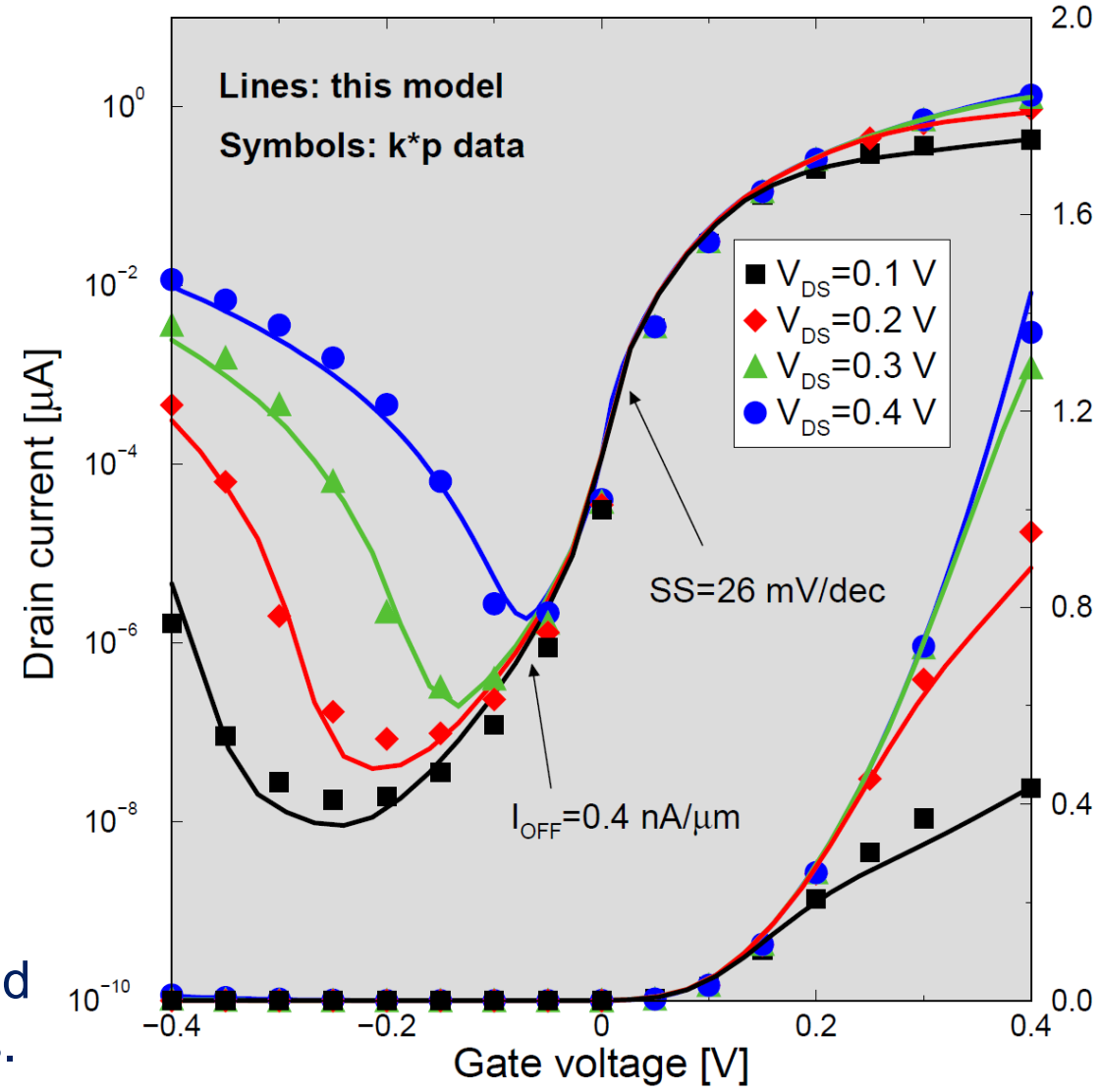


Output cond. & Fall time v.s. S/D degeneracy



InAs n-type Tunnel FET





- To fit the OFF-current → T_{sd}
- T_{sd} depends on the tunneling probabilities across the channel and source/drain space-charge regions.

Conclusions

- The problem of the small drain conductance in NW-TFETs is addressed with the help of an analytical model which makes it possible to work out an optimal device design.
- With a source and drain doping density such that $E_{VS} - E_{FS} = E_{FD} - E_{CS} = 3k_BT$ we achieve:
  - g_d as large as 90% of its maximum theoretical value;
  - SS = 26 mV/dec;
  - I_{ON}/I_{OFF} ratio much larger than 10^4, with I_{ON} = 0.23 mA/μm.
- The present study shows that the performance penalty of TFETs is entirely due to the small tunneling probability.
- An improvement in the tunneling probability can possibly be achieved by a suitably designed heterostructure TFET.