

HV MOS Modeling

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MOS – AK Böblingen

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a leap ahead

LDMOS Transistor Modeling "The Skeleton in the Cupboard" ?

- Many unsolved problems in HV MOS Transistor modeling
- Accuracy of HV SPICE models are not comparable to standard MOS



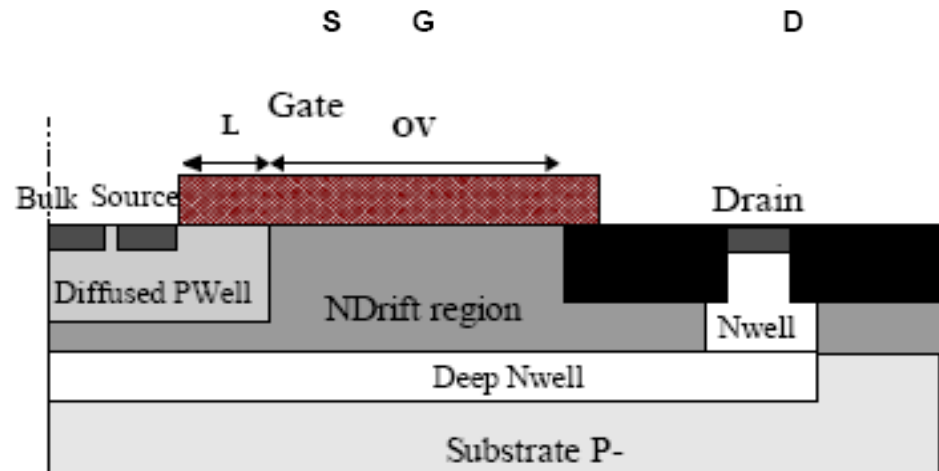
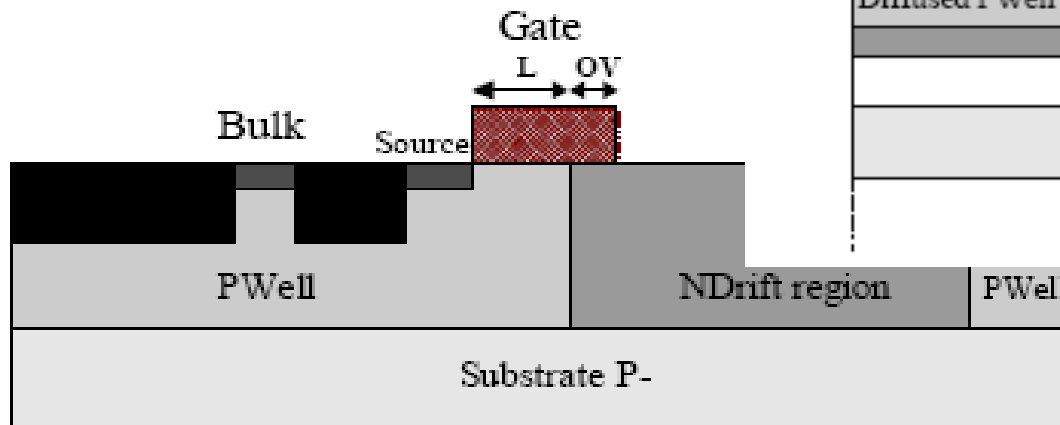
Different Devices and Requirement

RF LD MOS

- Accurate modeling of frequency dependency

Lateral HV MOS

Vertical HV MOS



Switching loss optimization of 20V devices integrated in a 0.13 μm CMOS technology for portable applications

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HV Transistor Model Requirements (first order)

- DC & AC characteristic
 - Scalability of W & L, Quasi-Saturation, drift region, Intr. Extr. Caps.
- Symmetrical and unsymmetrical, source & drain res and cap.
- Voltage up to 120V & Temperature behavior up to 180°C
- Physical parameter set (Statistical Corner & MC Modeling)
- Self heating effects
- Noise Modeling (1/f, thermal, (gate induced))
- Simple and comprehensible parameter extraction.

HV Transistor Model Requirements II

- Capable of creating statistical models
- Substrate current modeling
- Transient behavior RF characteristics (in a limited subset of applications)
- Parasitic modeling (parasitic bipolar, body diode recovery)
- Breakdown characteristics
- Scalable over the drain extension length.

Model Solutions

Sub-circuits (Macro model):

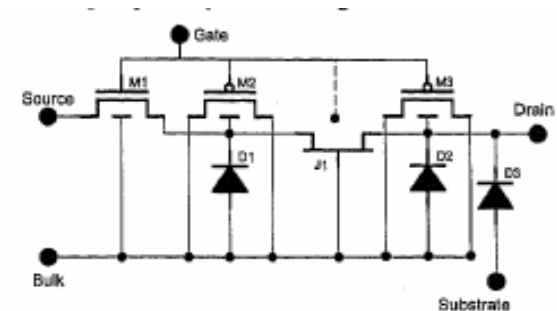
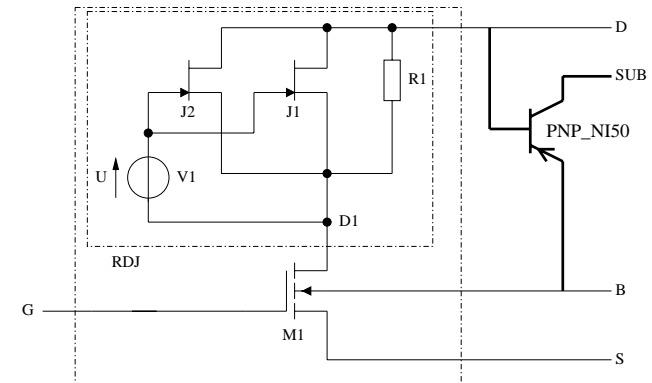
- Compatible to all simulators
- Higher simulation time, convergence

Compact Model with internal node:

- Node solved internally or from the simulator
- Higher simulation time, convergence

Compact Model:

- Combination of the low voltage MOS region with the high voltage drift region without internal node.
- Short computation time



An Improved LDMOS Transistor Model That Accurately Predicts Capacitance for all Bias Conditions

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SYNOPSYS- HSPICE level 66

Press Release

Synopsys' HSPICE High-Voltage MOS Transistor Model Adopted by UMC

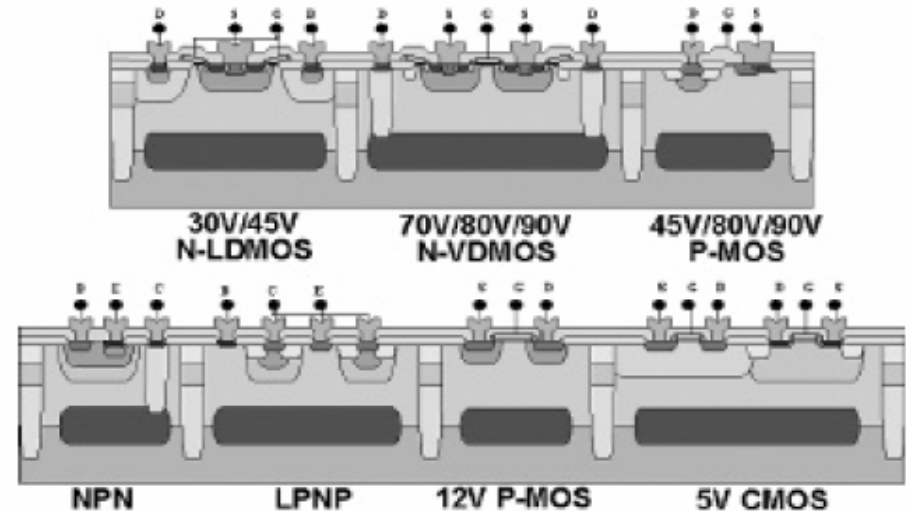
Strength of our level 66 HVMOS

- a) a global model for high V_{gs} and low V_{gs} at the same time
- b) easier to extract the model card and easier to verify
- c) much more accuracy with BSIM-4 based methodology

-Level 66 is not public domain

BCD (Bipolar CMOS DMOS) means more than LDMOS

- N-LDMOS
- N-VDMOS
- P-MOS
- HV NPN, PNP
- Lateral PNP, NPN
- 5V, 12V, 20V, 50V, 80, 120v,
- HV characterization of passives
- High temperature modeling for Automotive applications
- HV modeling of the parasitics



Roadmap Differentiation and Emerging Trends in BCD Technology

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CMC Activities

- The CMC is in fact beginning to look into standardization of HV MOS models.
- Yutao Ma of Cadence is leading this effort which is just getting underway.