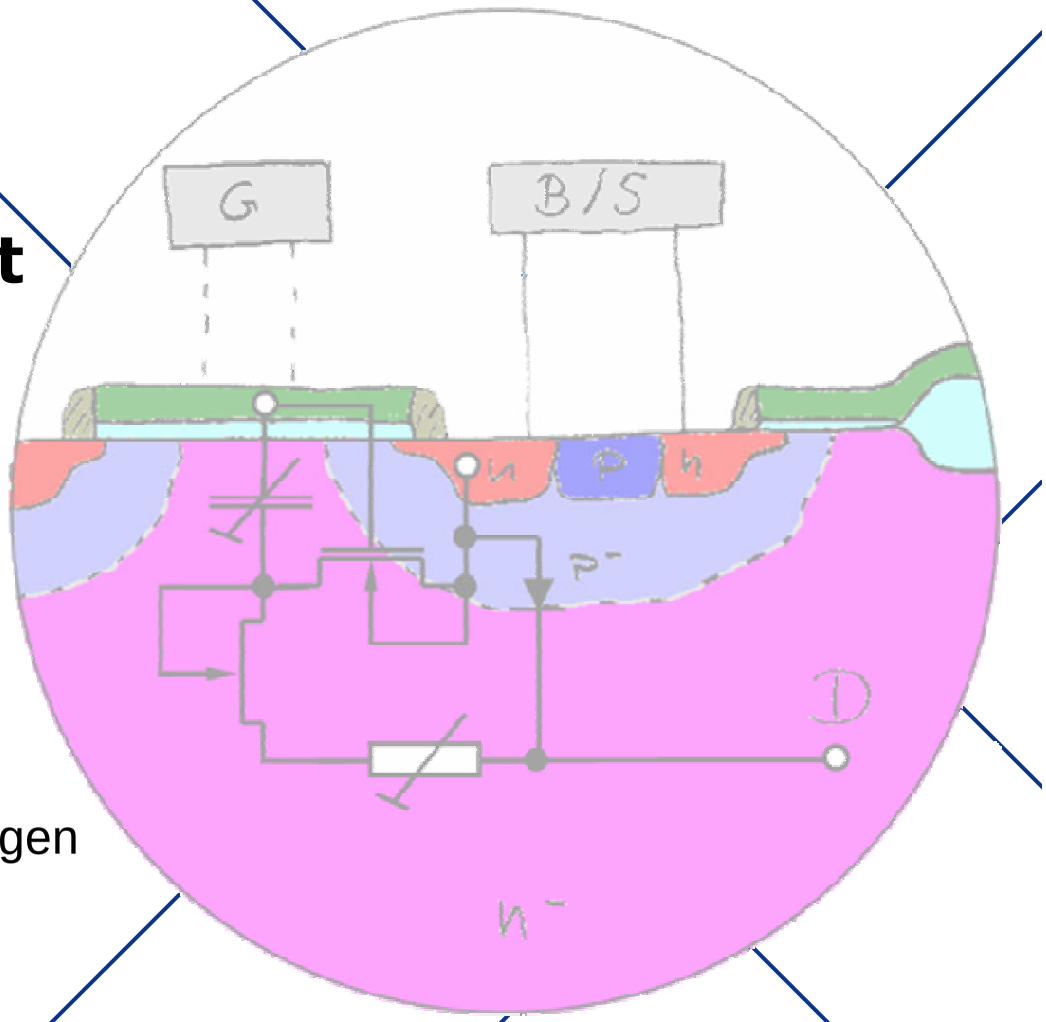
X-FAB SEMICONDUCTOR FOUNDRIES

Lumped Element High Voltage MOS Model



presented by
Sebastian Schmidt
at MOS-AK / Böblingen

March 2006

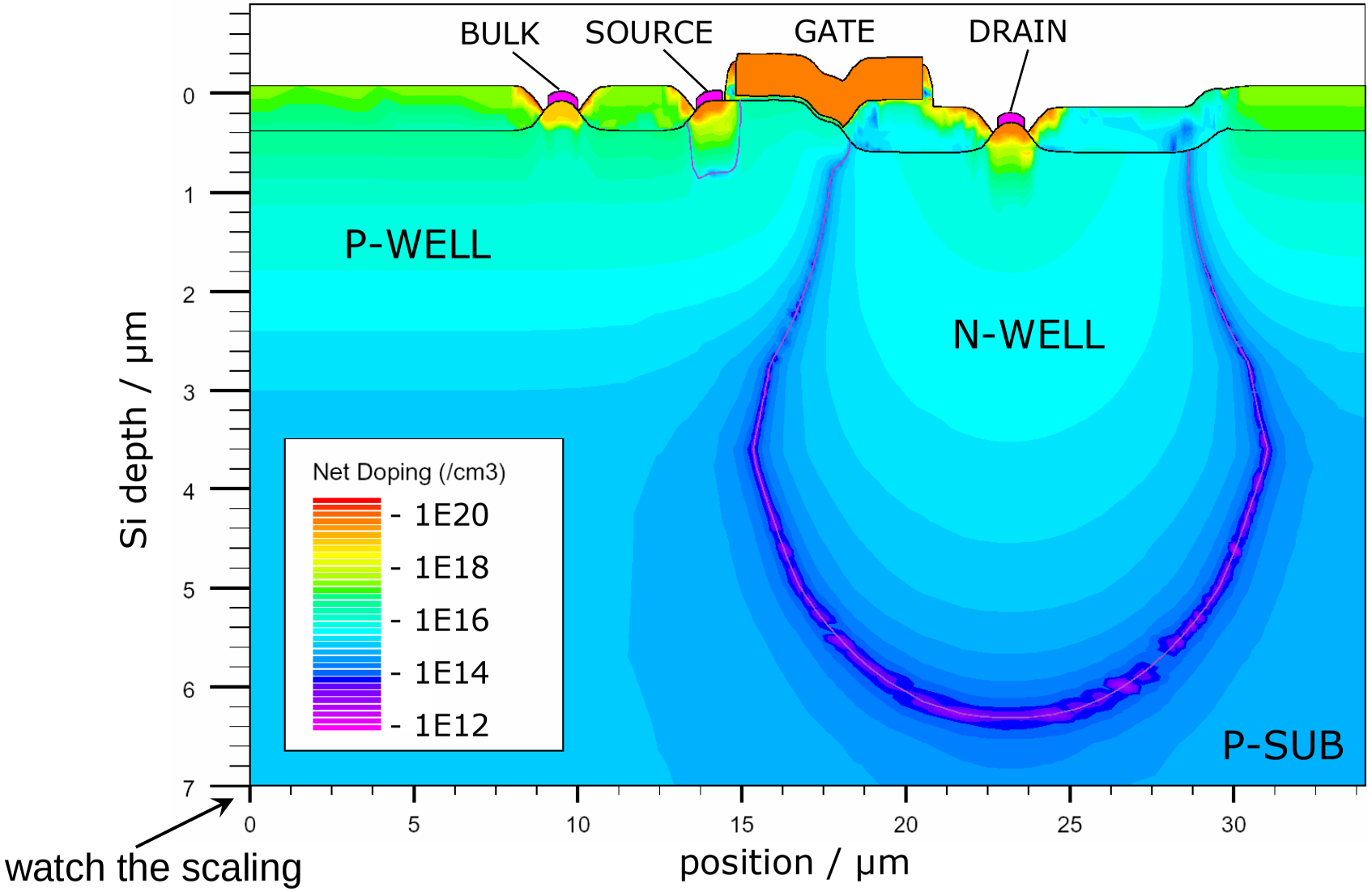
Agenda (1)

- The Devices:
  Types and Construction
- DC Model:
  Mathematical considerations, types
- AC Model:
  Non diode variable "gate" capacitance
- Ring Oscillator Test Bench:
  A challenge for the simulator
- Outlook

Introduction

- The goal is to show an extension to the BSIM3v3 model which can be simulated by a standard Spice simulator.
- At the time of development a VerilogA formulation was not intended.
- The model shows a more accurate description of the so called quasi saturation effect.
- A better description of the LDDMOS drain overlap capacitance is considered.

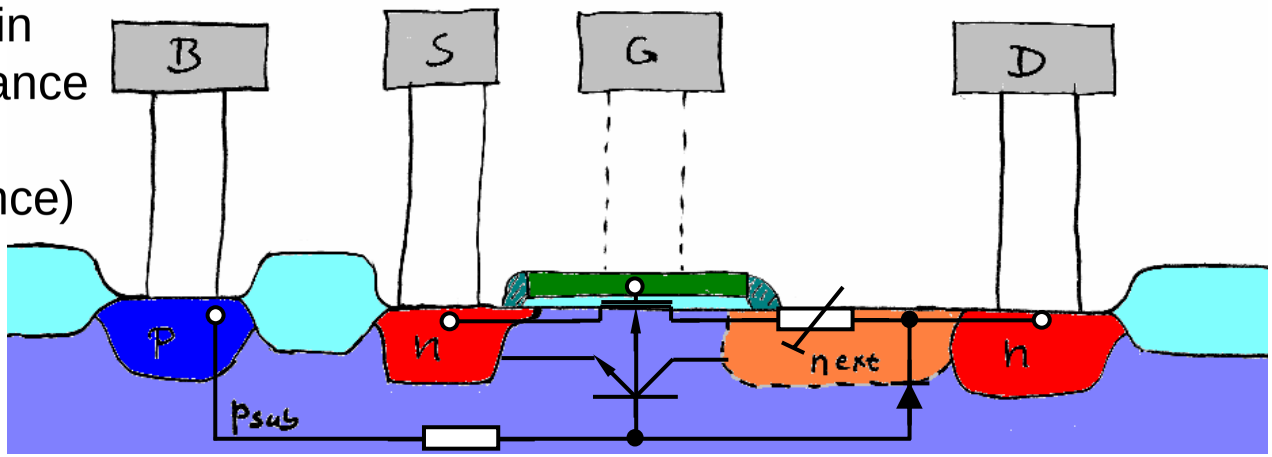
High Voltage Drain Extension MOS Cross Section

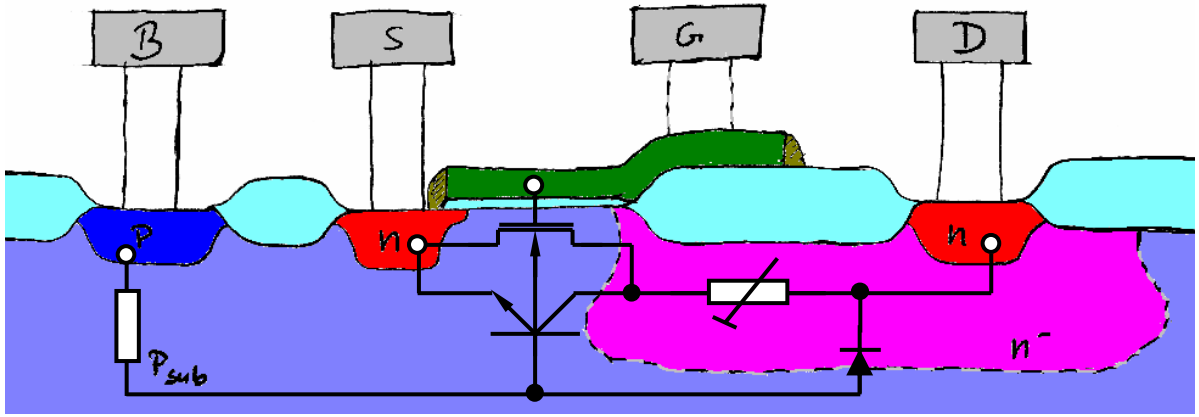


Two Types of Drain Extension MOS

Extension region at drain
Circuit with drain resistance and parasitic elements (BJT, substrate resistance)

Name:
Extended Drain MOS
XDMOS



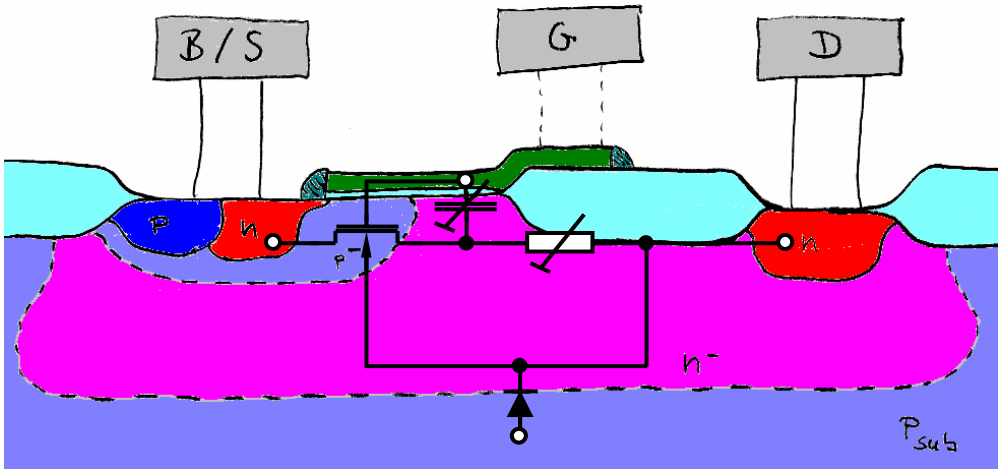


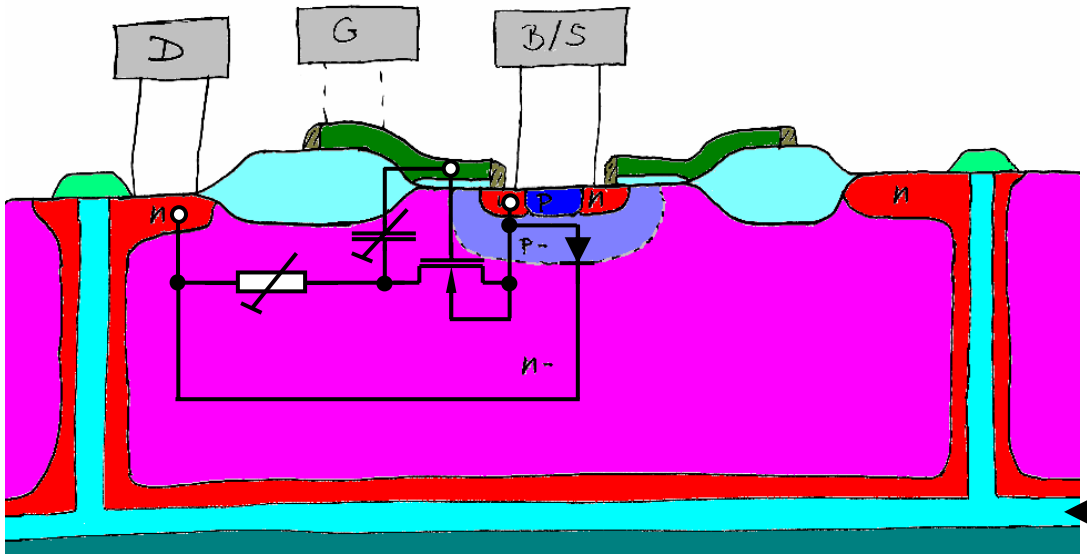
N-Well as drain extension

Two Types of Lateral Diffused Drain MOS

Diffused drain with
lateral drain connection

Name: LDDMOS
or LDMOS





Diffused drain with
vertical drain connection

XD_10 with up to 650 V
LDMOS transistors

Trench

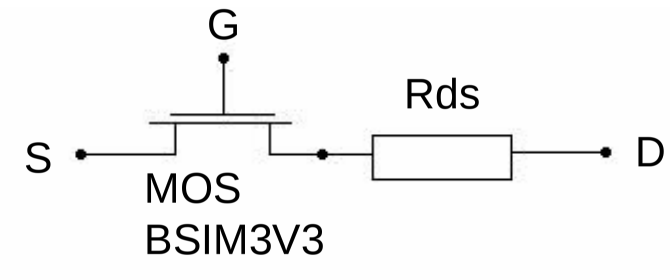
Agenda (2)

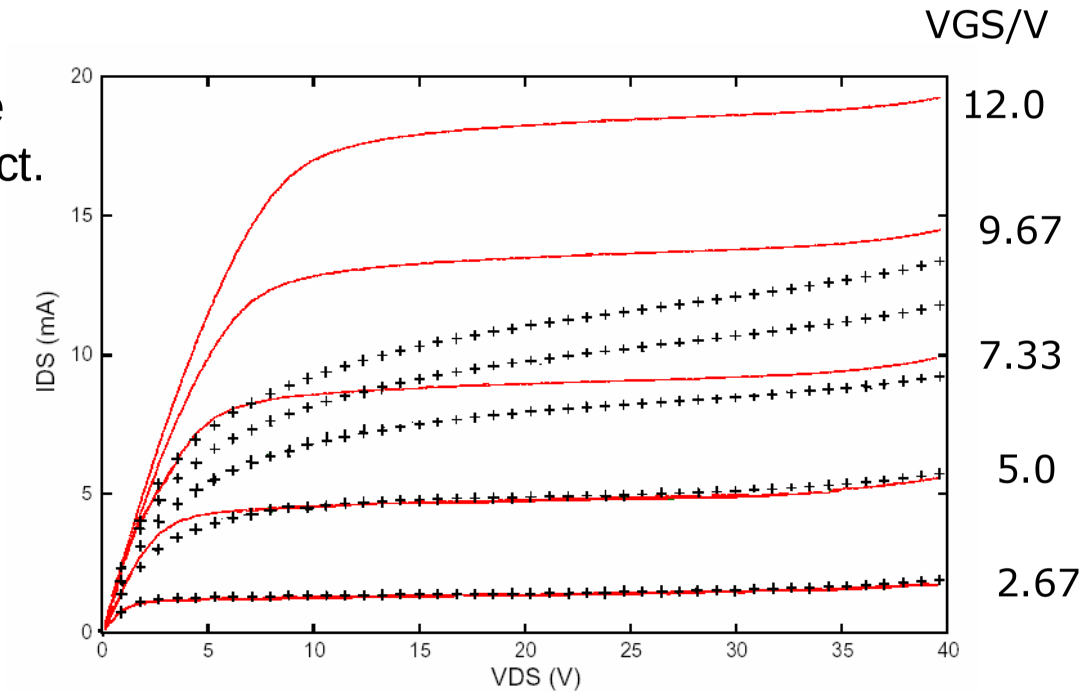
- The Devices:
  Types and Construction
- **DC Model:**
  Mathematical considerations, types
- AC Model:
  Non diode variable "gate" capacitance
- Ring Oscillator Test Bench:
  A challenge for the simulator
- Outlook

First Generation HV MOS Model

> MOS transistor with serial resistor

The model does not take into account the quasi saturation effect.



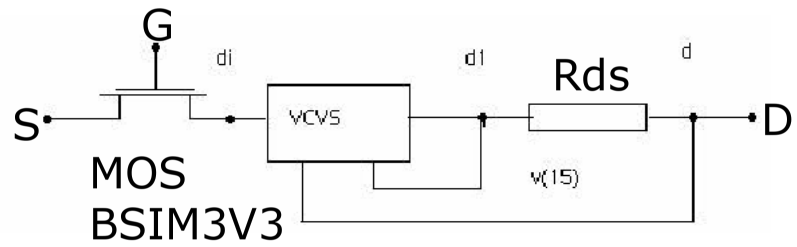


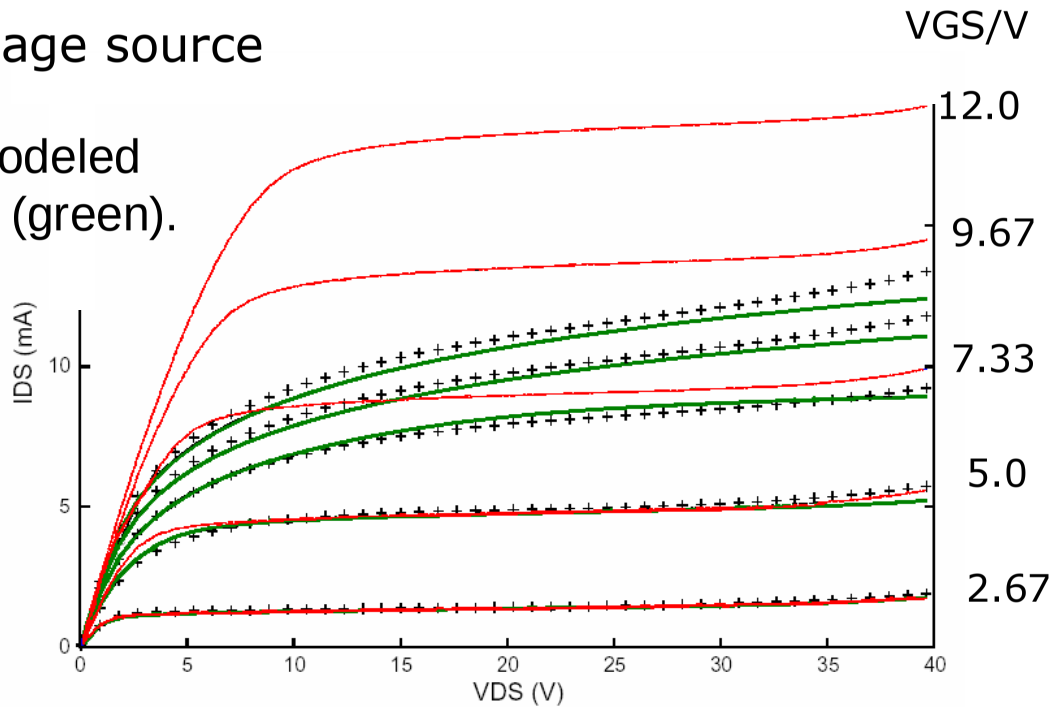
- good model accuracy for low gate voltages
- drain current saturation effect at high VGS and VDS not included
- fast simulation speed and good convergence

Second Generation Behavioural HV MOS

> MOS transistor with serial resistor and voltage controlled voltage source

The quasi saturation is modeled with acceptable accuracy (green).

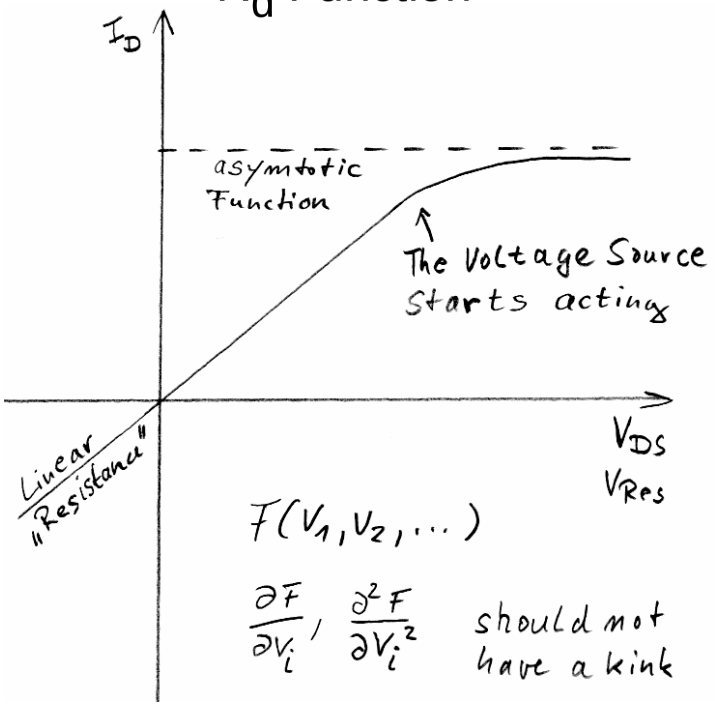


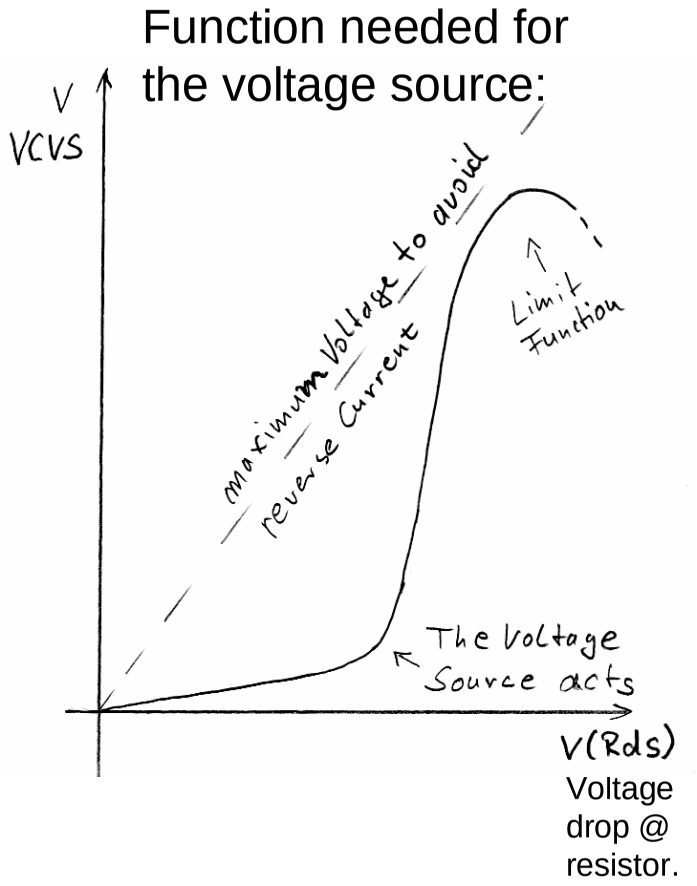


- core devices MOS and Rds identical to HV model
- several parameters for VCVS added
- good model accuracy, error less than 10%
- higher simulation time
- simulation convergence problems more likely

Function Requirement for the Voltage Source

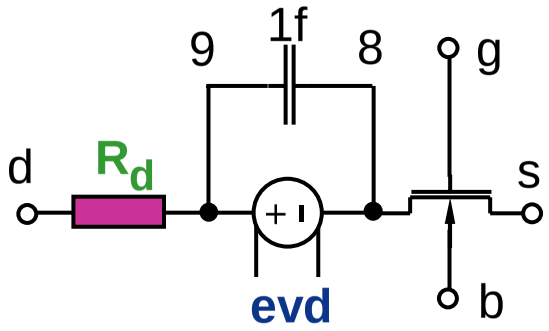
- Demands on the behavioral current function:
  - The function should be monotone (not necessarily).
  - The first and second derivative must be continuous.





Implementation: Controlled Voltage Source

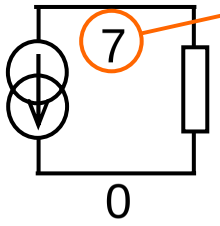
> Improved accuracy has its price:
3 auxiliary networks, 7 parameters, several additional elements



evd = max(sgn(v(d,s)),0) * max(sgn(v(g,s)),0) * min(v(7)*v(6),v(d,s))

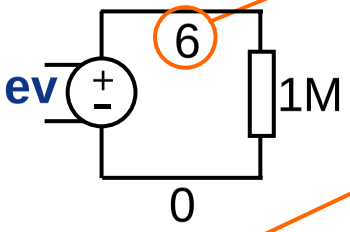
> Auxiliary Networks:

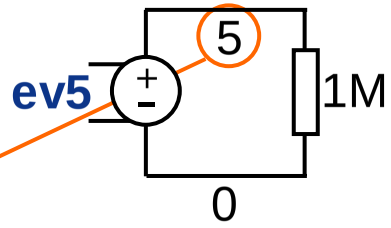
TC network



R=1k
tc1=5.5E-3
tc2=1.2E-5

main formula



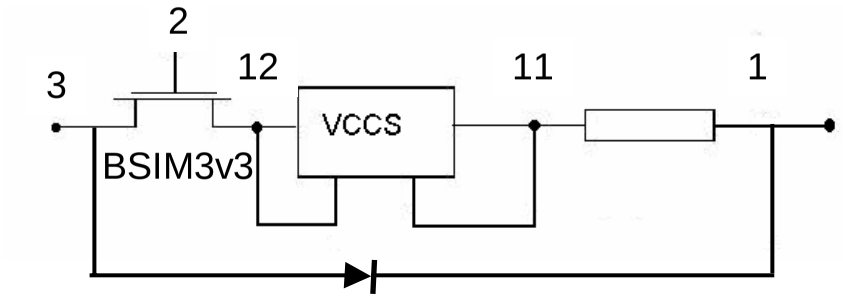


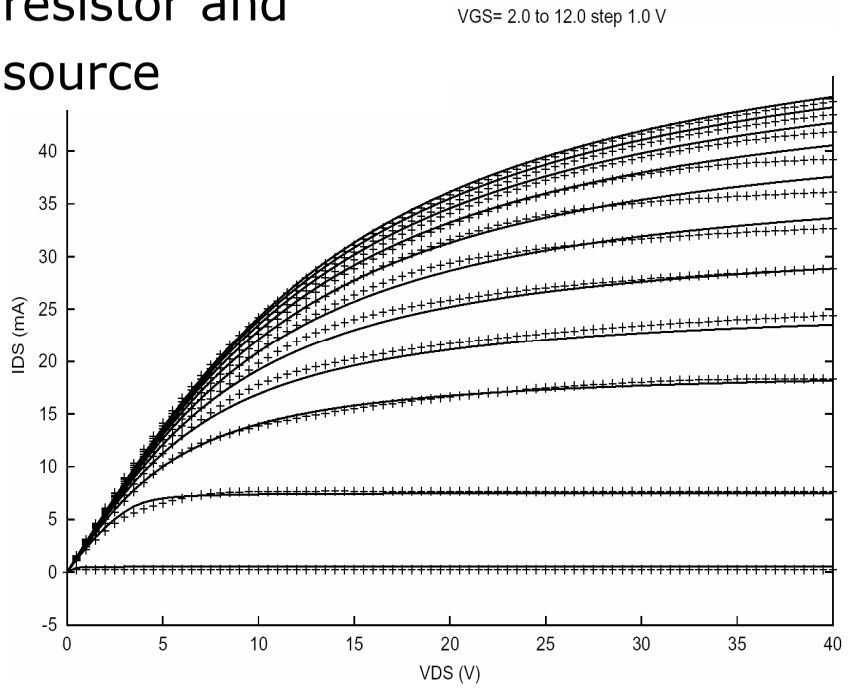
ev5 = **v(d,9)** / (v(7) + 1E-6)

ev = (kp3 v(5)^3 + kp4 v(5)^4 + kp5 v(5)^5) * **f**(v(g,s),k1h,kgs) * $\mathbf{f_{limit}}$(v(d,s),kds)

Current Source Behavioural HV MOS

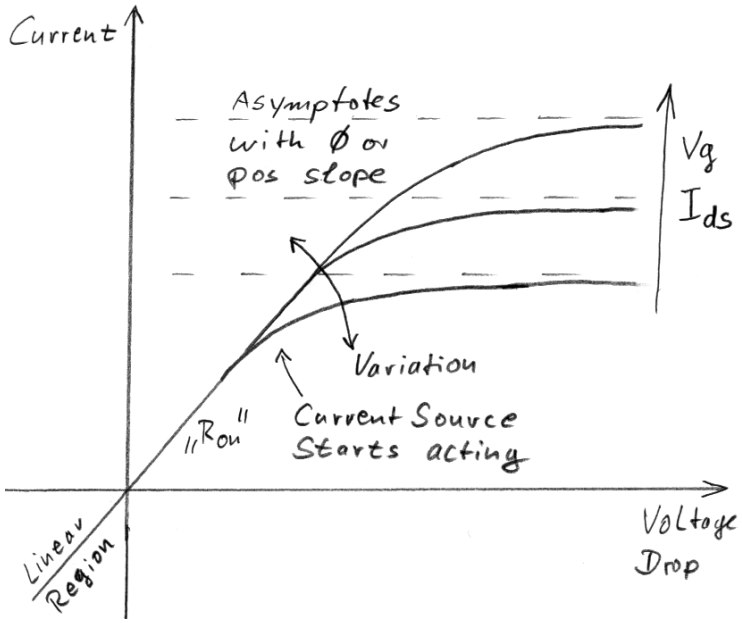
> MOS transistor with serial resistor and voltage controlled current source





- core devices MOS and Rds identical to HV model
- added fly back diode due to device construction
- improved accuracy compared to the voltage source model
- shorter simulation time
- capacitance modeling difficult in case of LDDMOS

Function Requirements for the Current Source

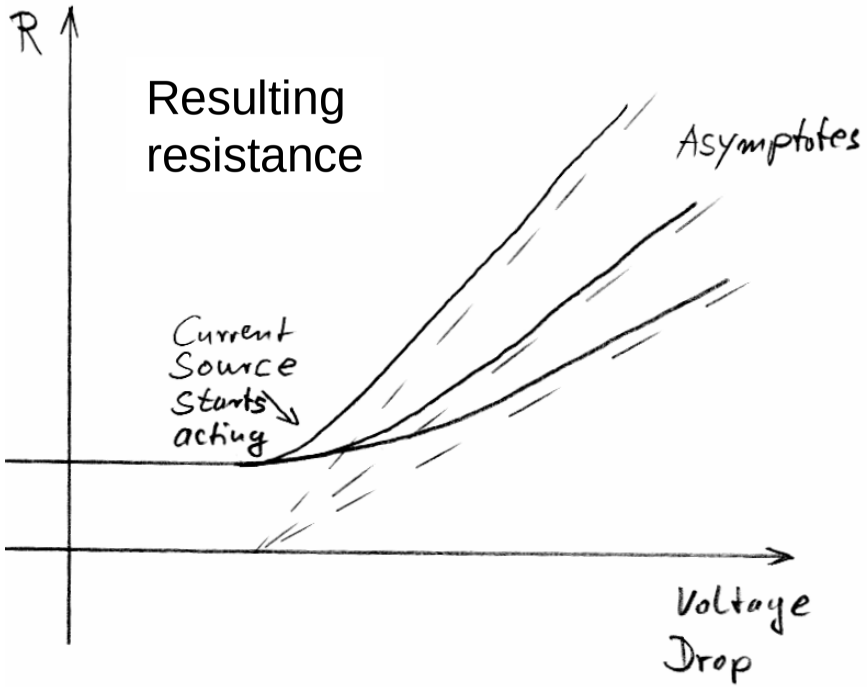


The function for the current in the drain extension region

$$F(V_1, V_2, \dots)$$

$$\frac{\partial F}{\partial V_i}, \frac{\partial^2 F}{\partial V_i^2}$$ must not have a kink

Variations ...



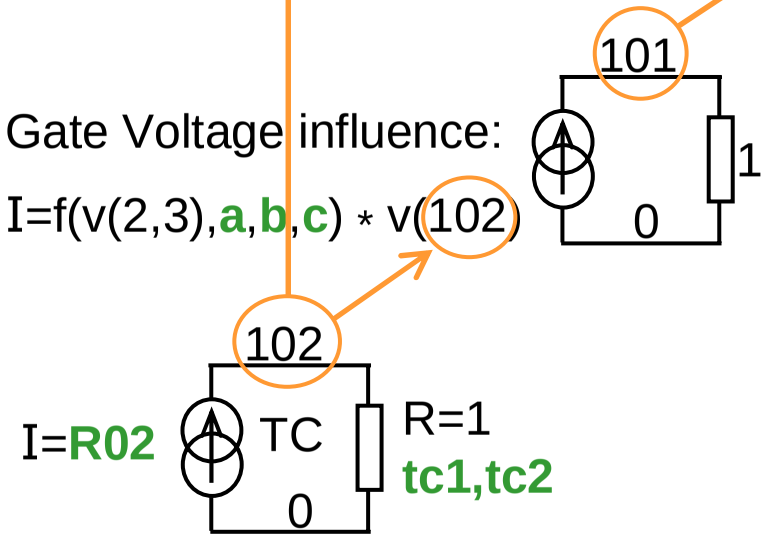
Behavioural Current Source Model

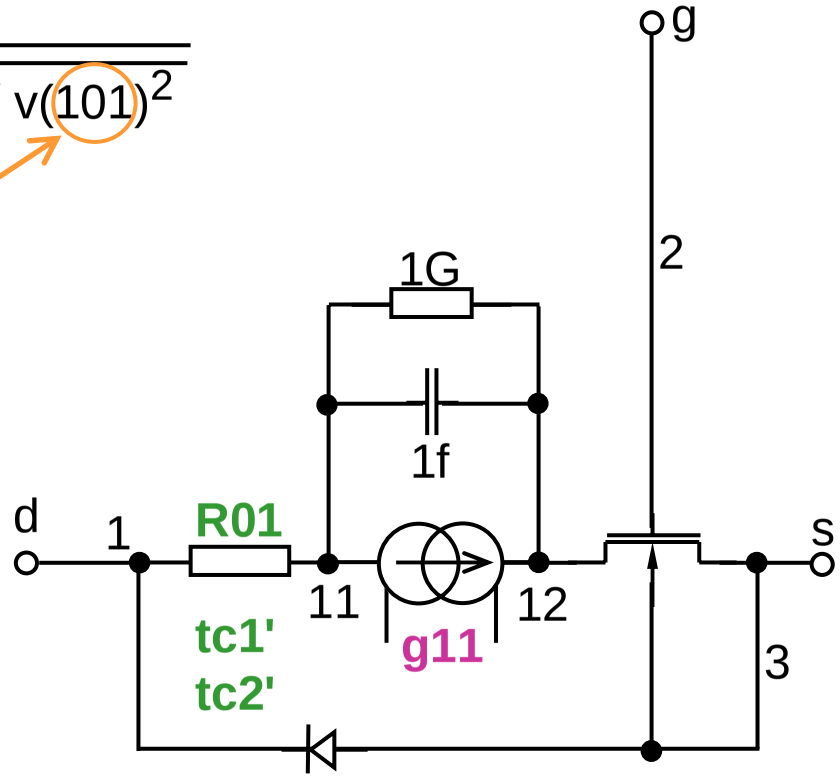
- Less auxiliary sources, improved TC modeling.
- More compact model, all effects in a few equations.
- Improved convergence, fewer parameter (5).

$$I(g11) = \frac{v(11,12)}{v(102) * 1 + \sqrt{1 + v(11,12)^2 / v(101)^2}}$$

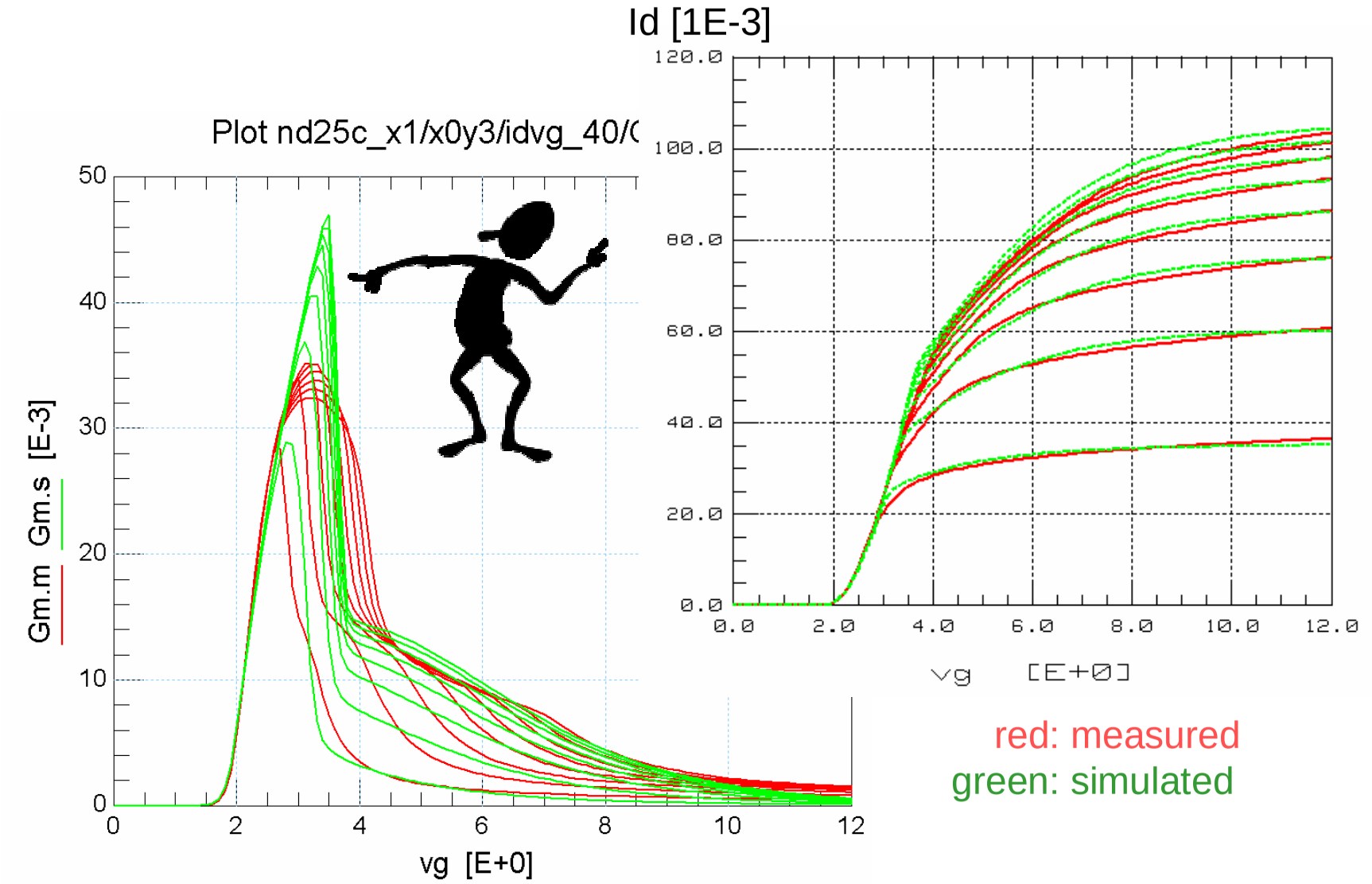
Gate Voltage influence:

I=f(v(2,3),a,b,c) * v(102)



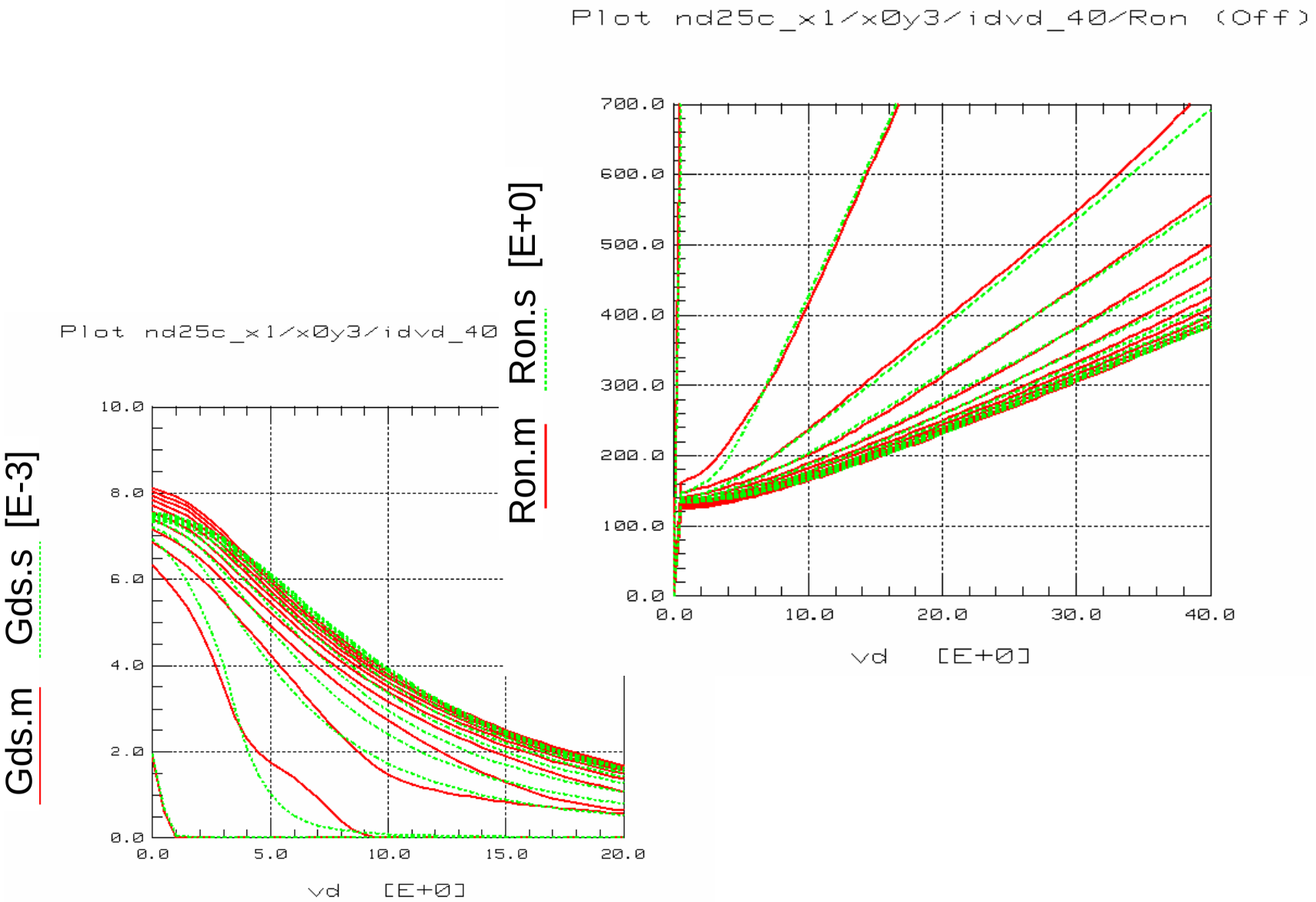


Gm and Transconductance Example



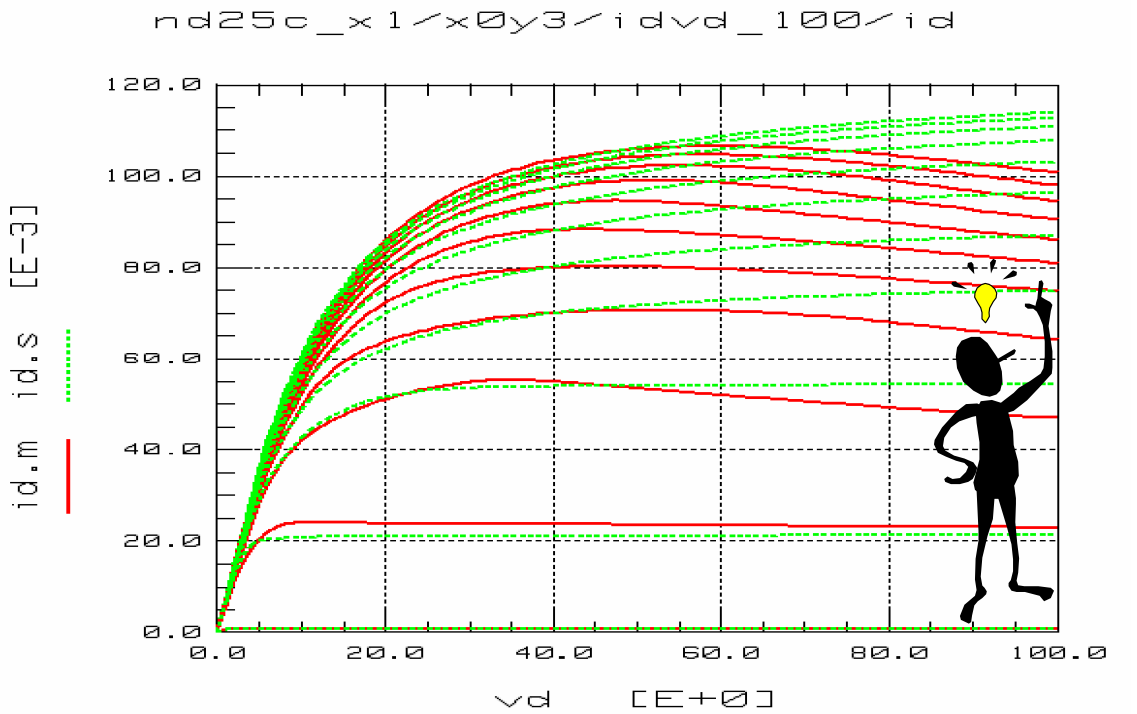
red: measured
green: simulated

Gds and Ron accuracy



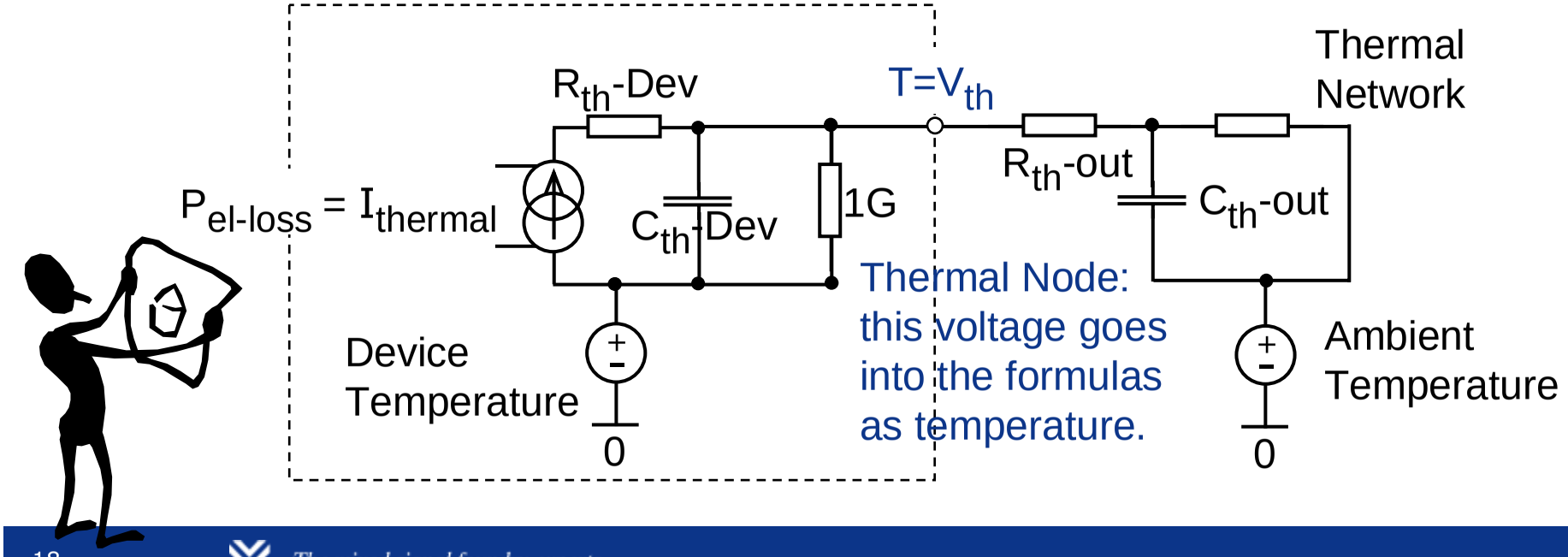
Self Heating

- The below plot shows clear self heating:
  a "falling" current trace in the saturation region
- To include this effect into the model, it needs a
  temperature node and additionaly ...
- A thermal resistance / capacitance network.
  It's not yet implemented in the model.



Introduction to Self Heating

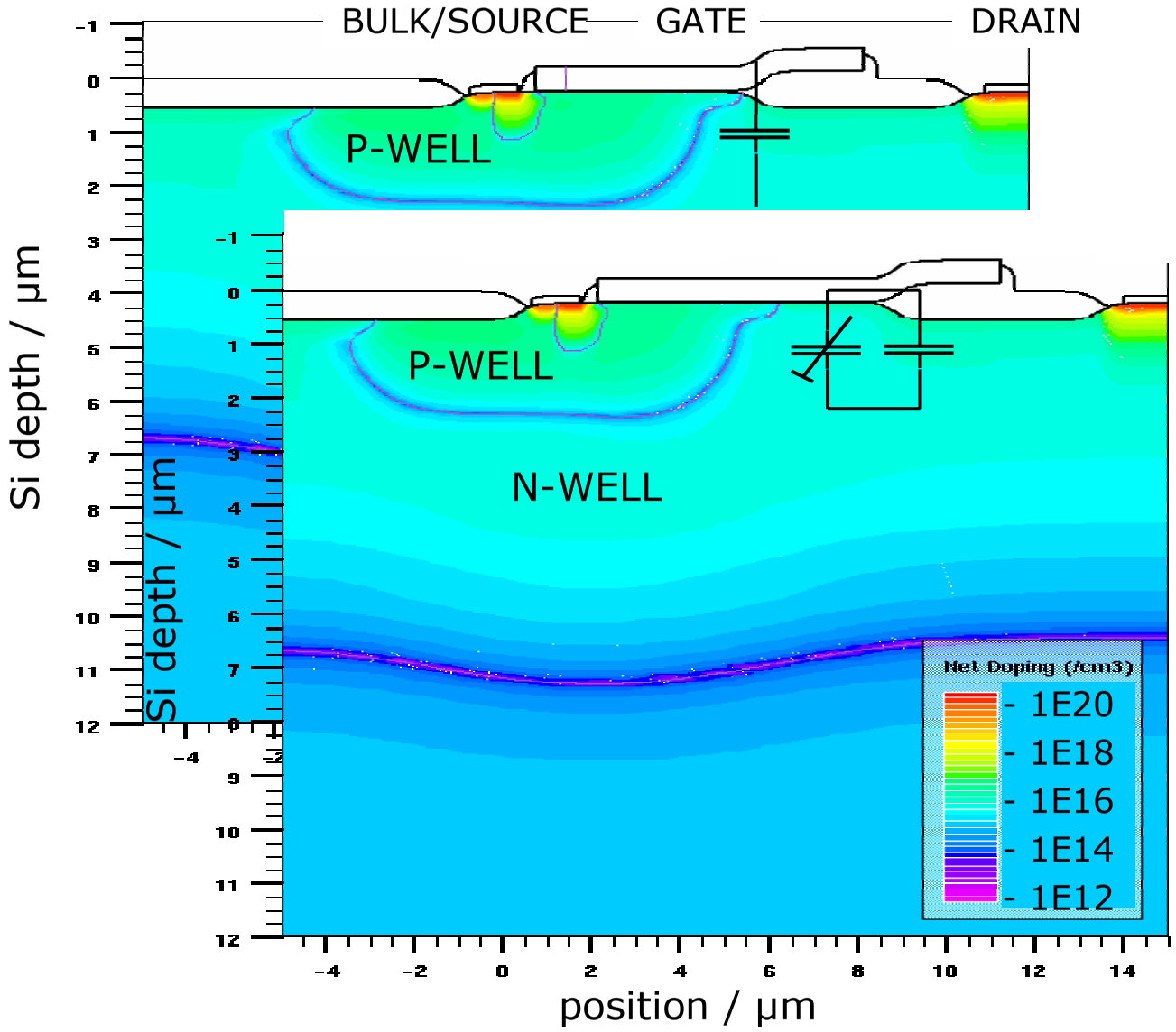
- Simple thermal network added for self heating:
  - Voltage [V] ≙ Temperature [K]
  - Current [I] ≙ Thermal Current [J/s=W]
  - Resistance [Ω] ≙ Thermal Resistance [K/W]
  - Capacitance [C/V] ≙ Thermal Capacitance [J/K]
  - Charge [C] ≙ Energy [J=Ws]
- The thermal power equals the electrical power loss.



Agenda (3)

- The Devices:
  Types and Construction
- DC Model:
  Mathematical considerations, types
- **AC Model:**
  Non diode variable "gate" capacitance
- Ring Oscillator Test Bench:
  A challenge for the simulator
- Outlook

The Drain Overlap Capacitance Problem



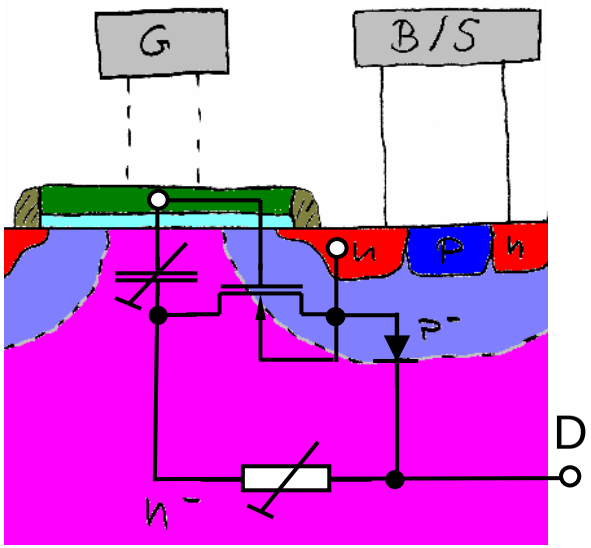
A capacitance, which depends strongly from the drain voltage, develops if the gate overlaps the drain extension region.

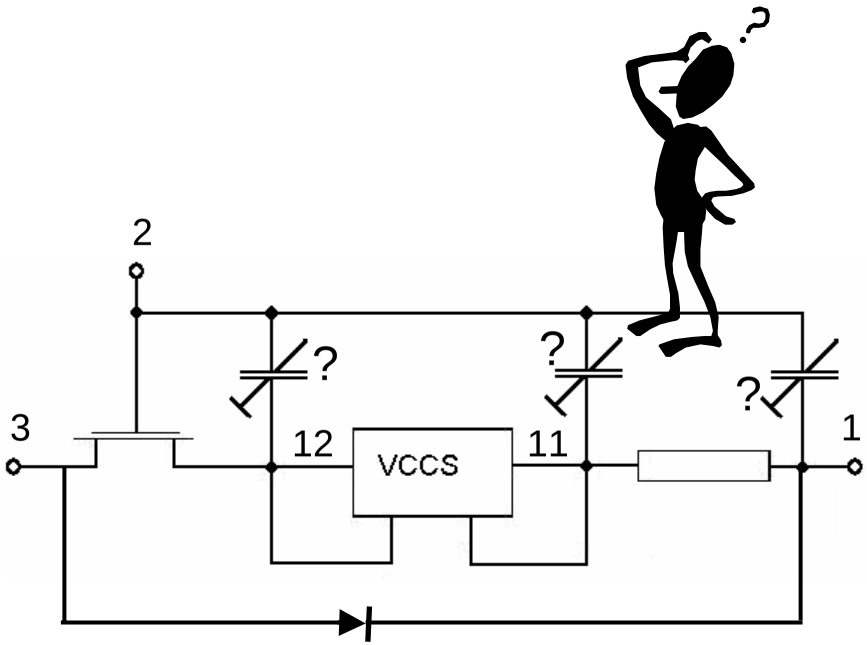
This is true for the LDDMOS type MOS with Trench isolation.

Fortunately it does not occur in the standard CMOS technologies, e.g. xc06.

LDDMOS Capacitance Model

- For the LDDMOS of the XD?10 technology a (variable) capacitance has to be added in the drain to gate path.
- It can not be decided by CV measurement which node has to be occupied to get a good fitting transient respond.

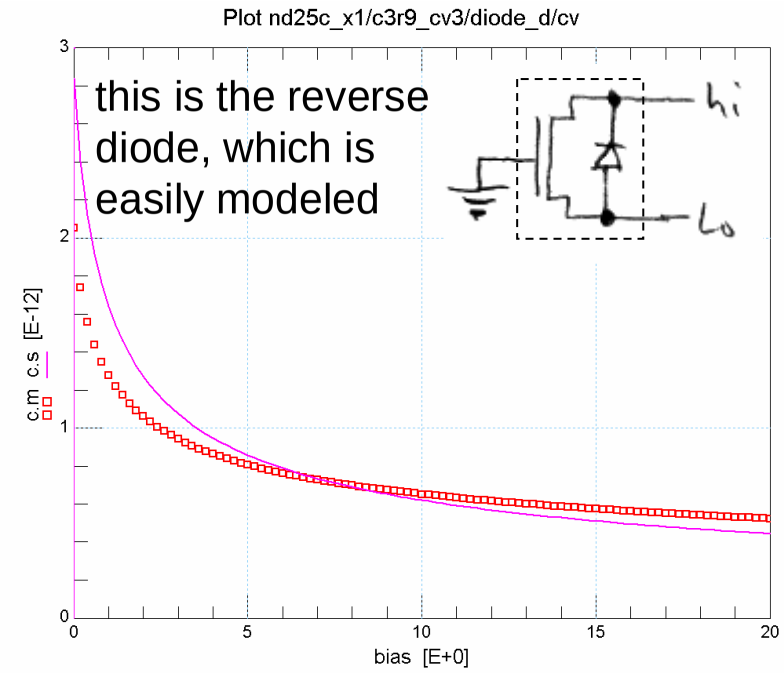


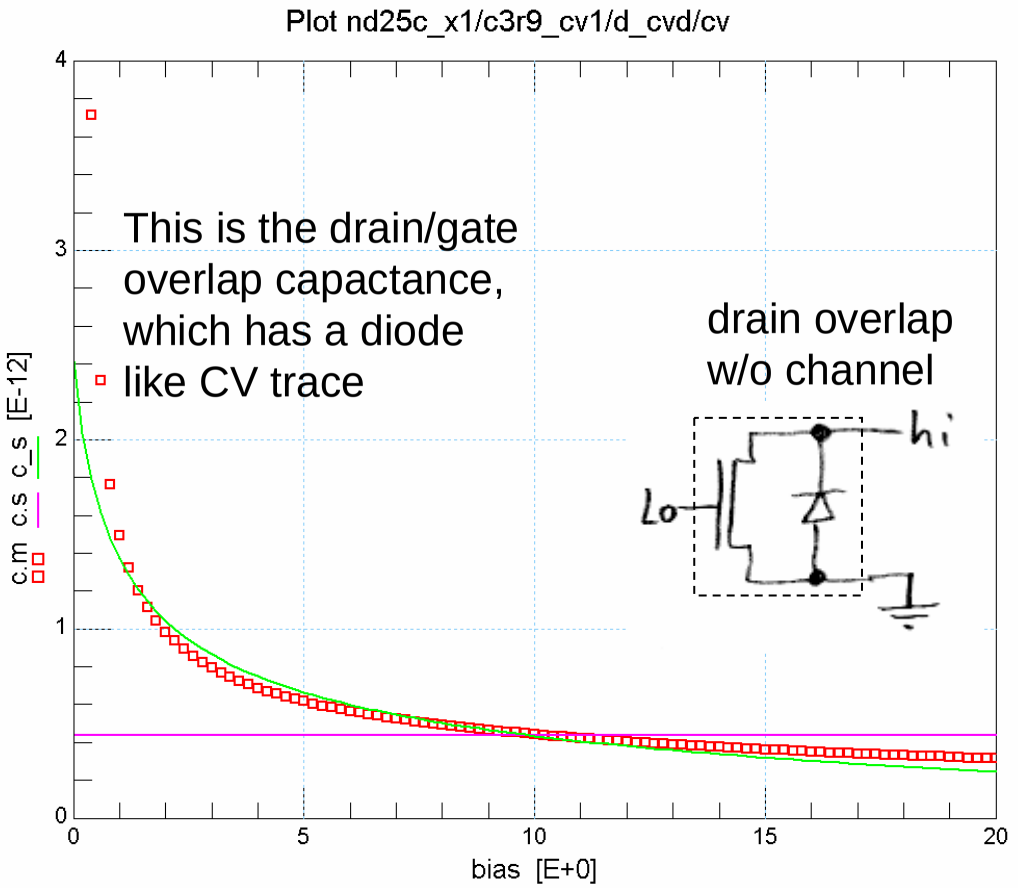


BSIM3v3

Improved CV Model

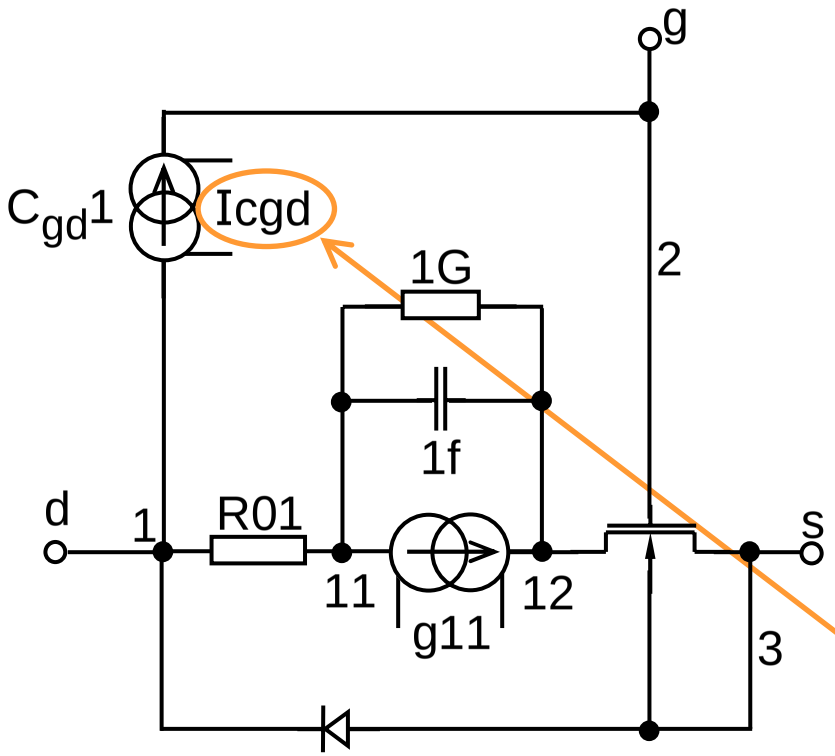
This model is not yet implemented in X-FAB's HV models, ongoing work.



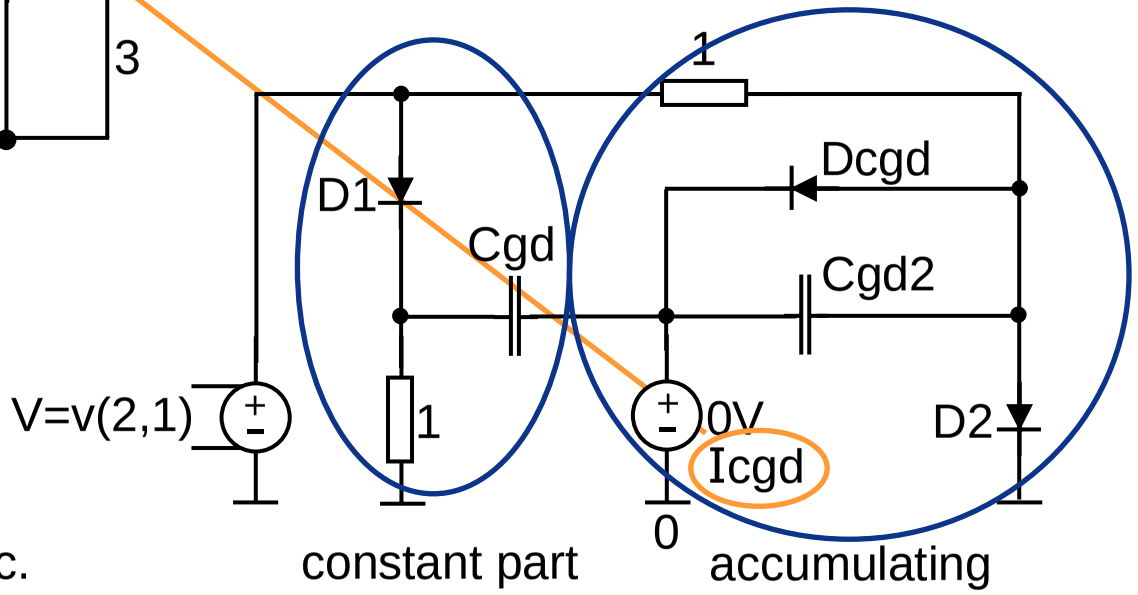


constant cap @ drain (purple)
improved model (green)

Drain Voltage dependent Capacitance Model



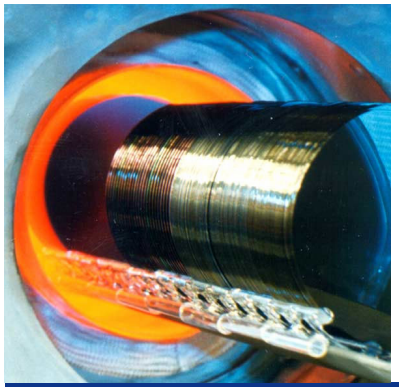
- The capacitance is modeled in an auxiliary circuit. The current is mirrored back into the current controlled current source between the drain and gate node.
- This is fine for stand alone AC simulation but proved as not converging in the ring oscillator test.



An alternative model is in development.
It uses function controlled sources instead of diodes to modulate the CV characteristic.

Agenda (4)

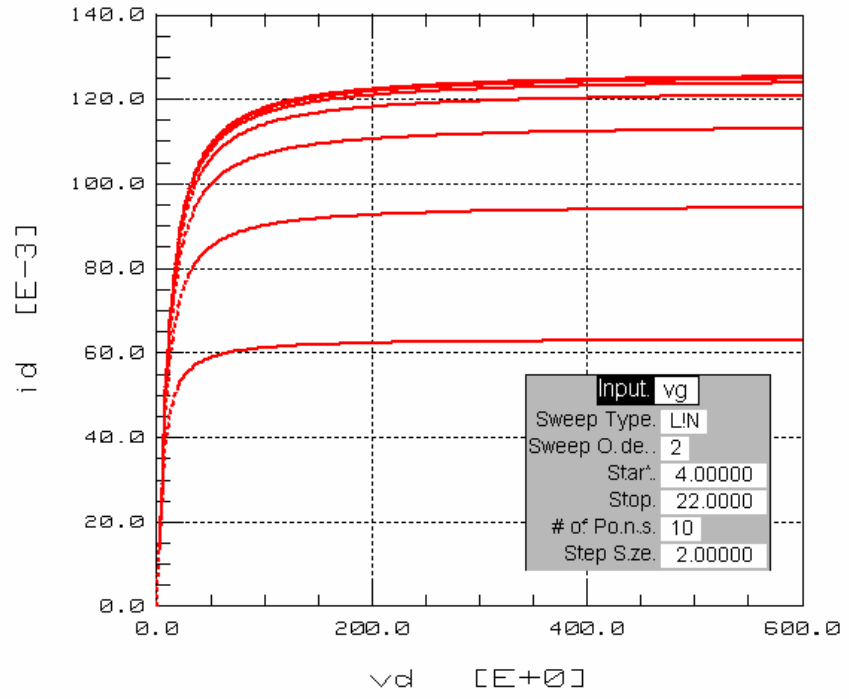
- The Devices:
  Types and Construction
- DC Model:
  Mathematical considerations, types
- AC Model:
  Non diode variable "gate" capacitance
- **Ring Oscillator Test Bench:**
  A challenge for the simulator
- Outlook



Health Checks and Convergence Tests

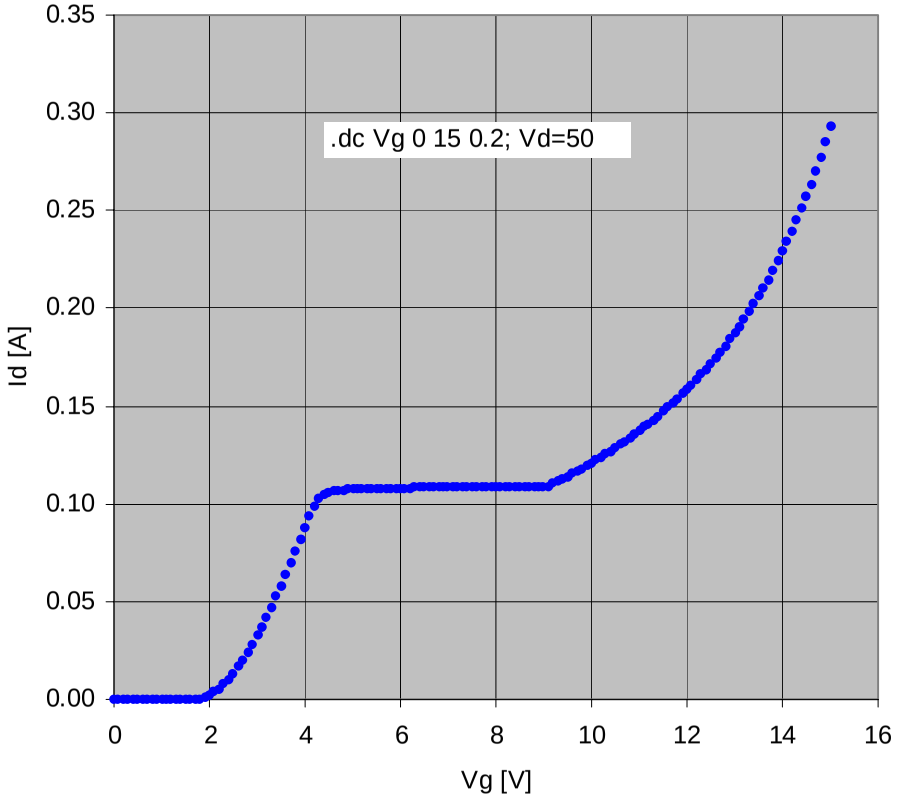
- The Model is tested regarding convergence.
- DC check with extended voltages.
- Transient analysis with ring oscillator as benchmark.

Simulation health check with high gate and drain voltages:



I will show two bad examples from the time of model development on the next slides ...

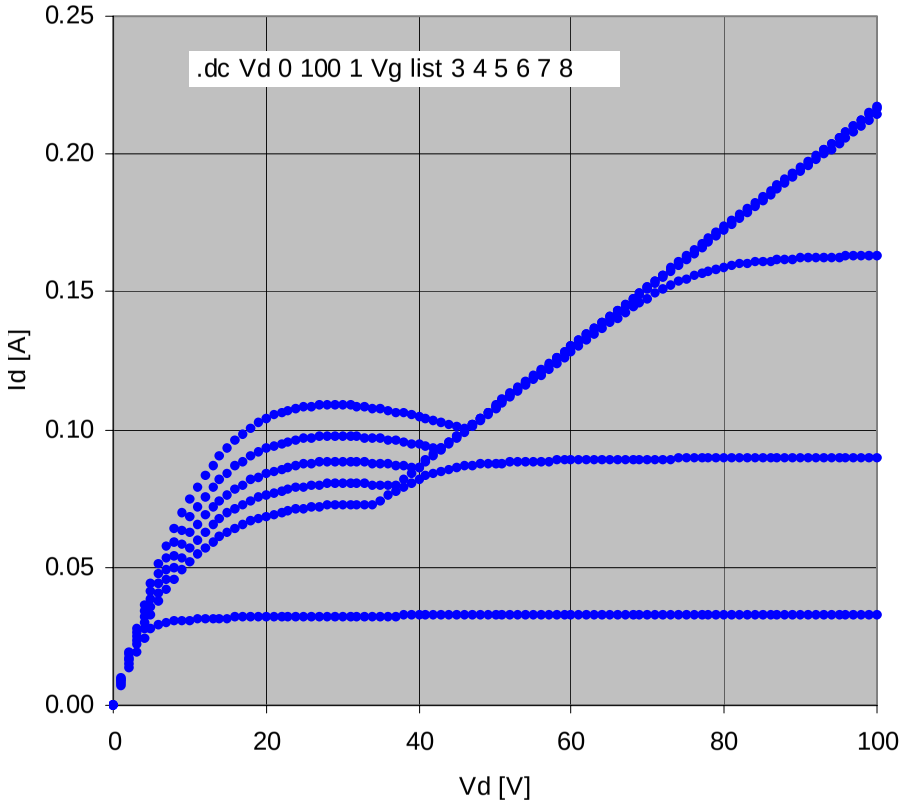
Behavioural Model Pitfalls (1):



Initially the model was extracted at low gate / drain voltages.

➔ It was not sanity checked.

Adverse effect of high drain voltage on the effective gate voltage:
The model is not physical.

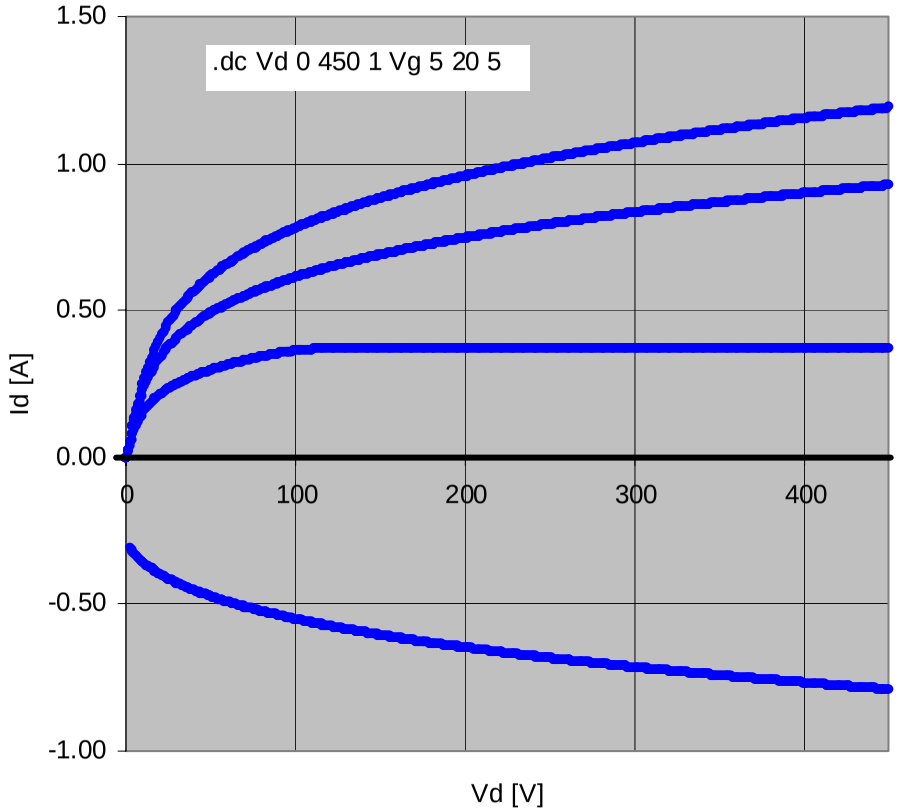


Behavioural Model Pitfalls (2):

> Non physical convergence found by the simulator:

Negative drain current in the simulation due to a reversed voltage in the drain voltage source. This can occur if the mathematical formulation is not monotone or no cautions are taken against nonphysical results.

The simulator finds convergence even with the impossible ...

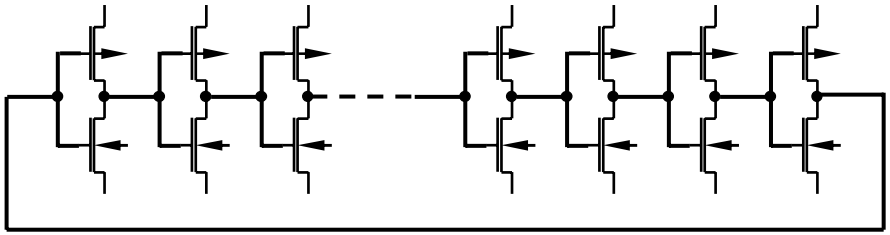


Ringoscillator Test Circuitry

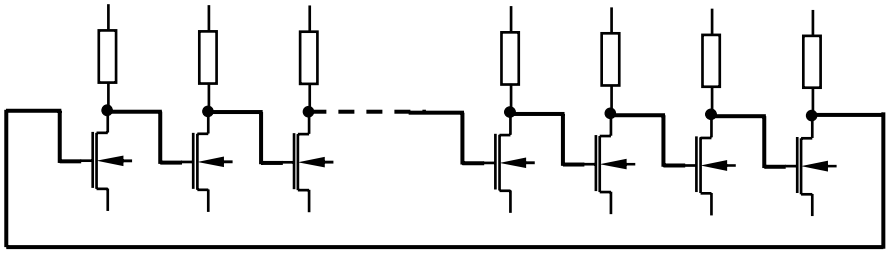
```
.option  tnom=27 gmindc=1e-16 gmin=1e-16 pivtol=0.5e-16
.option  newtol ingold=1  absi=1e-10  reli=1e-5 relv=1e-4
.option  nomod
.TEMP     27.00

* Analyses
.tran 1n 50n uic
.print tran v(1)
.param vdd = 15

vvdd vdd 0 'vdd'
.ic v(1)='vdd'
* Initial Condition to
* start the oscillation

.subckt inv i o vdd
xmp o i vdd vdd phve w=40u l=3.5u pd=50u ps=50u ad=160p as=40p nrd=0.025
nrs=0.025
xmn o i  0   0  nhve w=20u l=3.5u pd=30u ps=30u ad=80p as=20p nrd=0.025
nrs=0.025
.ends inv

.subckt inv8 1 9 vdd
xi1 1 2 vdd inv
xi2 2 3 vdd inv
....
xi6 6 7 vdd inv
xi7 7 8 vdd inv
xi8 8 9 vdd inv
.ends inv8

xinv1 1 2 vdd inv8
....
xinv3 3 4 vdd inv8
xinv0 4 1 vdd inv
```

> Ring oscillator with 25 stages

In this case NMOS and PMOS HV model.



Alternative if only NMOS (PMOS respective):



Transient Analysis Test Bench Results

> The transient analysis simulation time is considerably longer compared to the simple resistor model.

Model Type	CPU time [s]
Simple resistor @ drain	2.52
Resistor with behavioural voltage source	36.41
First Current Source Model	133.35
Improved Model, changed maths	47.94
Final Behavioural Current Source Model	40.24
Model with CV modelling (diodes)	not converg.

Factor 15 to >50 depending on mathematics behind the model.

The challenge is the transient analysis.

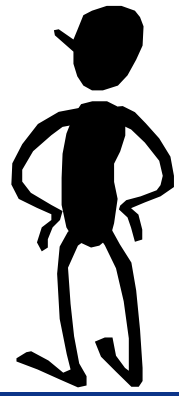
AC and DC analyses are more robust regarding convergence.

Agenda (5)

- The Devices:
  Types and Construction
- DC Model:
  Mathematical considerations, types
- AC Model:
  Non diode variable "gate" capacitance
- Ring Oscillator Test Bench:
  A challenge for the simulator
- Outlook

Plans for Enhancement of the HV Model

- Improvement of the Capacitance Model.
- Test of Capacitance and Reverse Diode Model with transient measurement and simulation. (TT problem)
- Further simplification of the mathematical description for better convergence.
- Consideration of self heating effects.
- Why not VerilogA ?
  Most of the Simulators cope with it nowadays.
  It would made the formulation much simpler.



Agenda (6)

- The Devices:
  Types and Construction
- DC Model:
  Mathematical considerations, types
- AC Model:
  Non diode variable "gate" capacitance
- Ring Oscillator Test Bench:
  A challenge for the simulator
- Outlook

Acknowledgements

I would like to thank:

> Uta Kuniß (X-FAB)
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> Axel Hammer (X-FAB)
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> Matthias Franke (X-FAB)
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