



Modeling and analysis of RF LDMOS for reliability issues

*M. Gares, M. A. Belaid, **H. Maanane**, M. Masmoudi, J. Marcon,
K. Mourgues and Ph. Eudeline*

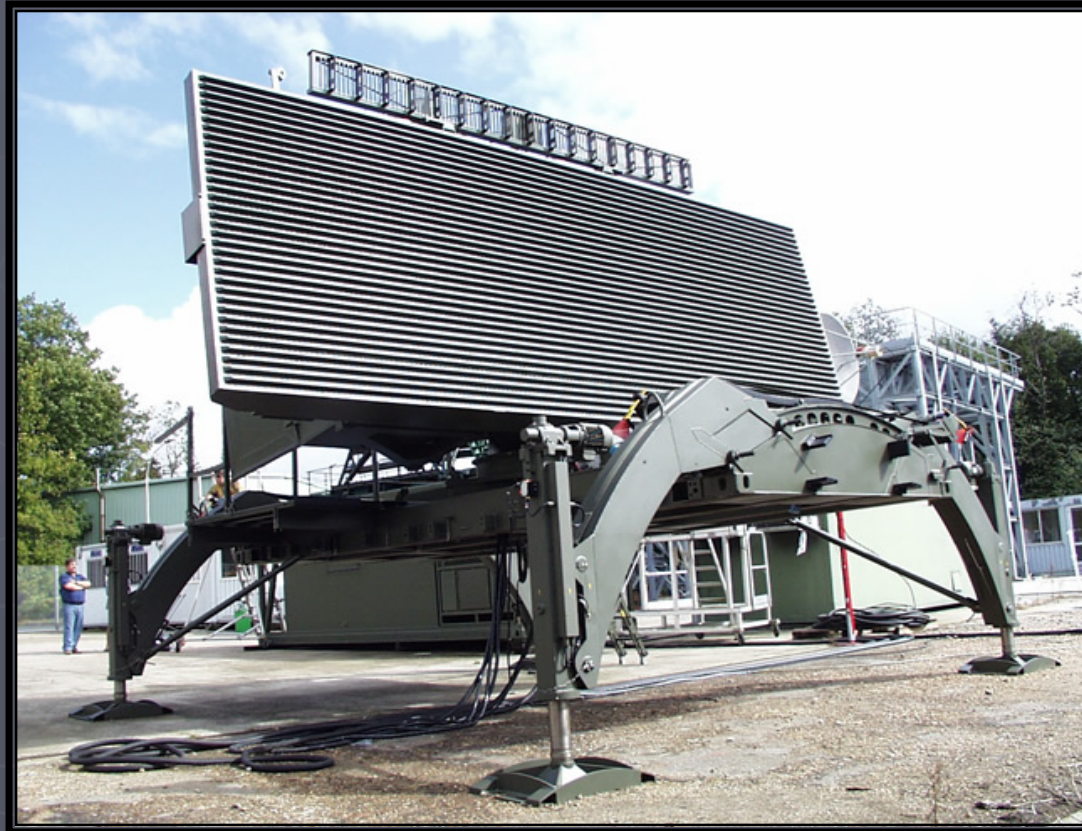
*MOS AK WORKSHOP
Boeblingen, March 24, 2006*

*Electronic **M**icrotechnology & **I**nstrumentation **L**aboratory*

Presentation outline

- ▶ **Context of this study**
- ▶ Objectives
- ▶ Innovative reliability bench
- ▶ DC and CV characterization
- ▶ RF LDMOS modeling
- ▶ Conclusion & prospects

Context of this study



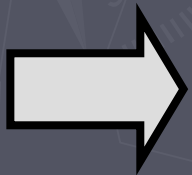
Reliability improvement of amplifier stages for S Band radar (2-4 GHz)

Presentation outline

- ▶ Context of this study
- ▶ **Objectives**
- ▶ Innovative reliability bench
- ▶ DC and CV characterization
- ▶ RF LDMOS modeling
- ▶ Conclusion & prospects

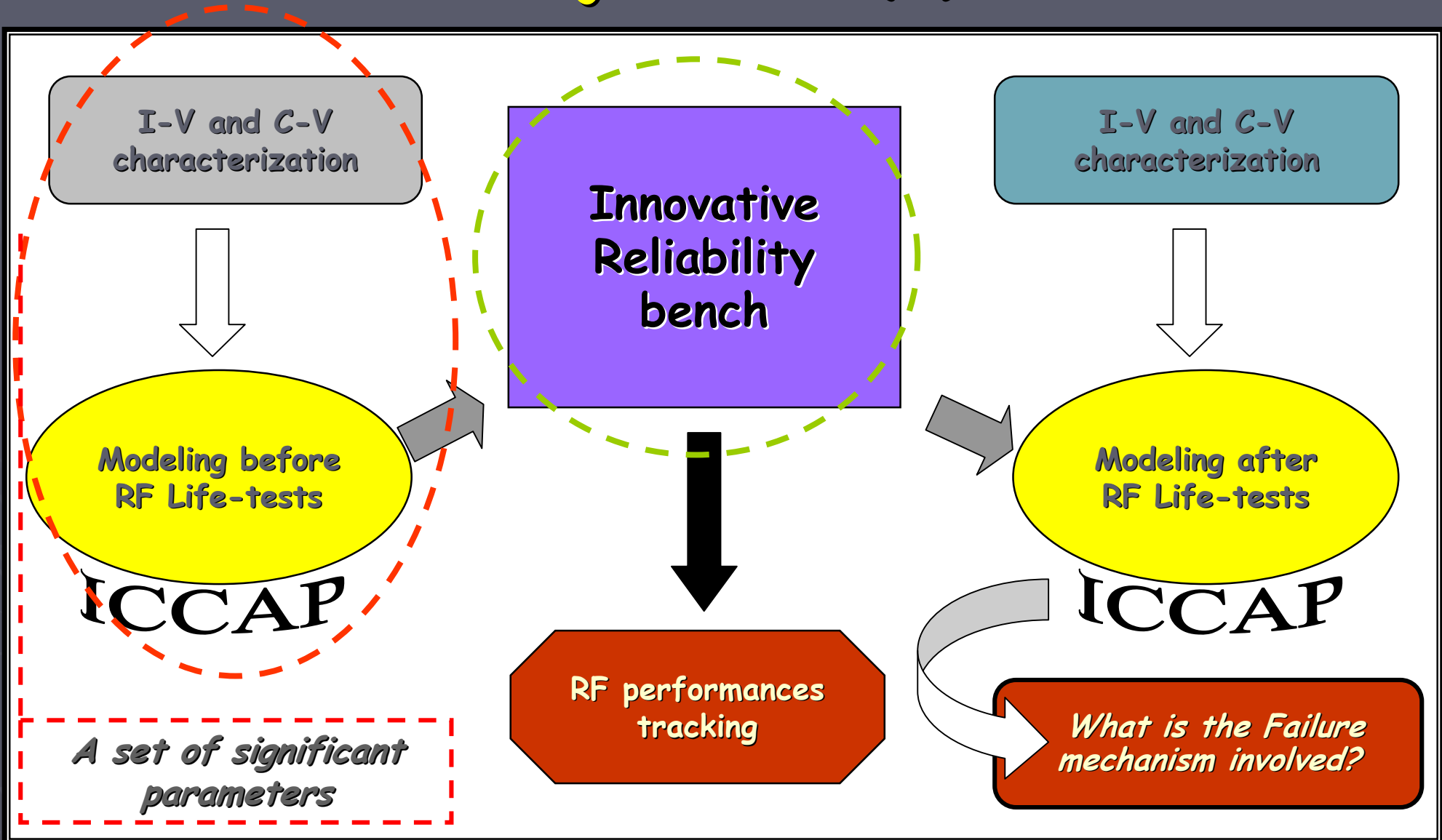
Objectives (1)

- Characterization and modeling for reliability issues
- Obtaining a set of significant parameters such as transconductance (G_M), threshold voltage (V_{TH}), On-state resistance (R_{ON}) and capacitances (C_{RSS} , C_{OSS} , ...).
- Correlation between RF LDMOS electrical parameter drifts and any kind of degradation phenomenon, after RF Life-tests (S band radar operating conditions).



Electro-thermal modeling as a tool for RF LDMOS reliability study

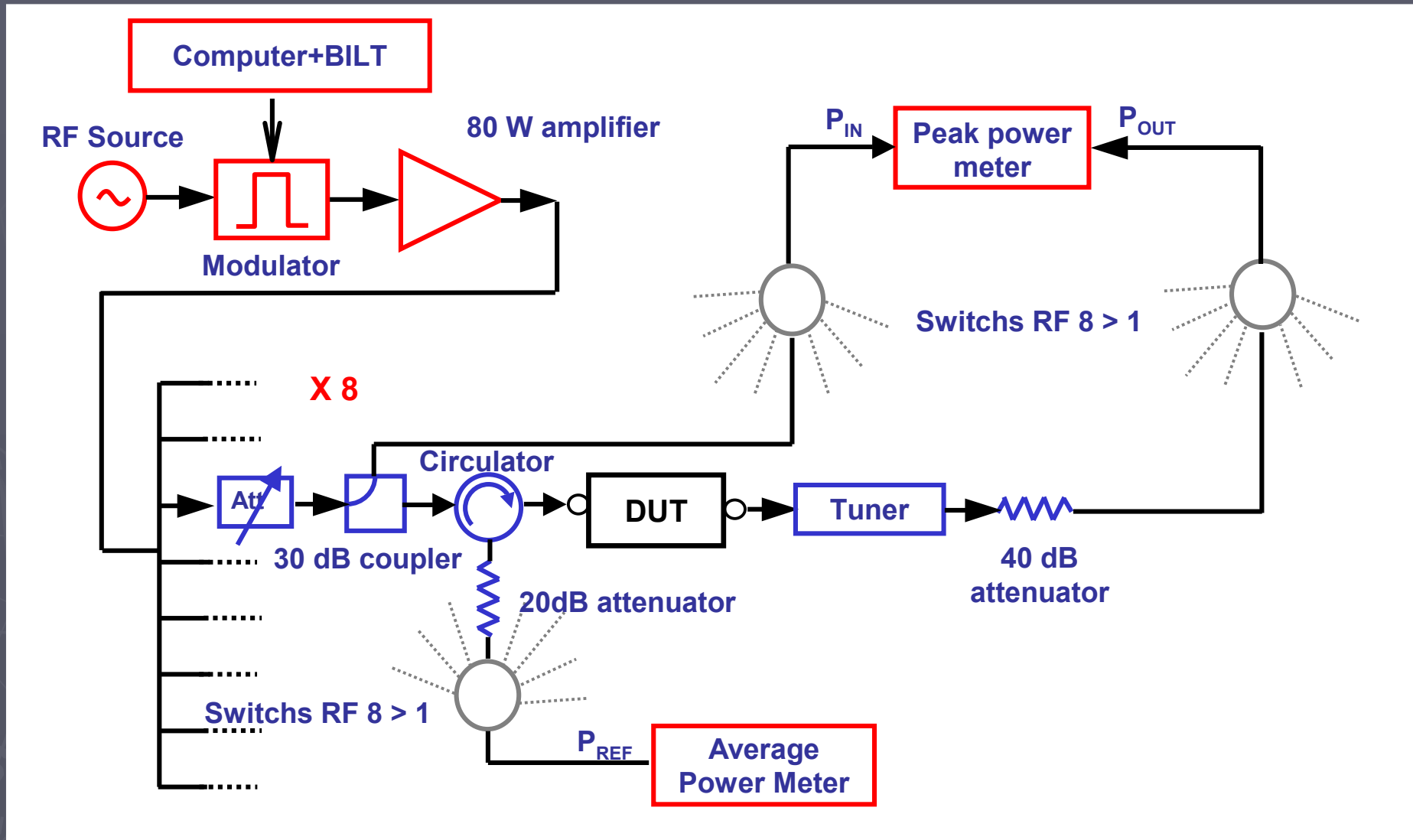
Objectives (2)



Presentation outline

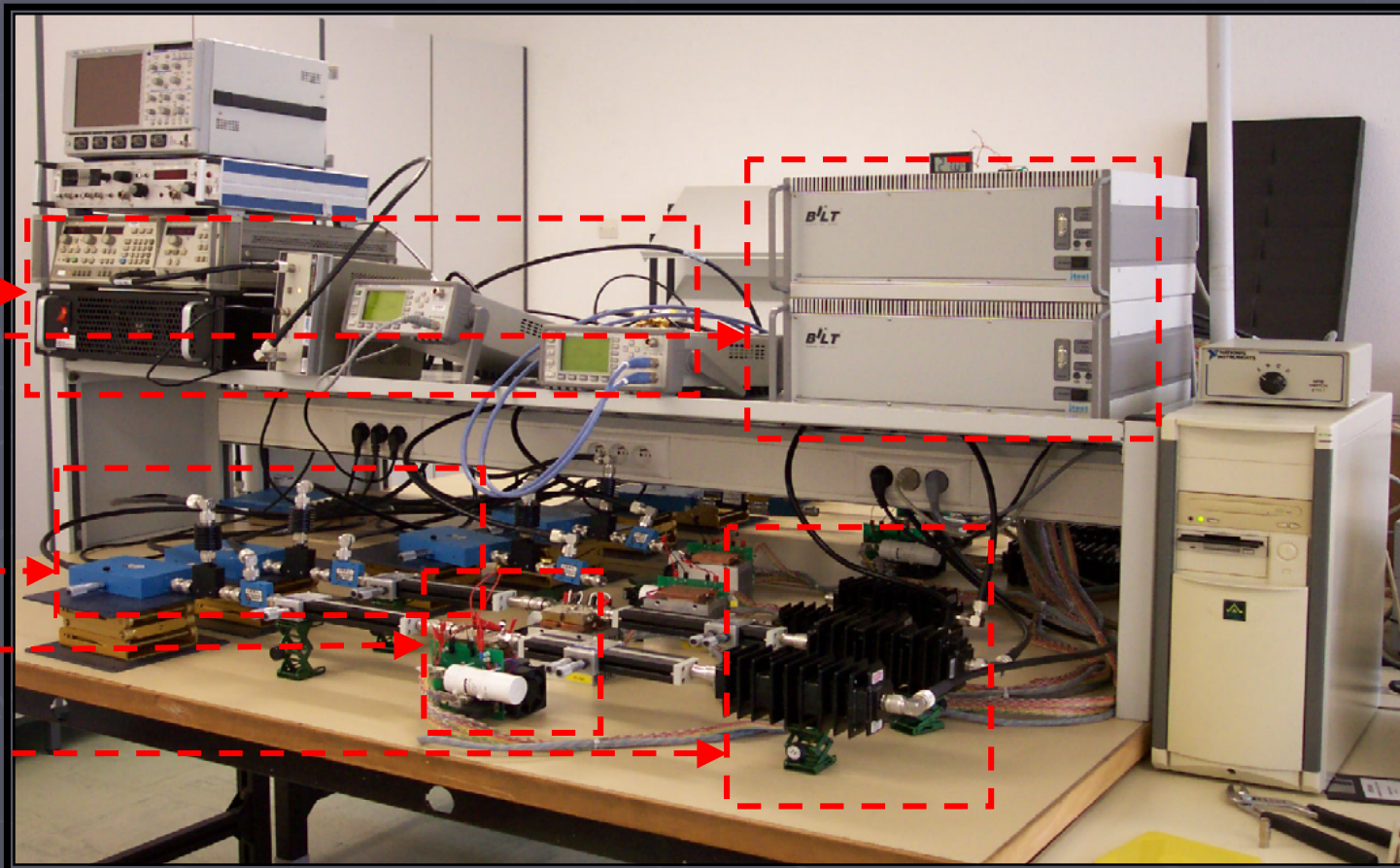
- ▶ Context of this study
- ▶ Objectives
- ▶ **Innovative reliability bench**
- ▶ DC and CV characterization
- ▶ RF LDMOS modeling
- ▶ Conclusion & prospects

Innovative reliability bench (1)



Innovative reliability bench (2)

- ❑ A microwave part
 - ❑ A control/command part piloted by a dedicated software
 - ❑ Thermal module for each devices

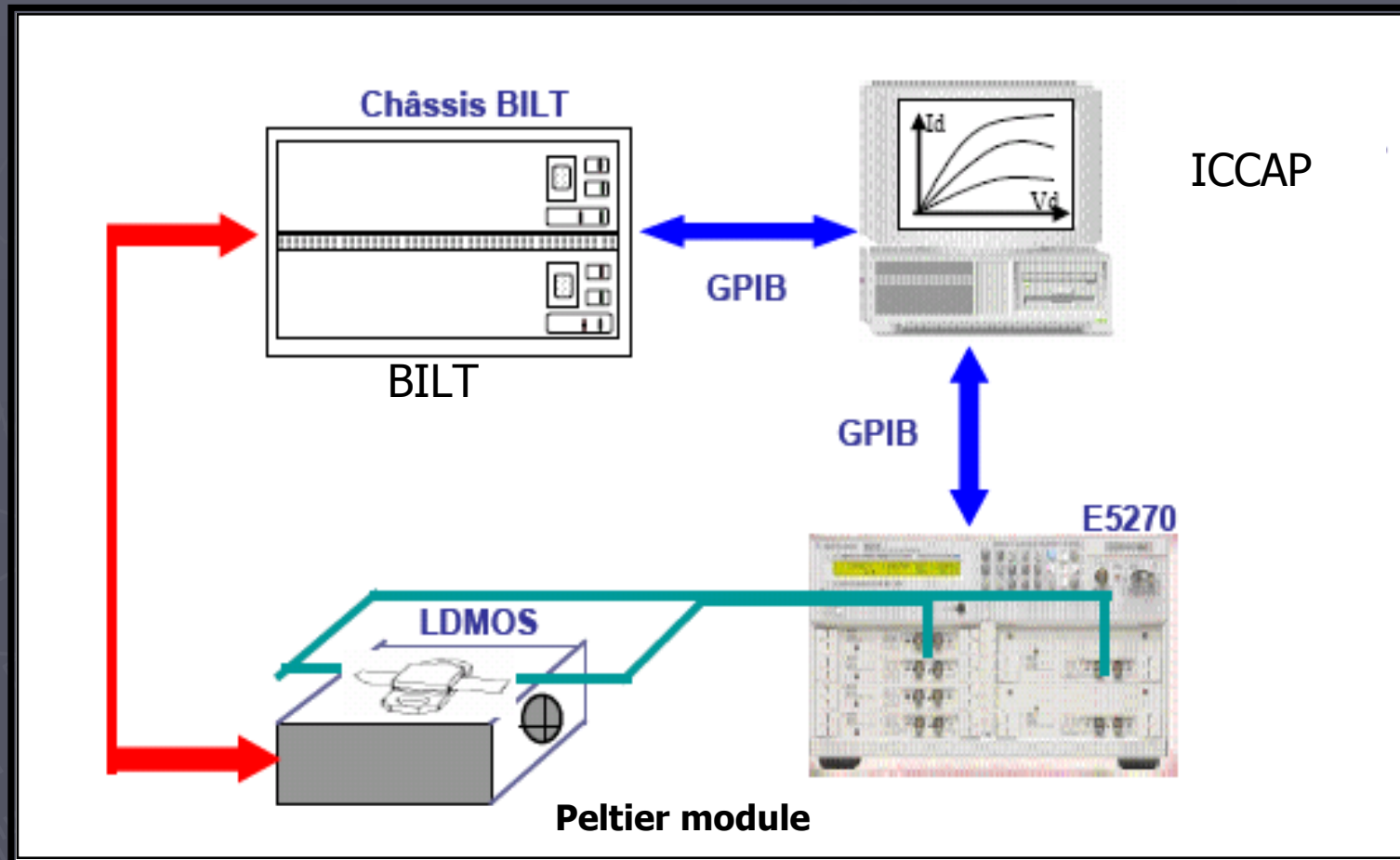


Presentation outline

- ▶ Context of this study
- ▶ Objectives
- ▶ Innovative reliability bench
- ▶ **DC and CV characterization**
- ▶ RF LDMOS modeling
- ▶ Conclusion & prospects

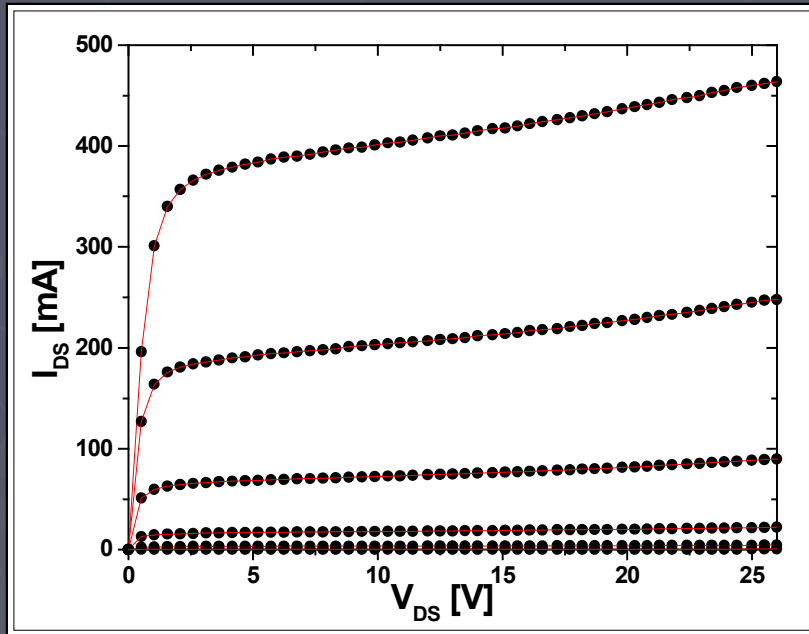
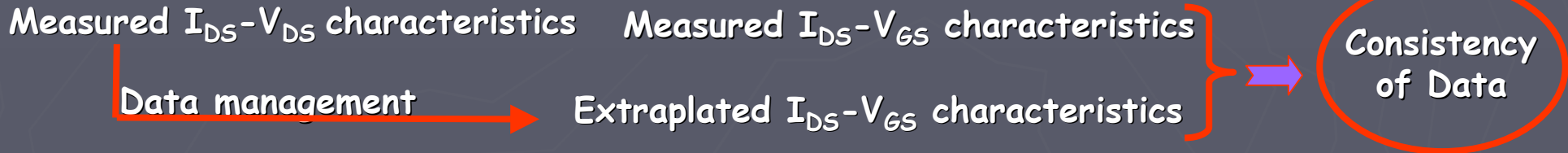
DC Characterization (1)

DC measurement setup



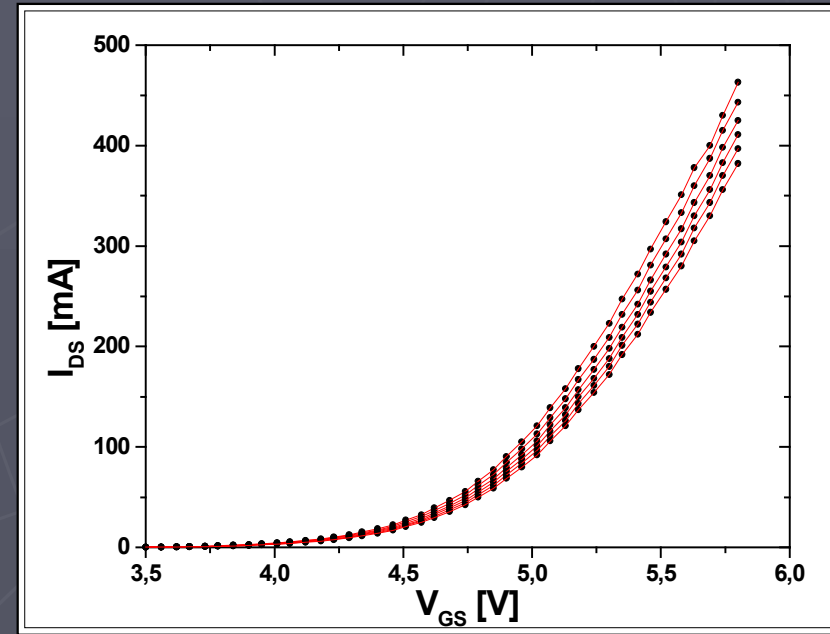
DC Characterization (2)

Results & Measurement consistency



Measured (symbols) and extrapolated (continuous lines) output characteristics

$V_{DS}=0...26$ V with a step of 520 mV
 $V_{GS}=3.5...5.8$ V with a step of 383 mV

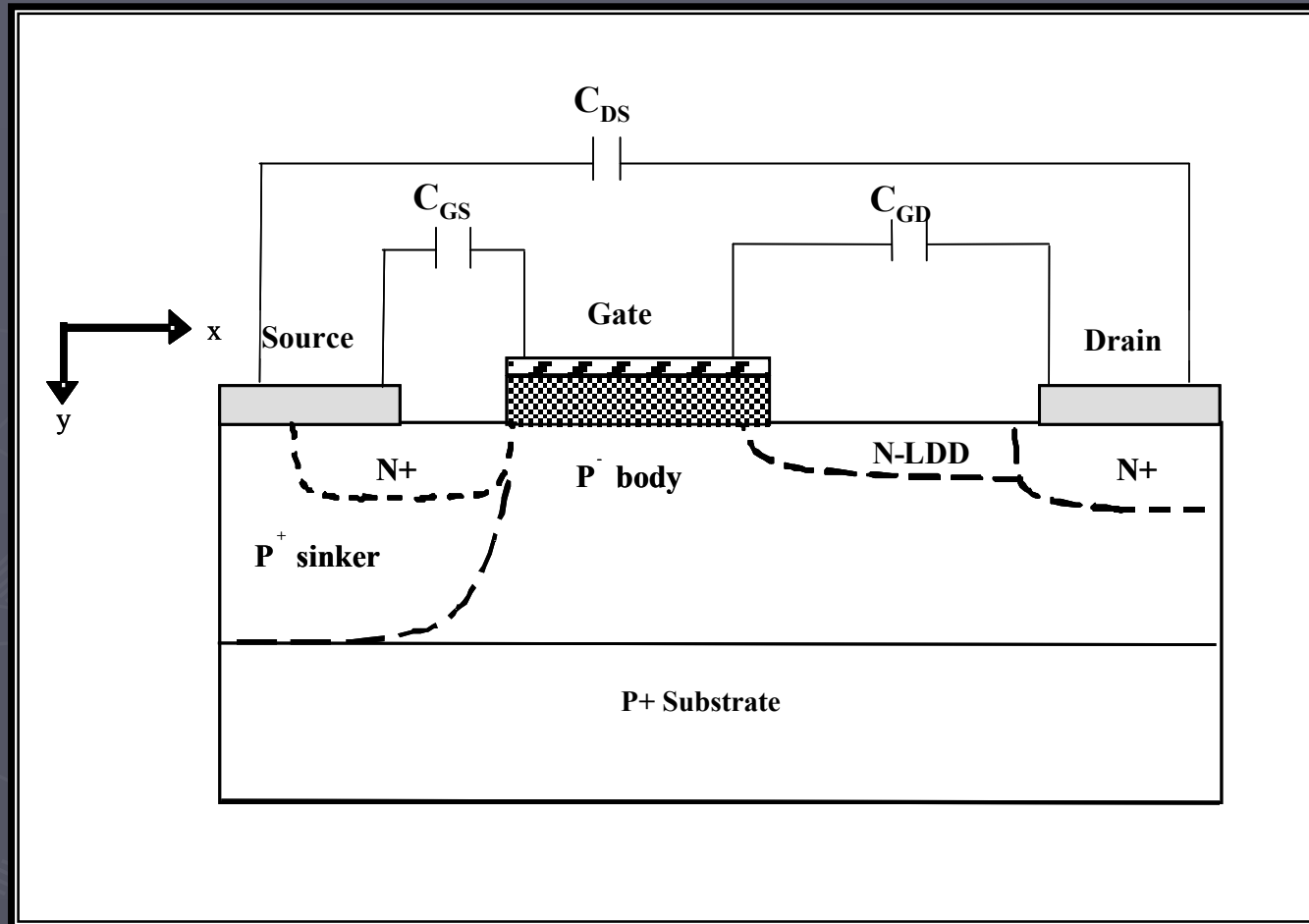


Measured (symbols) and extrapolated (continuous lines) transfer characteristics

$V_{DS}=0...26$ V with a step of 4.33 V
 $V_{GS}=3.5...5.8$ V with a step of 45 mV

CV Characterization (1)

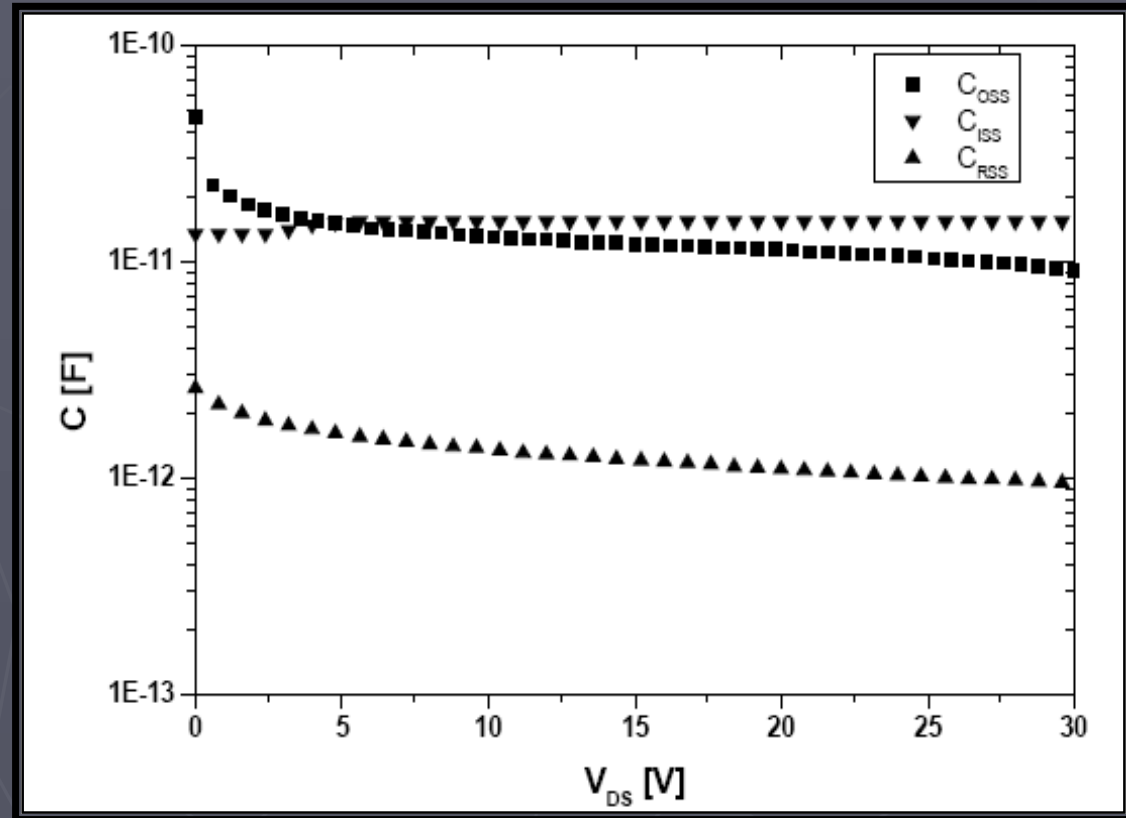
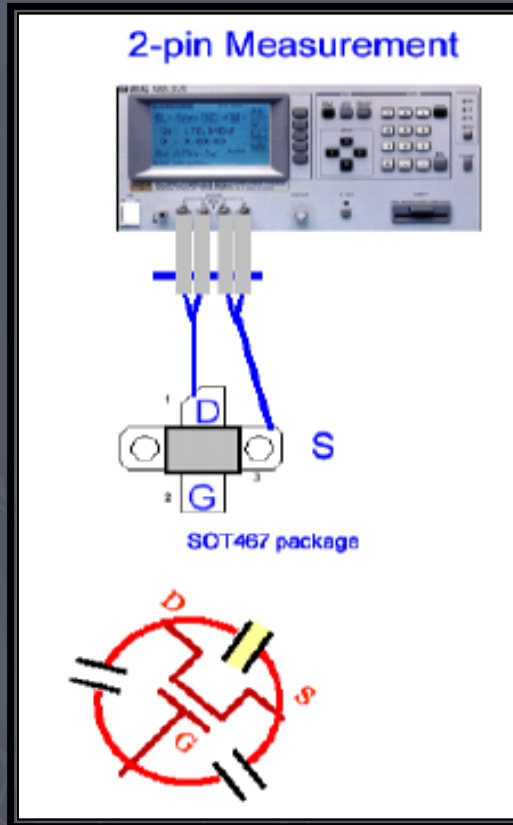
localization of capacitances



RF LDMOS device cross-section with its intrinsic capacitances

CV Characterization (2)

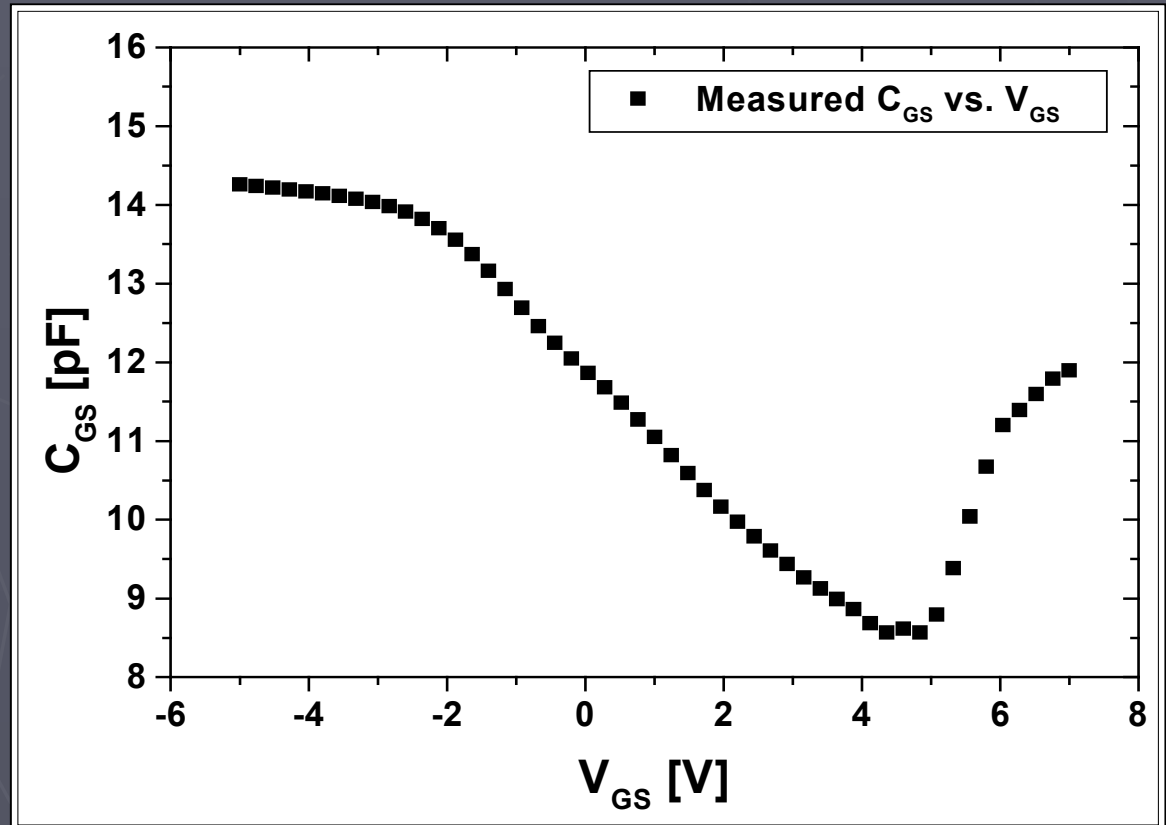
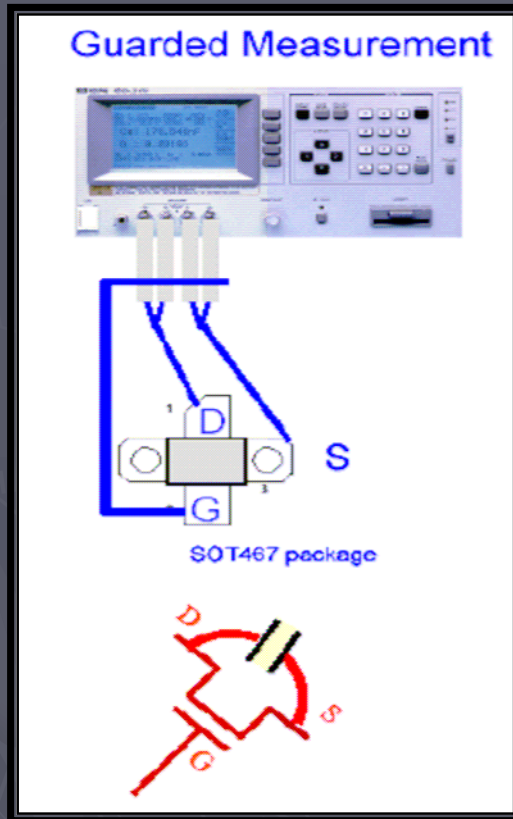
Primary capacitance measurements



Measured C_{RSS} , C_{ISS} and C_{OSS} , Freq=1MHz and $V_{DS}=[0V, 30V]$ at room temperature

CV Characterization (3)

Intrinsic capacitance measurements



Measured C_{GS} vs. V_{GS} profile ($V_{DS} = 0V$ and Freq. = 1 MHz) at room temperature.

Presentation outline

- ▶ Context of this study
- ▶ Objectives
- ▶ Innovative reliability bench
- ▶ DC and CV characterization
- ▶ **RF LDMOS modeling**
- ▶ Conclusion & prospects

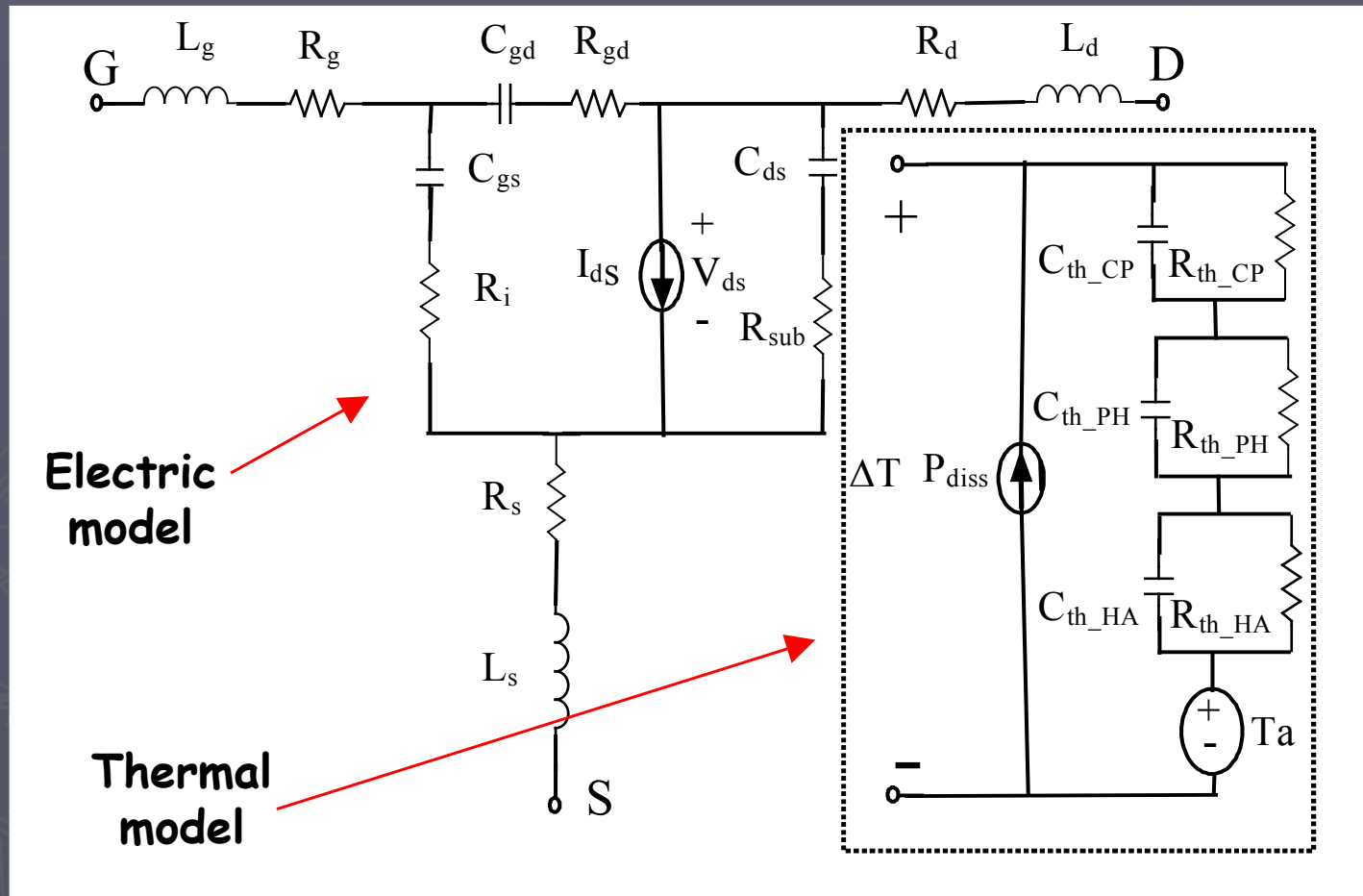
RF LDMOS modeling

Improved MET LDMOS Model overview

- An empirical large signal non-linear model.
- An electro thermal model including static and dynamic thermal dependencies.
- An electro thermal model, taking into account self heating effects and temperature influence on LDMOS electric behaviour.

RF LDMOS modeling

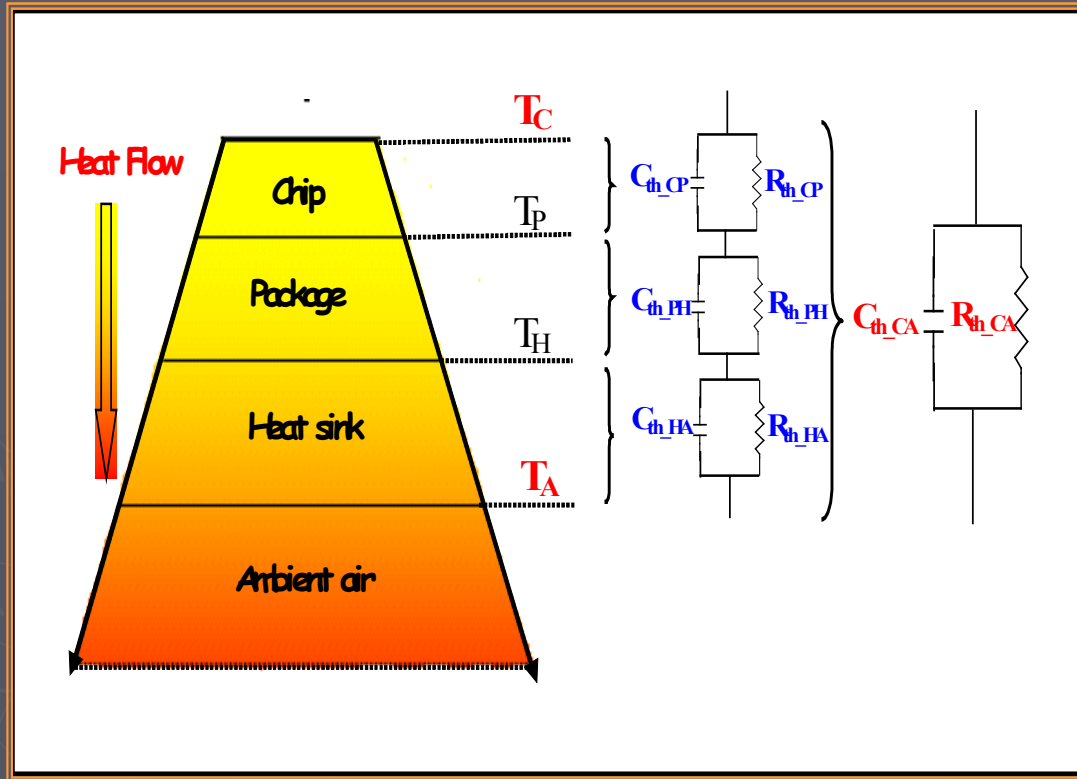
Improved MET LDMOS Model overview



Large signal equivalent circuit of the MET LDMOS model

RF LDMOS modeling

Improved MET LDMOS model overview (thermal aspects)



$$\Delta T = R_{th_CA} \cdot P_{diss} + T_a$$

$$P_{diss} = I_{ds} \cdot V_{ds}$$

$$R_{th_CA} = R_{th_CP} + R_{th_PH} + R_{th_HA}$$

RF LDMOS modeling

Implementing the model equations into IC-CAP's ADS circuit page

- An ADS "SDD" (Symbolic defined device) was developed.
- The SDD is a feature in ADS, which allows the user to specify a real-time model description, without compilation.
- The developed SDD covers the transistor DC forward current $i_d=f(v_{GS},v_{DS})$, the series resistors R_G , R_S and R_D , as well as the charges q_{GS} , q_{GD} and q_{DS} .
- The thermal network is implemented taking into consideration the temperature dependence of the parameters.

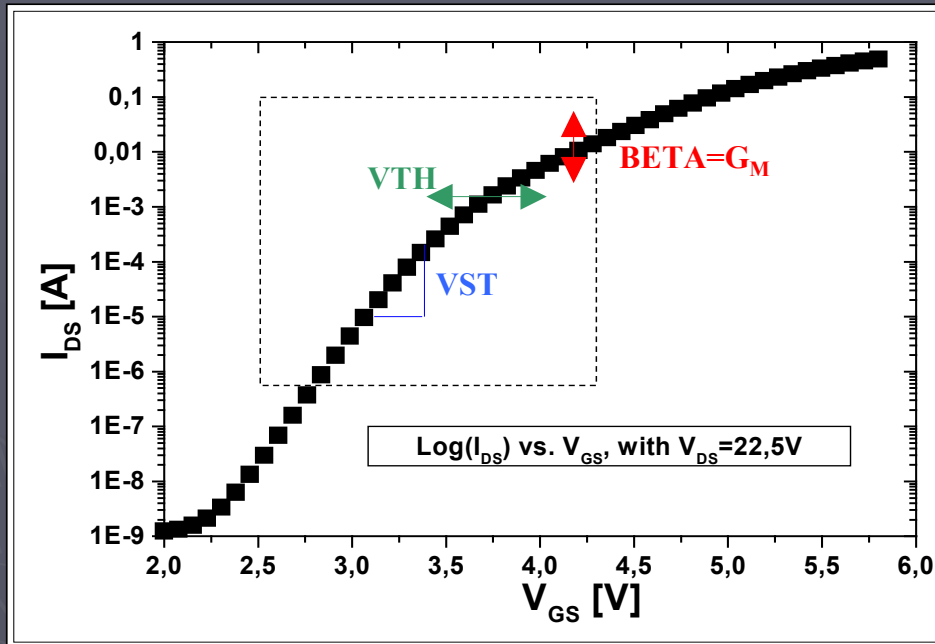
RF LDMOS modeling

Main parameters of the model

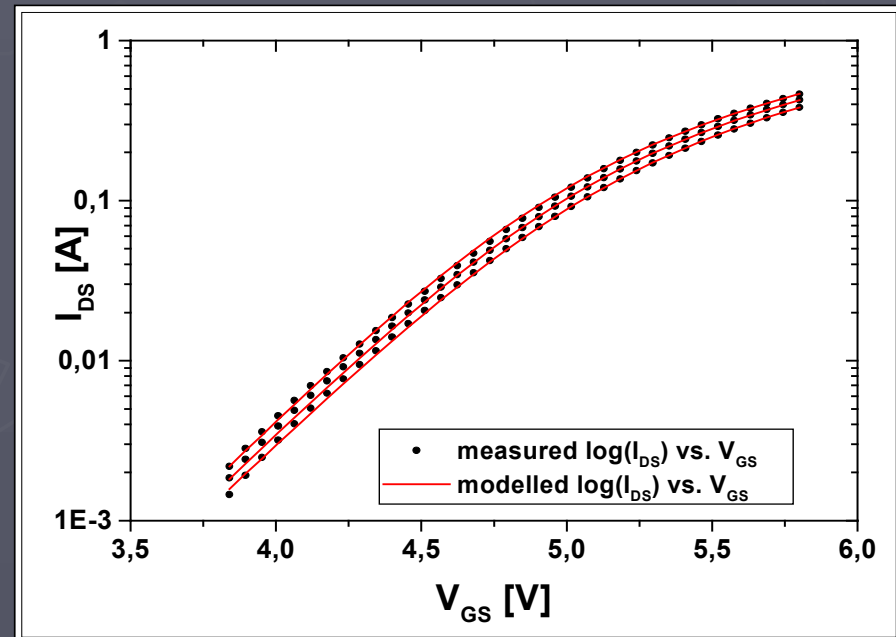
Parameter	Definition	Unit
Beta	Transconductance parameter	Siemens
V_t	Threshold voltage	V
Delta	V_t variation according to V_{ds}	V
V_{br}	Break down voltage	V
$K_{1/2}, M_{1/3}$	Break down parameters	--
V_K	I_{ds} equation coefficient	V
Alpha	Linear range	$1/\Omega$
Gamma	Slope of the channel current	--
Lambda	Shapes of the I_{ds} saturation	$1/V$
V_{gexp}	Term of power	--
V_{ST}	Sub-threshold slope coefficient	V

RF LDMOS modeling

Sub-threshold modeling : $\log(I_{DS})$ vs. V_{GS}



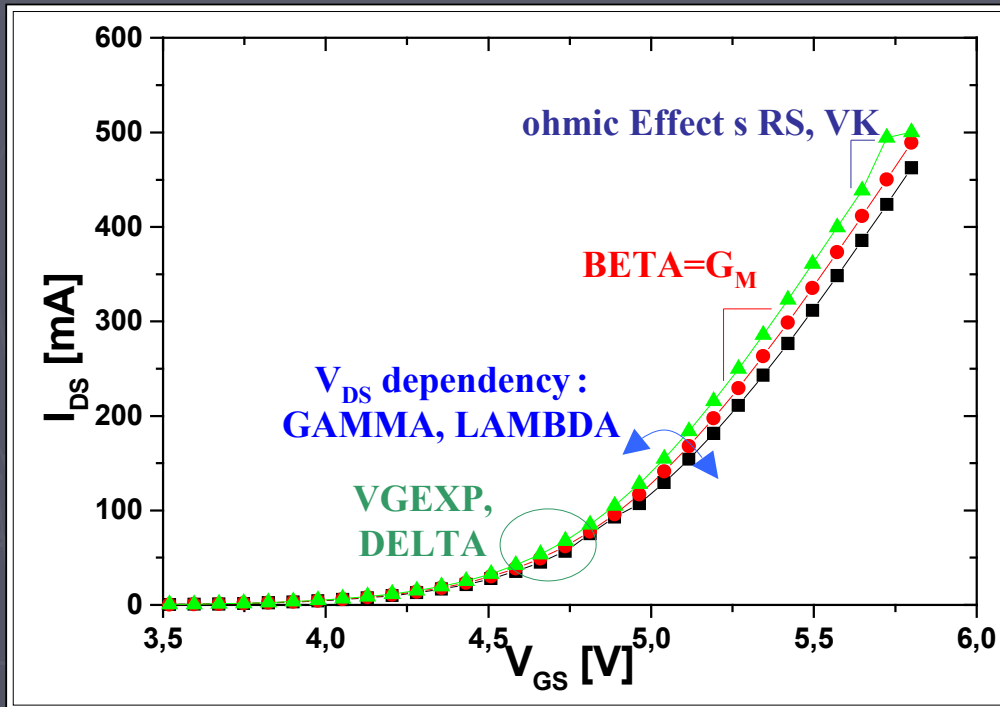
Measured transfer characteristics ($\log(I_{DS})$ vs. V_{GS}) with the influence of few MET LDMOS model parameters



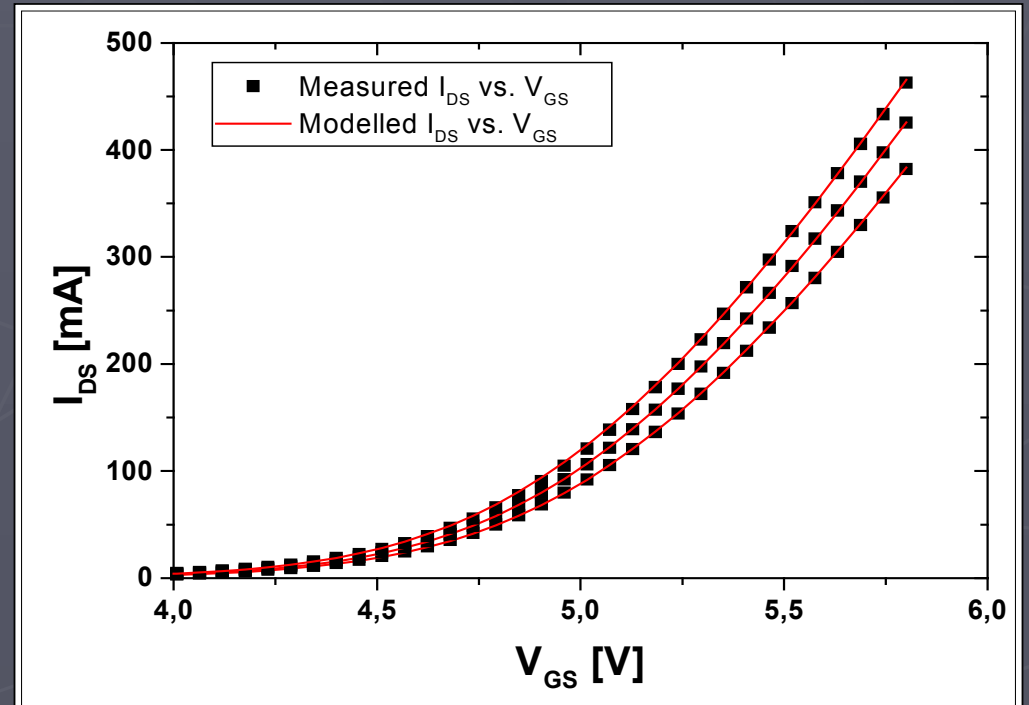
Measured (symbols) and modelled (continuous lines) transfer characteristics, with $V_{GS}=3.8-5.8$ V (step=56 mV) and $V_{DS}=5.2$ V, 17.68 V & 26 V

RF LDMOS modeling

Transfer characteristics modeling (I_{DS} vs. V_{GS})



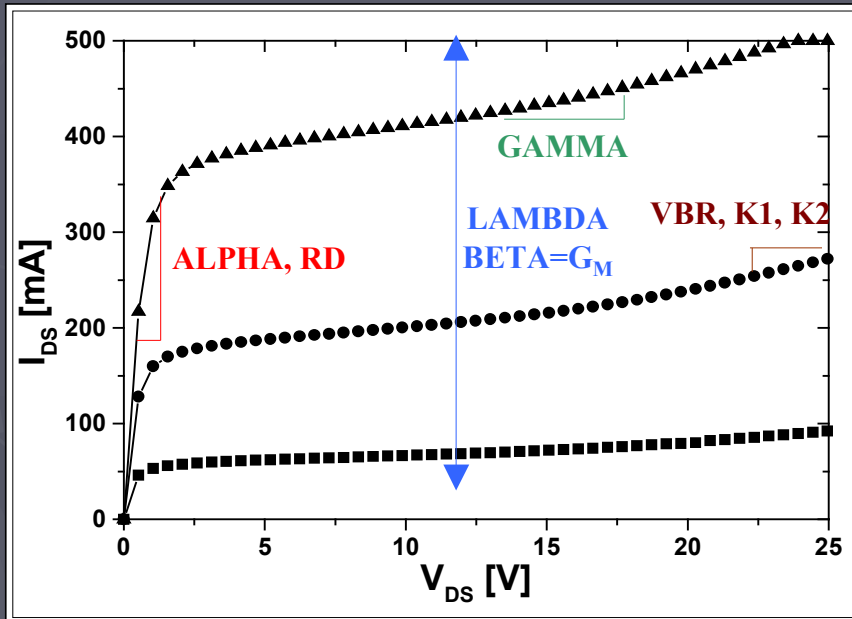
Measured transfer characteristics I_{DS} vs. V_{GS} with the influence of few MET LDMOS model parameters



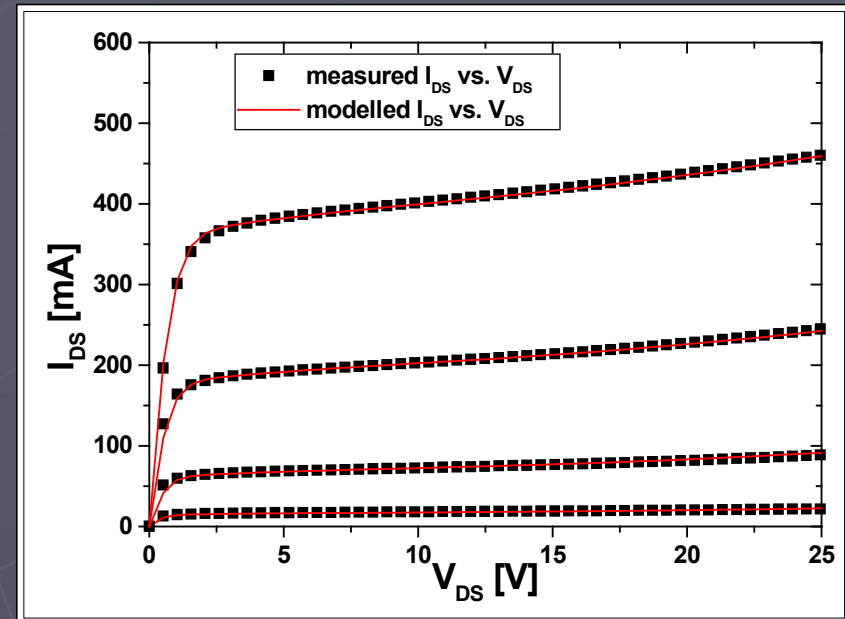
Measured (symbols) and modelled (continuous lines) transfer characteristics, with $V_{GS}=3.8$ V-5.8 V (step=56 mV) and $V_{DS}=5.2$ V, 17.68 V & 26 V.

RF LDMOS modeling

Output characteristics modeling : I_{DS} vs. V_{DS}



Measured output characteristics (I_{DS} vs. V_{DS}) with the influence of few MET LDMOS model parameters



Measured (symbols) and modelled (continuous lines) output characteristics with $V_{DS}=0-26$ V (step=520 mV) and $V_{GS}=4.45$ V, 4.9 V, 5.35 V & 5.8 V

RF LDMOS modeling

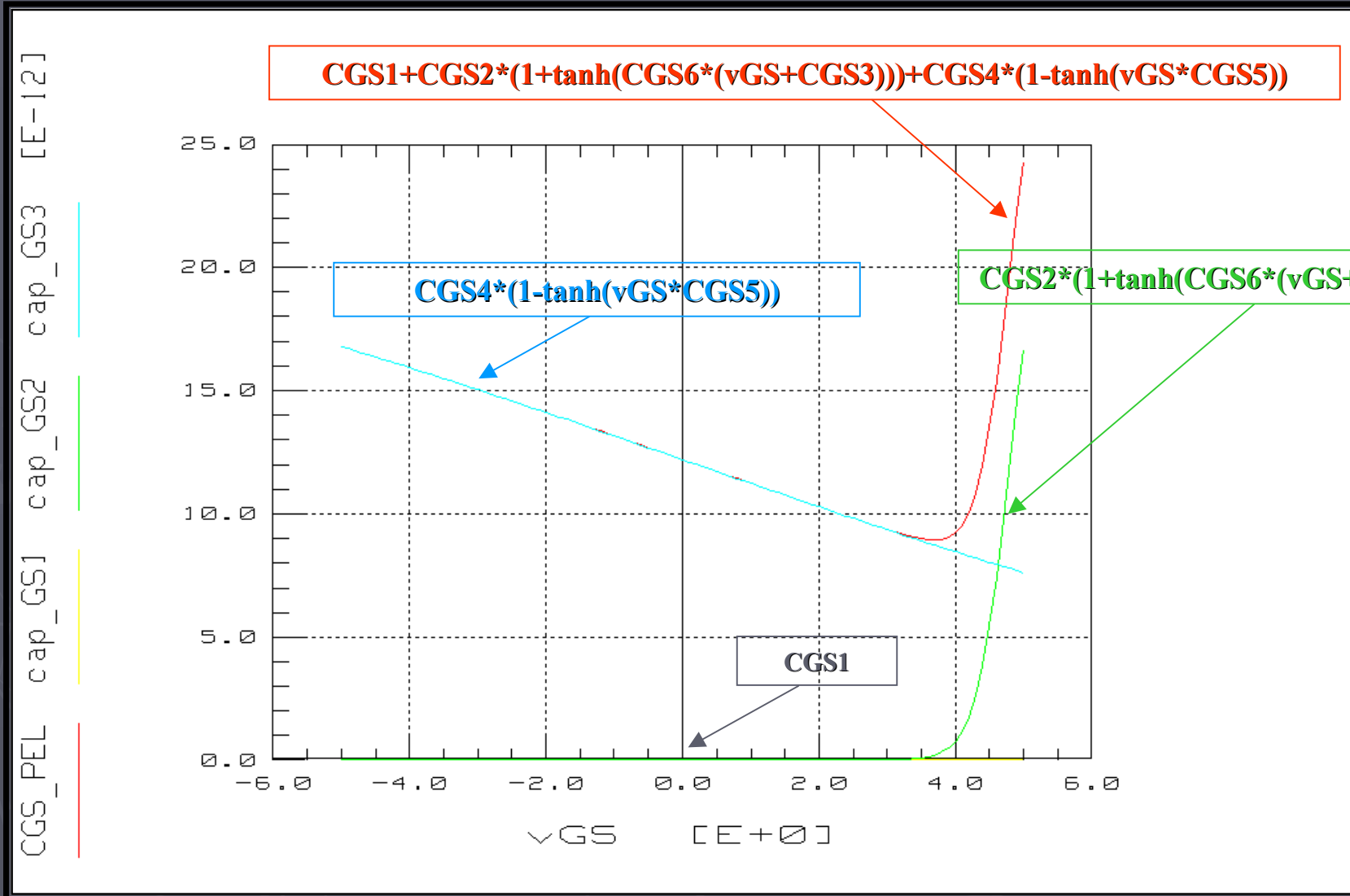
Model parameter extraction

MET model parameters	Classic DC parameter names	values obtained by modeling (Fitting error <1%)
VTO_0	V_{TH}	4.2 V
BETA_0	G_M	0.53 S
VBR_0	BV_{DSS}	87.5 V
RD_0	R_{DSON}	1.4 Ohms

Summary of few DC significant parameters extrapolated by modeling

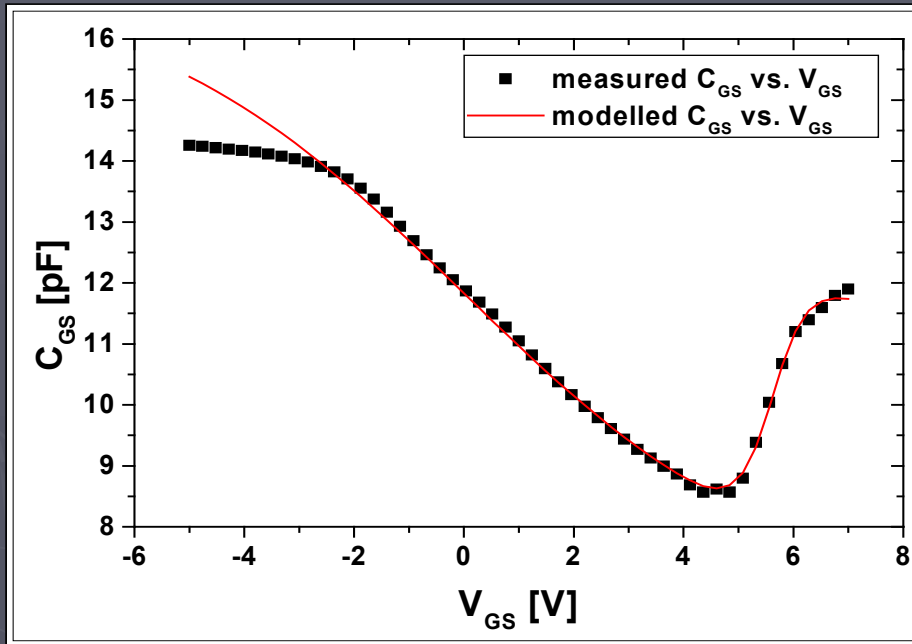
RF LDMOS modeling

C_{GS} capacitance modeling

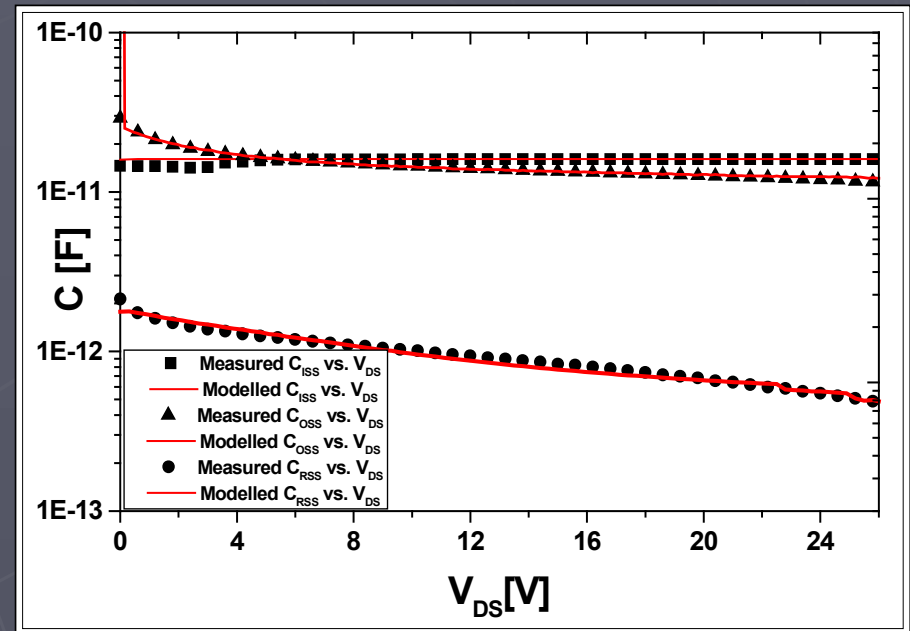


RF LDMOS modeling

CV modeling results



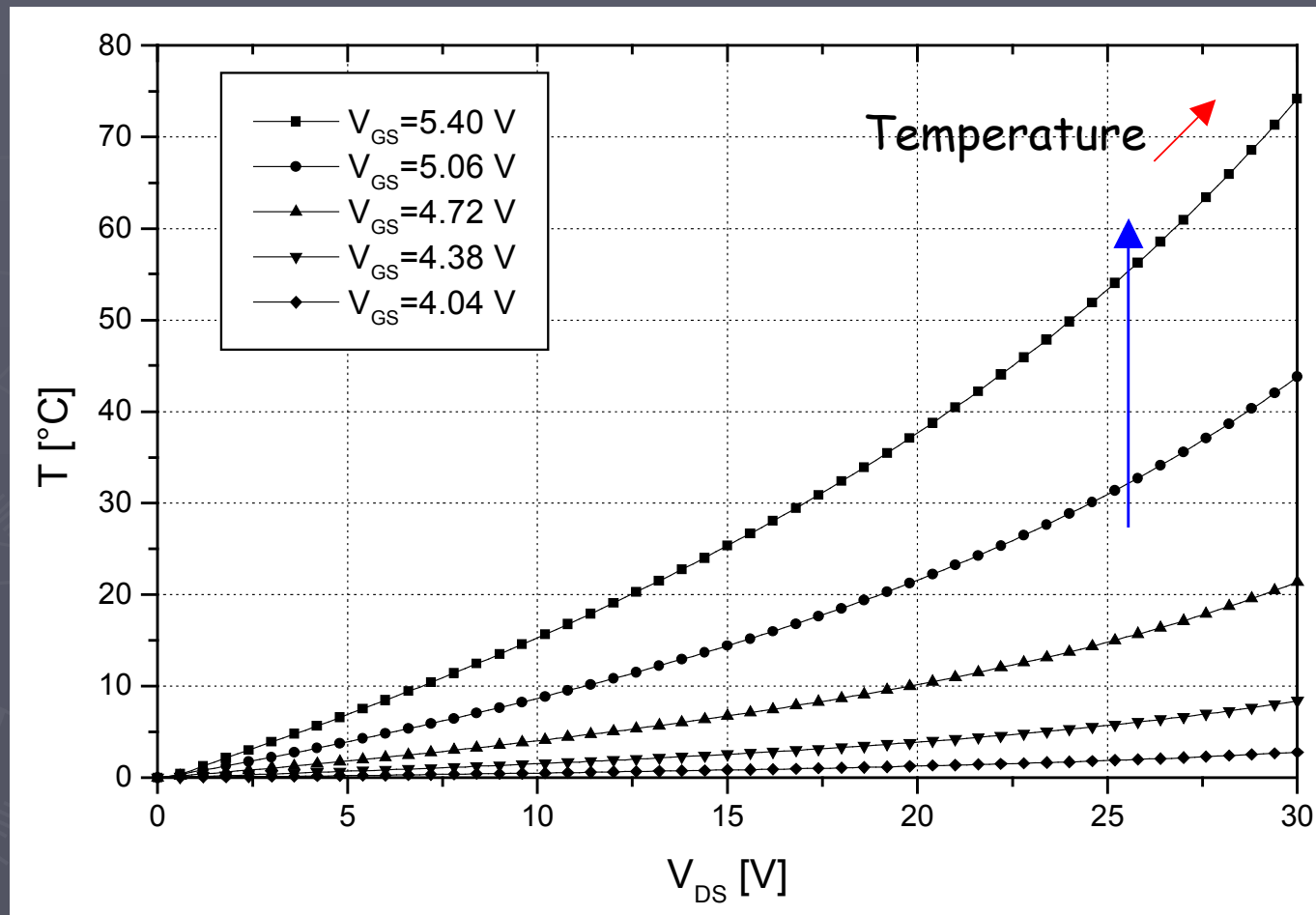
Measured (symbols) and modelled (continuous lines) C_{GS} capacitance, $V_{GS} = [-5 V, 7 V]$ and $V_{DS} = 0 V$, with $Freq = 1 MHz$.



Measured (symbols) and modelled (continuous lines) C_{ISS} , C_{OSS} & C_{RSS} capacitances, $V_{DS} = [0 V, 26 V]$, $V_{GS} = 0V$, and $Freq = 1 MHz$.

RF LDMOS modeling

Thermal simulation results



Presentation outline

- ▶ Context of this study
- ▶ Objectives
- ▶ Innovative reliability bench
- ▶ DC and CV characterization
- ▶ RF LDMOS modeling
- ▶ **Conclusion & prospects**

Conclusion

- ❑ An improved MET LDMOS model (three thermal cells), taking into account self-heating effects and the temperature influence was developed.
- ❑ The DC and CV modeling results fitted well with those obtained from the measurements
- ❑ A set of significant parameters has been extrapolated by modeling and used to help identifying a degradation phenomenon after RF life-tests.

Prospects

- ❑ S parameter measurements and simulations are in progress, to get a complete compact model and have a large significant parameter set.
- ❑ Simulation in Harmonic Balance (P_{OUT} vs. P_{IN} , IMD, ...) for RF LDMOS performance predictions after RF life-tests.
- ❑ Channel temperature measurement in order to confirm the thermal model.

Questions





RF Life-test conditions (1)

✓ DC

$V_{DS}=44\text{ V}$,
 $V_{GS}=3,79\text{ V}$ with $I_{DQ}=3\text{mA}$ at 25°C .

✓ RF

Fréq= 2,9 GHz.
Pulse length/duty cycle=500 μs /50%.
 $P_{IN}=30,5\text{ dBm}$, $P_{OUT}=43-44\text{ dBm}$.

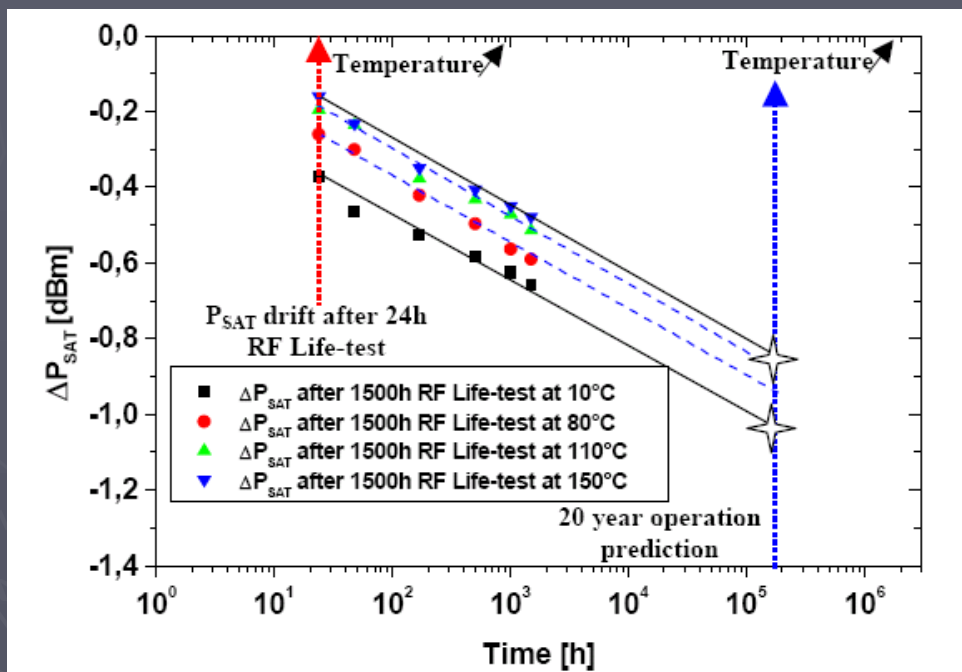
✓ Thermal

$T (^{\circ}\text{C}) = 10, 80, 110\text{ et } 150^{\circ}\text{C}$.

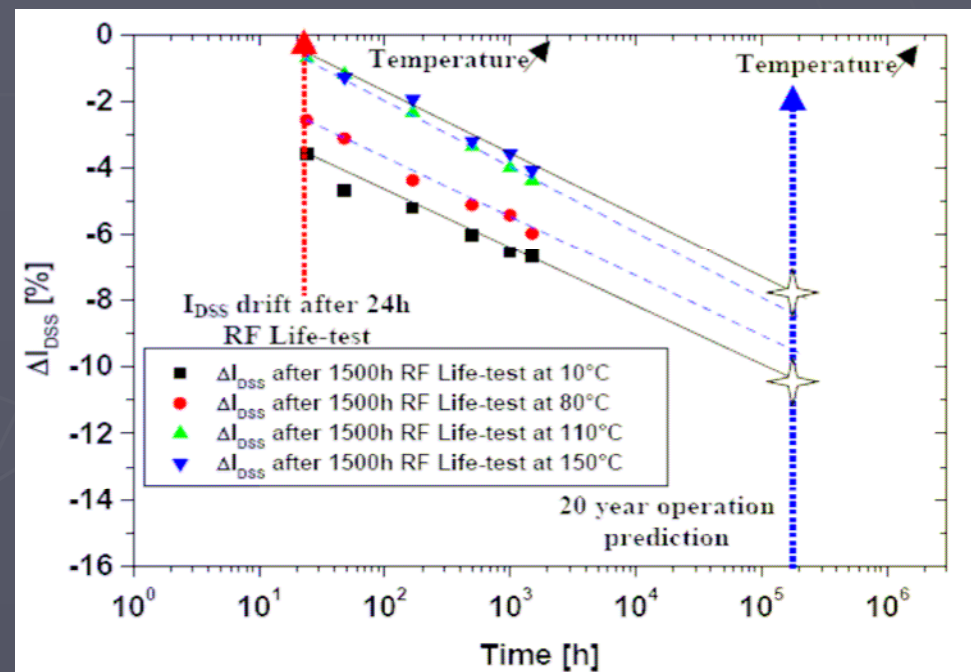
RF Life-test conditions (2)

Device base plate temperature (°C)	P_{IN} (dBm)	P_{OUT} (dBm)	P_{REF} (dBm)	I_{DQ} @ device base plate temperature (mA)	I_{DSS} during RF pulses (mA)
10	30.5	43,8	23.9	1.76	557.89
80	30.5	43.57	22,2	5,023	550
110	30.5	42.6	17.3	7.5647	537.68
150	30.5	40.2	22.2	13.348	500

Results obtained after RF Life-test



RF saturated output power evolution over ageing time (1500h) for various temperature conditions.



Drain source current evolution over ageing time (1500h) for various temperature conditions.

RF LDMOS modeling

Thermal aspects

