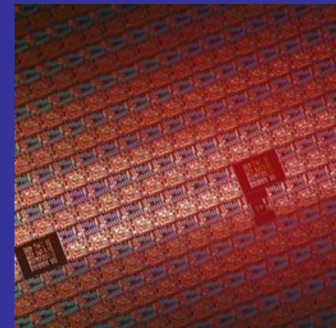
Accelerating the next technology revolution

Physical models for transistor gate stack degradation processes

Gennadi Bersuker

D. Veksler, H. Park, C. Young

FEP Division



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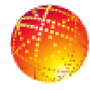
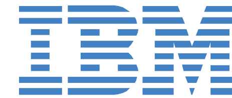
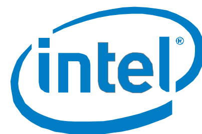
Global Consortium

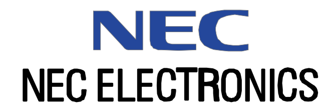
SEMATECH, ISMI, and Supplier members

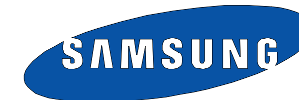

GLOBALFOUNDRIES

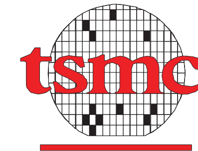
HEWLETT PACKARD











SEMATECH Locations- Austin

- Manufacturing Programs: ISMI, 450mm, NGF, EPIT
- Front end Technologies: Logic, memory, RF/Analog/MS
- Emerging Technologies: MEMS/NEMS, sensors, CMOS+, disruptive memory/logic, PV
- Fabless Program

SEMATECH Locations- Albany

- Lithography: EUV, immersion, Masks, alt. Litho
- Front End Technologies: Logic, memory, electrical characterization and reliability
- 3D IC: TSV
- Metrology

SEMATECH CMOS Activities

High-k / Metal Gate

Hi Mobility Channel

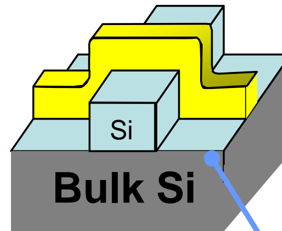
Si FinFET

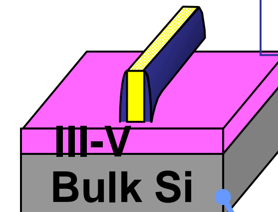
III-V

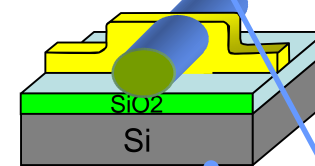
III-V FinFET

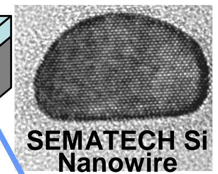
Nanowires

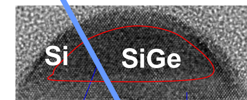
Graphene







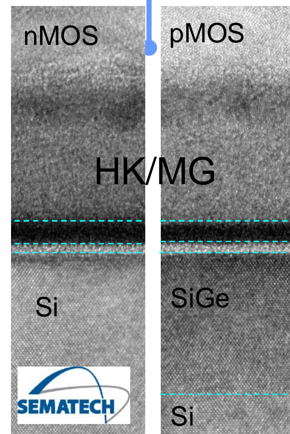


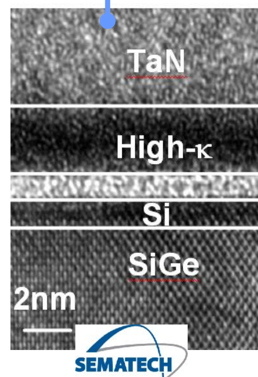


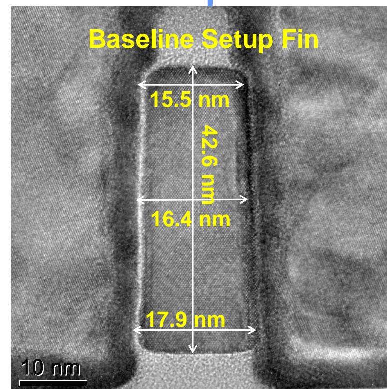
SEMATECH has CMOS HKMG solns

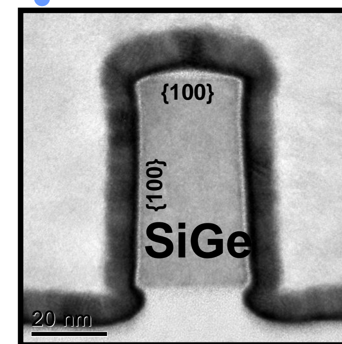
3X Si mobility with hi Ge % epi QW; dual silicides

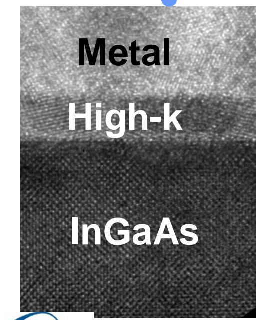
Si, SiGe finFETs with good SCE control











Collaborative Approach

SEMATECH developments
Comprehensive characterization

electrical

physical

modeling

electrical:
- U. Florida
- NIST
- U. Twente, Holland
- NJIT
- Bose State U.
- CNR, Italy
- U. of Sheffield, UK
- Yale U.
- UT-Austin
- Vanderbilt U.
- IIT, India

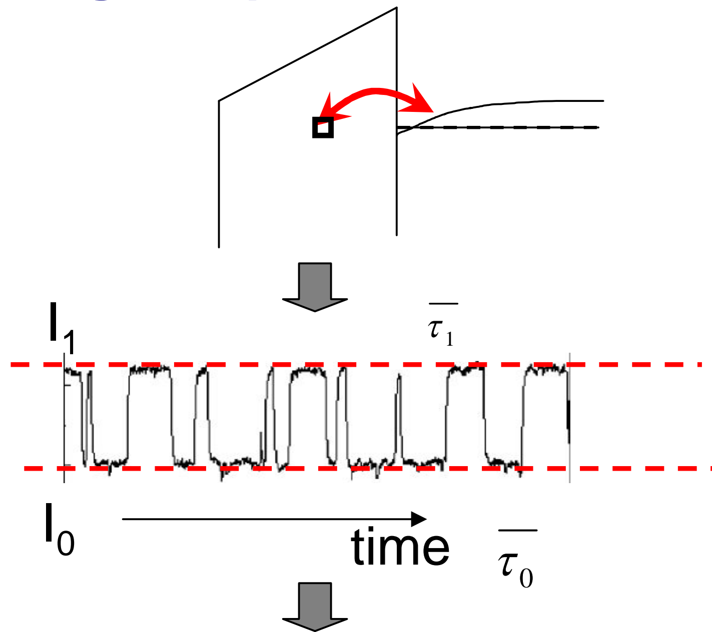
physical:
- ORNL
- UCSB
- Rutgers
- Penn State
- UT-Dallas
- NCSU
- Brookhaven NL
- UC-Davis

modeling:
- Univ. College London, UK
- UT-Austin
- UT-Dallas
- Glasgow U., UK
- U. of Modena, Italy
- NIST

1/f noise and RTS

Fluctuations of drain (gate) current in MOSFETs are caused by fluctuation of number and mobility of inversion carriers due to their capture/ emission by traps in oxide. RTS is observed in small devices

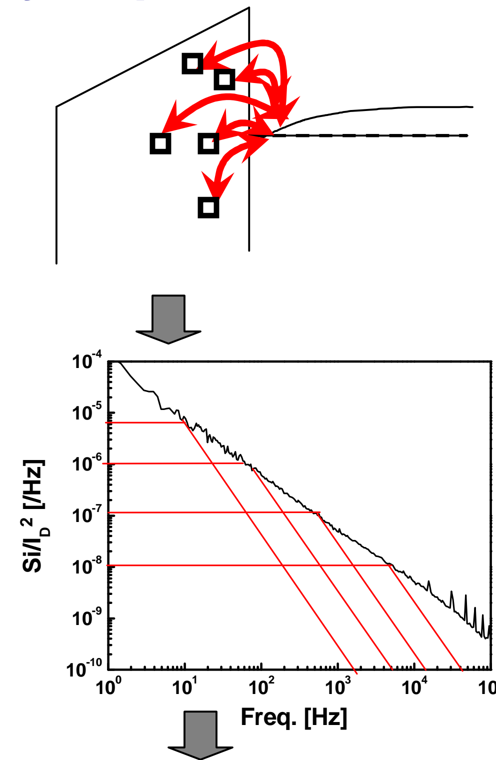
Single trap - RTS:



Noise power spectral density is Lorentzian:

$$S_I'(f) = \frac{\tau'}{1+(2\pi\tau \cdot f)^2} \; ; \; \tau = \frac{\overline{\tau_0}\,\overline{\tau_1}}{\overline{\tau_0}+\overline{\tau_1}}$$

Many traps -1/f noise:



$$S_I(f) \propto \int_0^{\infty} d\tau \times g(\tau) \times S_I'(f) \propto \frac{1}{f}$$

16 NA · IEEE SPECTRUM · AUGUST 2009

Future of Low-Power Chips in Doubt

Big flaw found in transistor noise theory

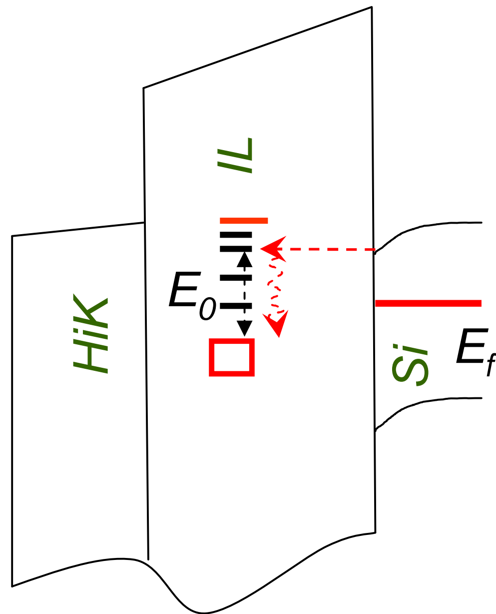
ENGINEERS AT the U.S. National Institute of Standards and Technology (NIST) say that the basic theory explaining the origin of a certain type of noise produced by very small transistors is totally wrong.

. He expected to see tunneling that took nanoseconds to picoseconds. Instead, the process took the milliseconds to seconds you'd see in a much bigger transistor. "What people thought is very likely not correct,"

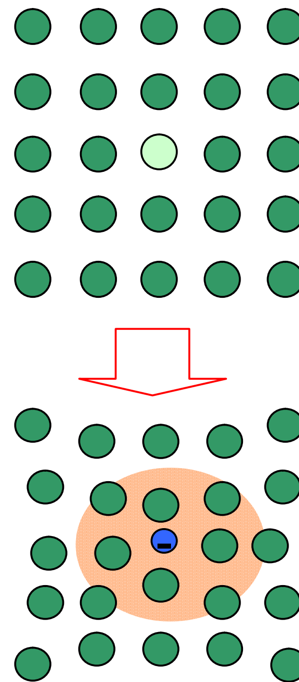
We think we have a solution…

Electron transport in dielectrics: trapping and trap relaxation

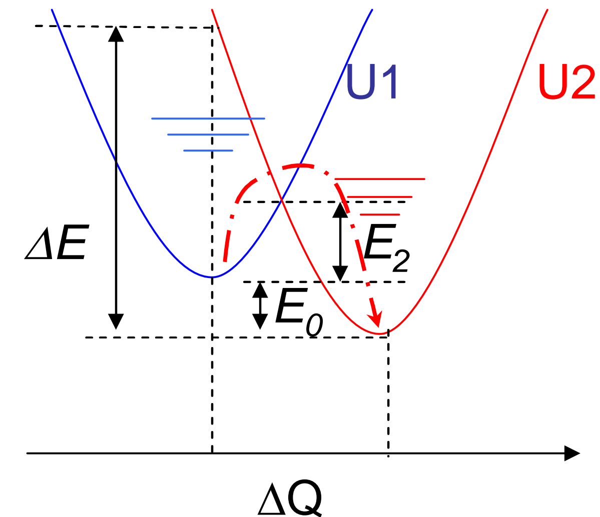
One electron description does not include relaxation



Lattice relaxation due to electron capture



Total energy description which includes relaxation



Capture probability:

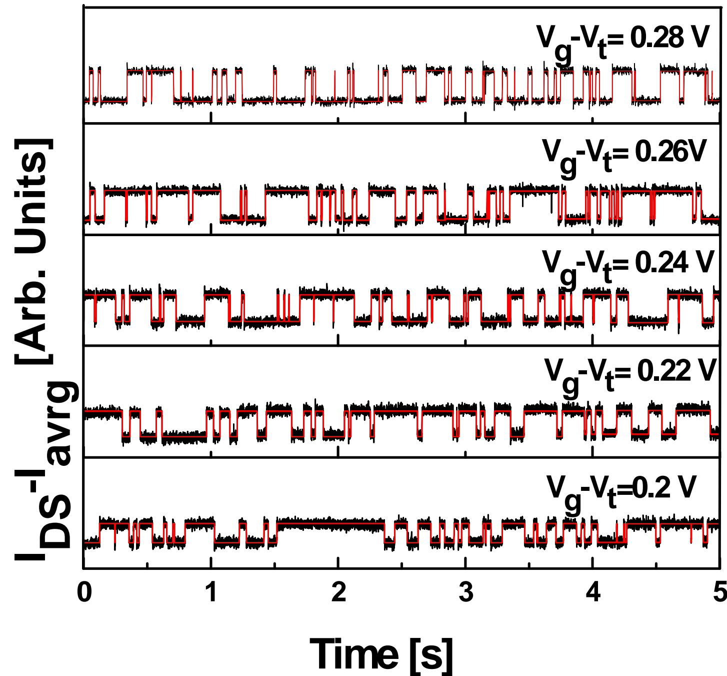
$$\frac{1}{\tau_c} = f_{imp} \times n_s \times T[0, F_{ox}, x_T] \times \sigma_0 \times a$$

Trap relaxation factor

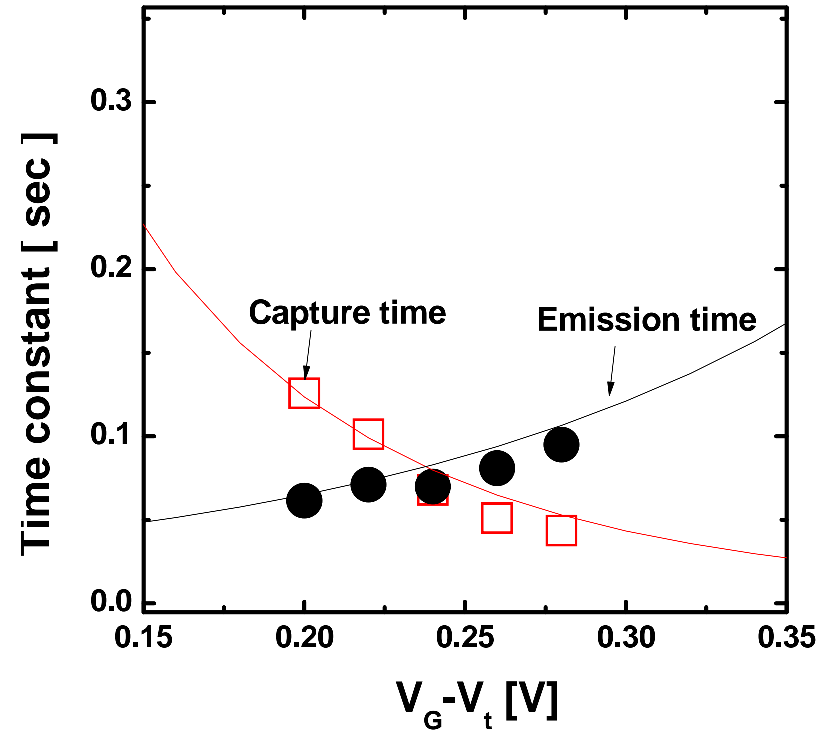
$$a = e^{-(2\bar{n}+1)S} \sqrt{\left(\frac{\bar{n}+1}{\bar{n}}\right)^p} I_p\left(2S\sqrt{\bar{n}(\bar{n}+1)}\right) \qquad S = \Delta E / \hbar\omega \qquad p = E_0 / \hbar\omega \qquad \bar{n} = \frac{1}{e^{\frac{\hbar\omega}{kT}} - 1}$$

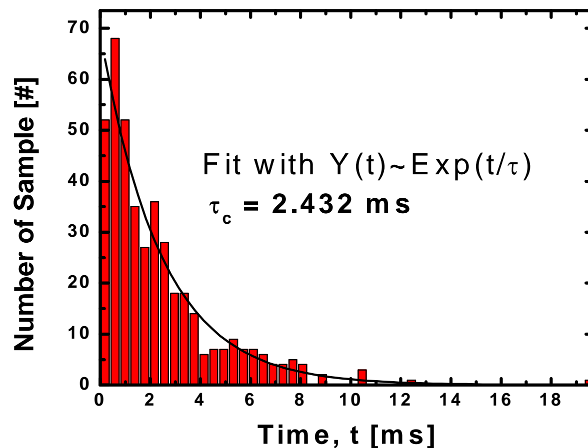
Simulating RTN in high-k stacks

W/L=0.3µm X 0.1µm,
Gate stack: 1nm SiO_2, 3nm HfO_2, TaN



Extraction of Capture/Emission times

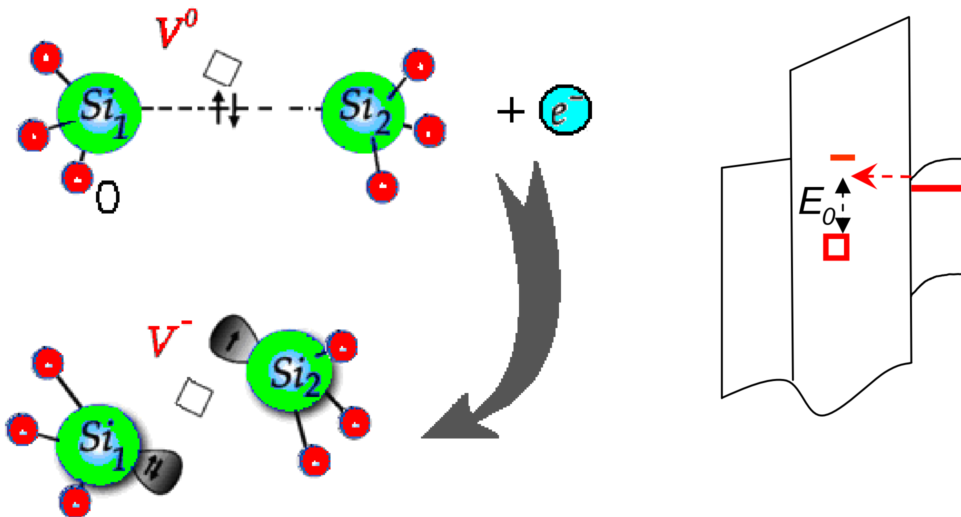




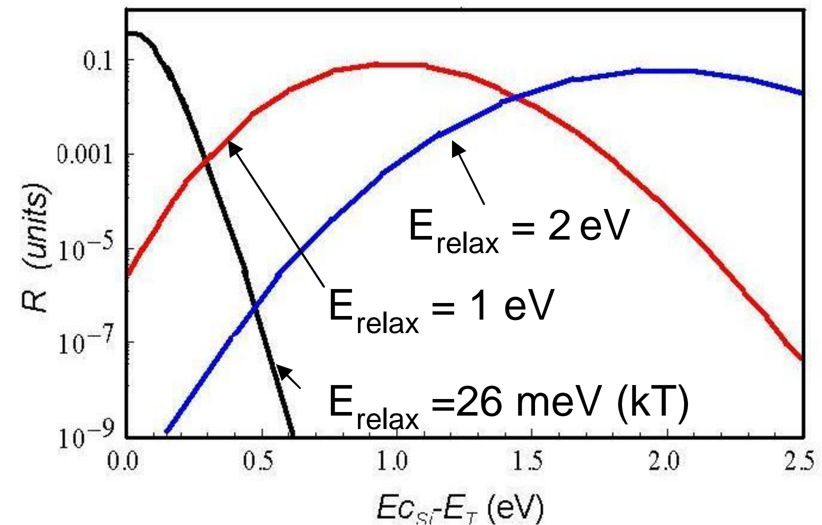
***E_T*=3.02 eV**
***x_T*=0.63 nm**
capture cross-section σ_0=1.3 10^{-14} cm^2,
geometric relaxation energy *E_{relax}* =1.86 eV

D. Veksler et al, IRW'09

Role of trap relaxation in electron capture process



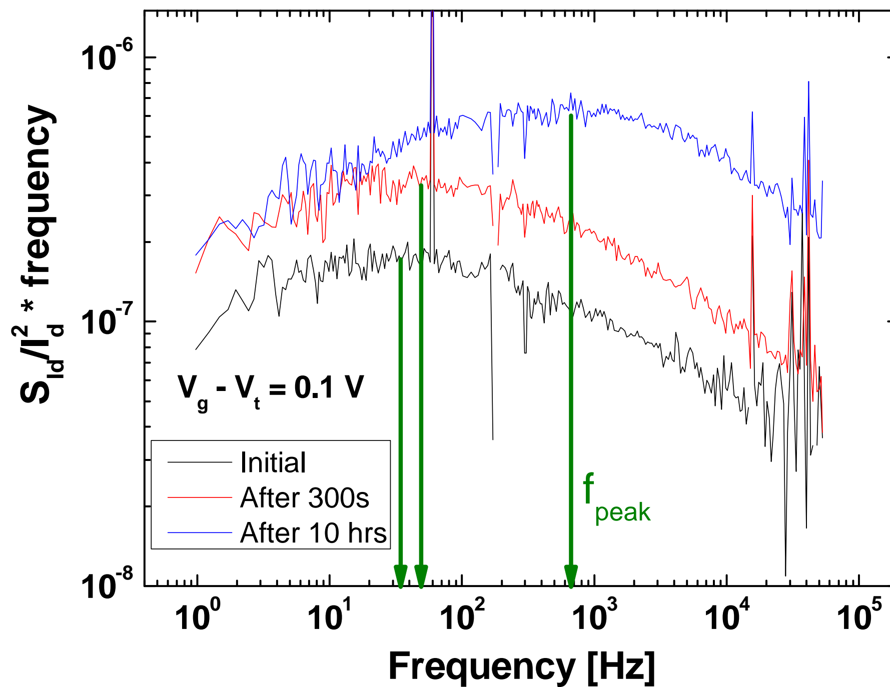
Multi-phonon relaxation factor vs. trap energy



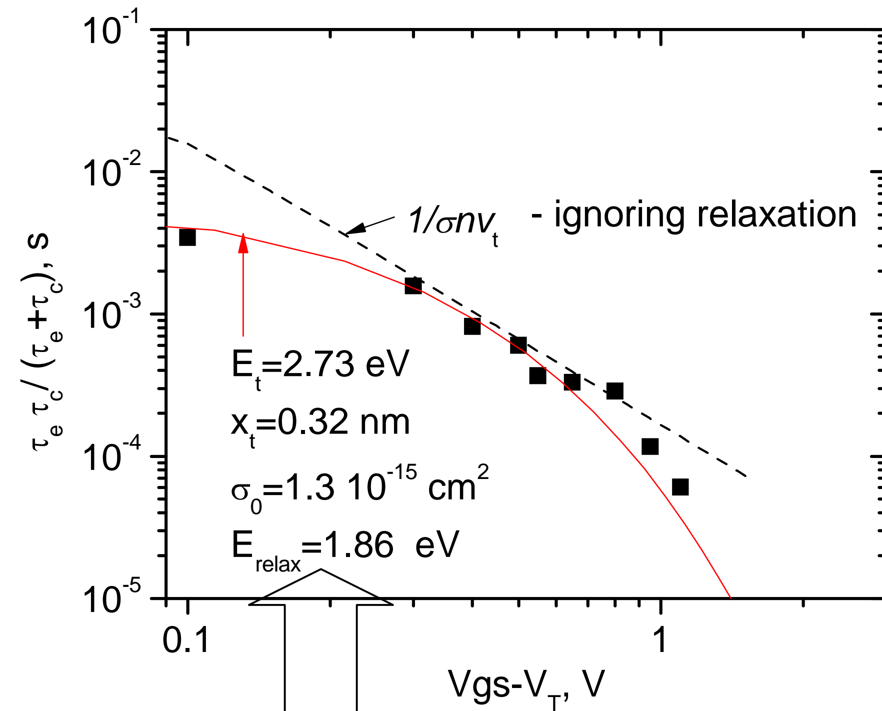
Transformation of V^0 into V^- by trapping an electron is accompanied by significant structural relaxation. (E_{relax} 1.5 – 2 eV)

Mismatch between relaxation and trap (E_0) energies exponentially reduces trapping probability

1/f Noise in High-k/Metal Gate Devices



f_{peak} gives the time constant associated with a trapping event allowing for extraction of the traps parameters.



Trap parameters are identical to those obtained from RTS

Trap is located in SiO_2 interfacial layer

RTS below threshold voltage: the role of interfacial states

E_t

1step

Ef

Metal

Si

Vg>Vt

E_t

2 step

Metal

Si

Vg<Vt, $\tau_{capture1}$ ↗

E_t

1

2

Ef

Metal

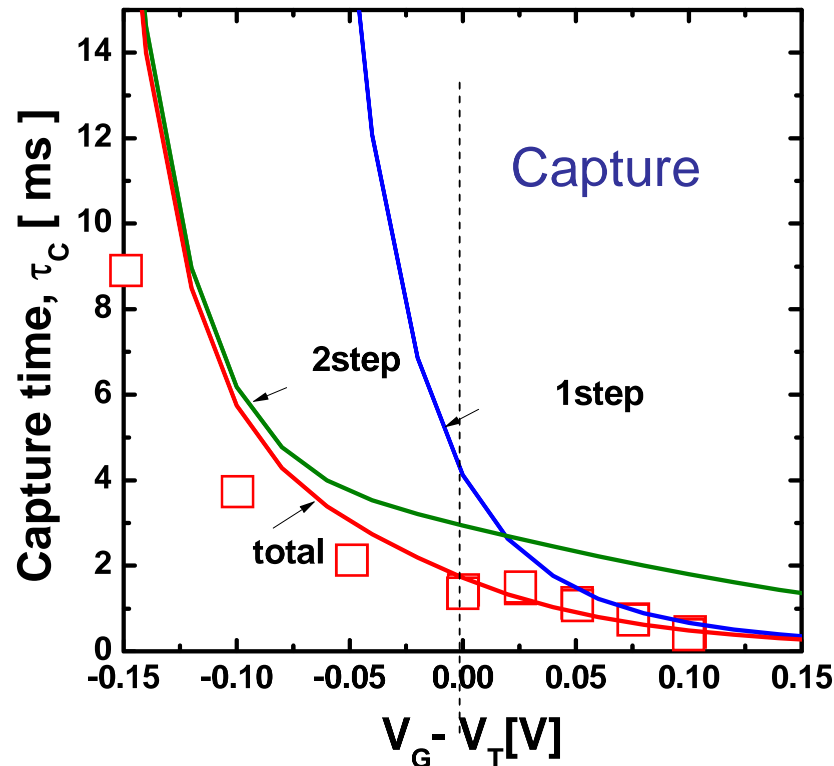
Si

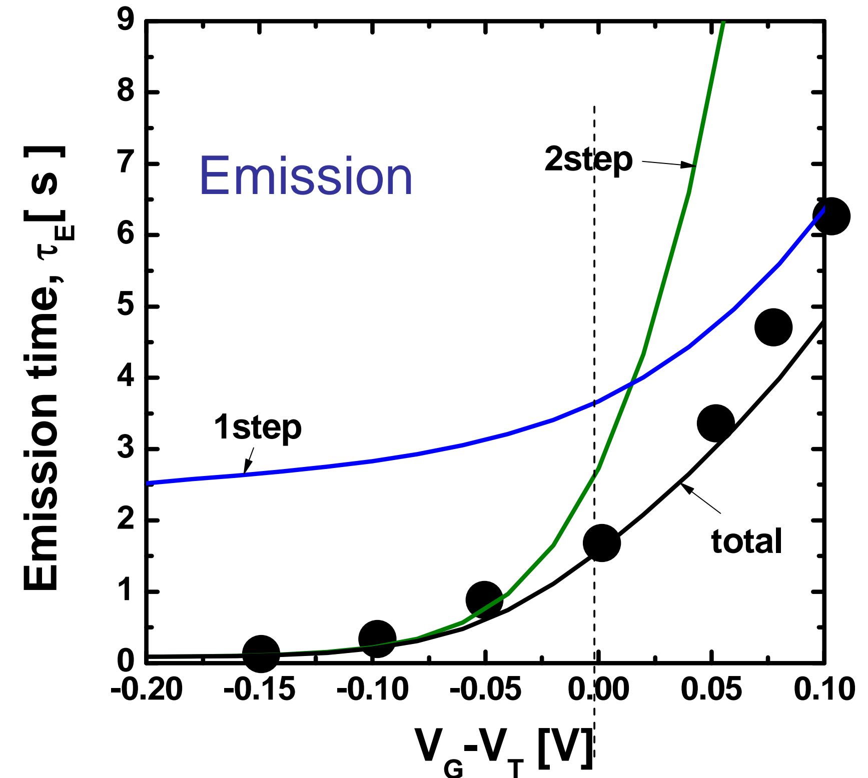
combined

$1/\tau_{capture} = 1/\tau_{1step} + 1/\tau_{2step}$

RTN in 1.4nm SiON/Poly-Si Gate Stack

Experimental data from: J.P. Campbell et al, IRPS'09

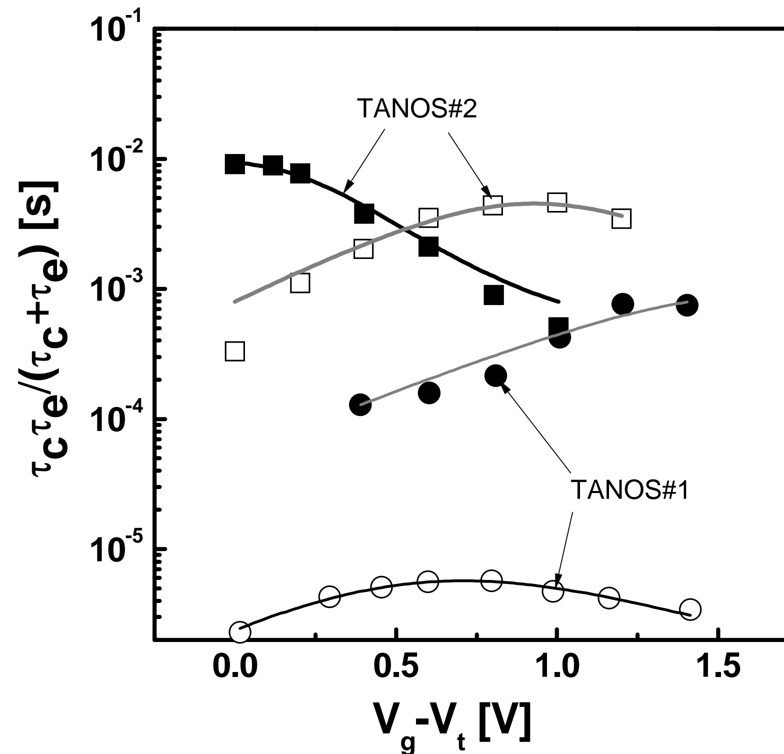




- 2-step model reproduces data *both below and above the threshold* - assuming no significant relaxation at interface state and its spatial alignment to the bulk oxide trap
- *Trap parameters are identical to those of traps located in SiO_2 interfacial layer in high-k stack*: E_T=3.3 eV, x_T=0.4 nm, σ_0=1.6 10^{-14} cm^2, S=33

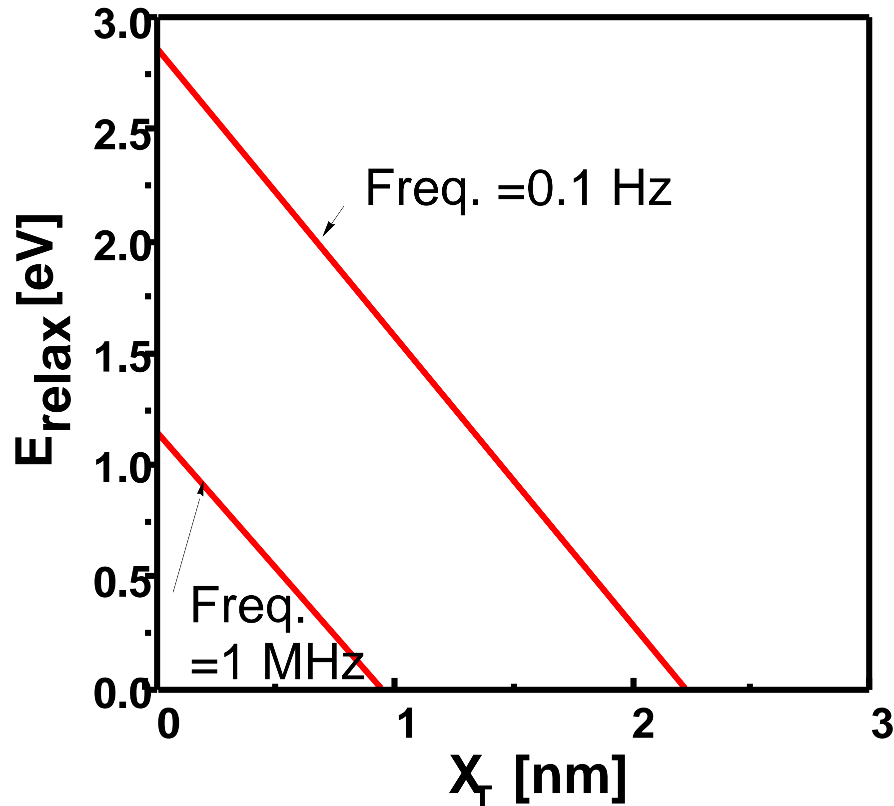
Traps in Tunnel Oxide in TANOS

$$\tau_c \tau_e / (\tau_c + \tau_e) = 1/2\pi f_{corner}$$



Open symbols stand for the pre-existing traps. Filled symbols designate stress induced traps.

Which traps can contribute to noise?

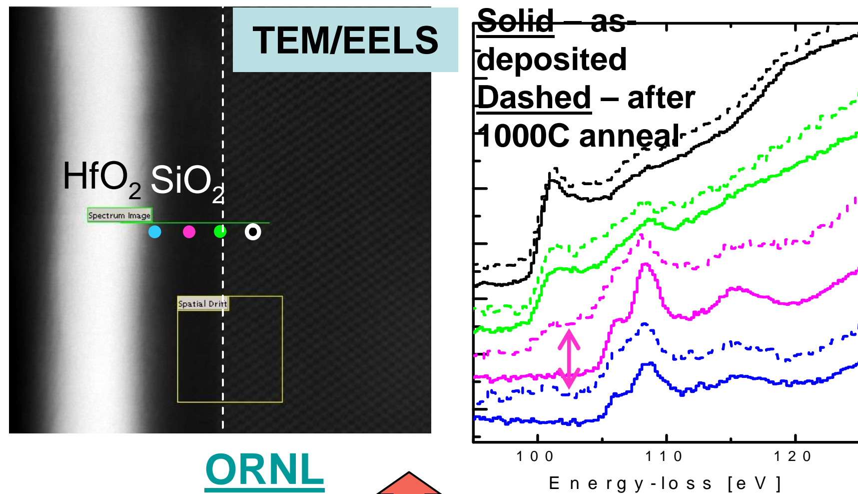


Correlation between relaxation energy and distance from substrate for the traps contributing to noise at a given frequency

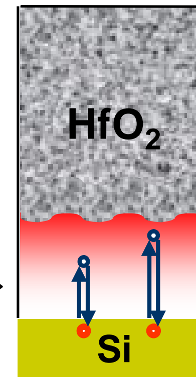
Example:
$\sigma_0 = 10^{-14}$ cm^2; $n = 10^{18}$ cm^{-3}
Shaded area identify the range of possible values of x_T and E_{relax} for traps detectable in the frequency range
0.1 Hz ÷ 1 MHz.

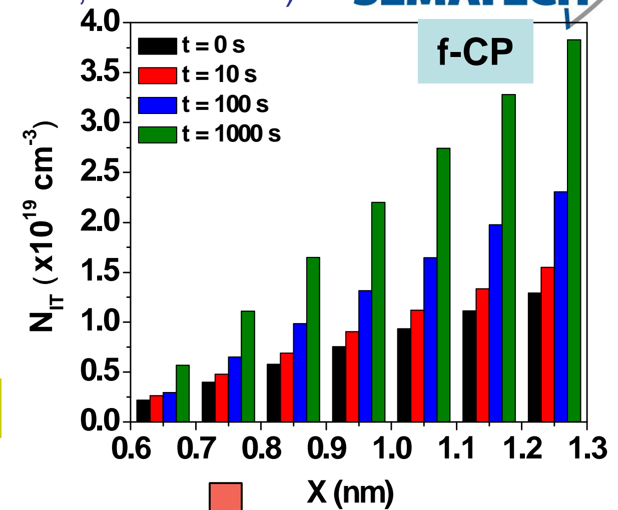
Physics-based mechanism for noise generation processes may lead to predictive noise simulation modeling

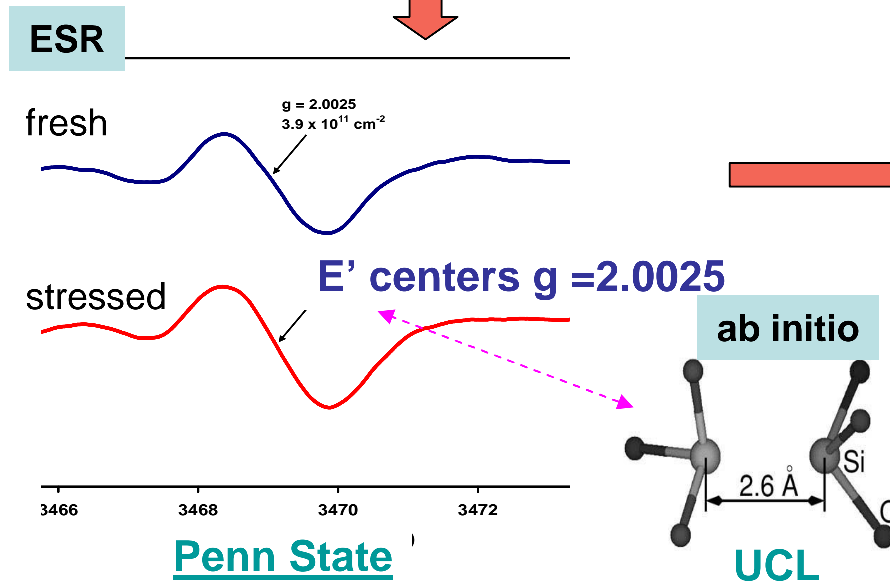
SILC mechanism in high-k stacks: oxygen deficiency of interfacial SiO_2 layer (Bersuker, IEDM 2008)



ORNL







Penn State

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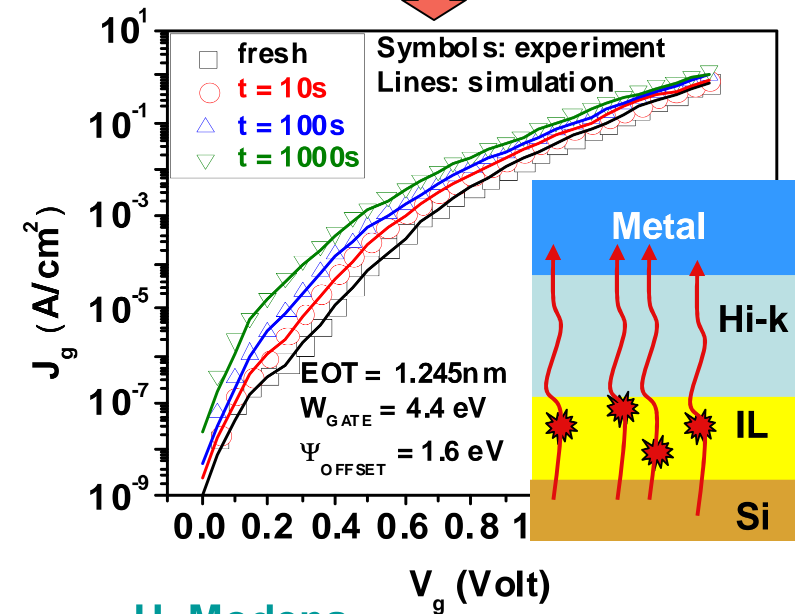
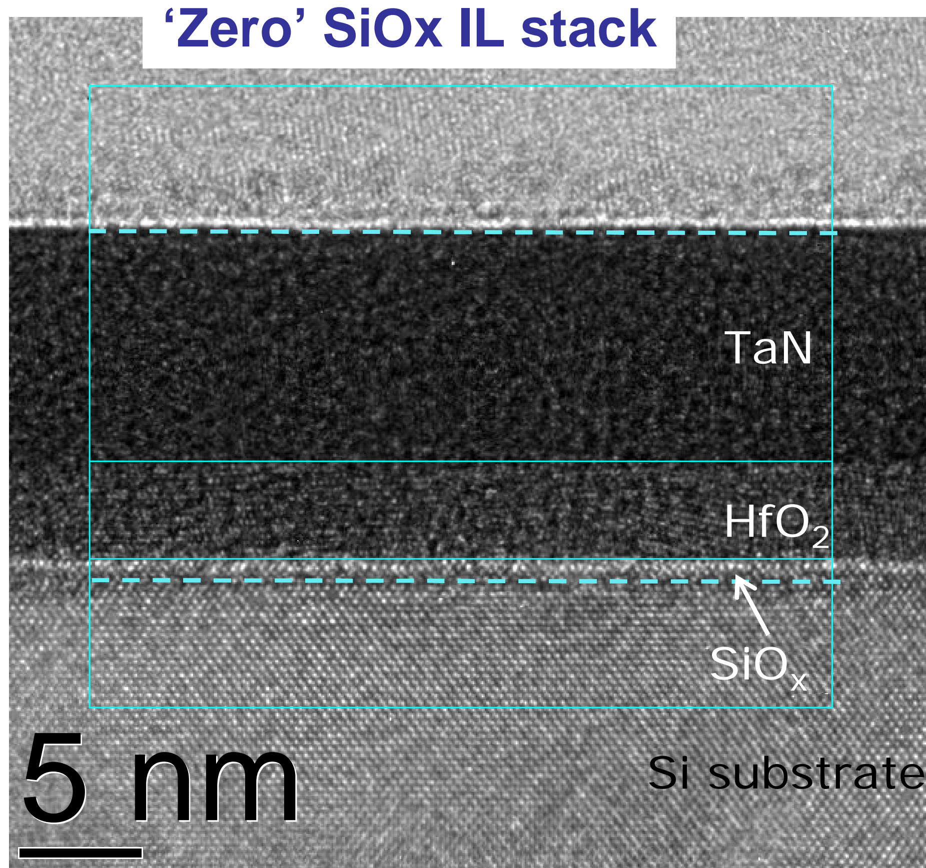


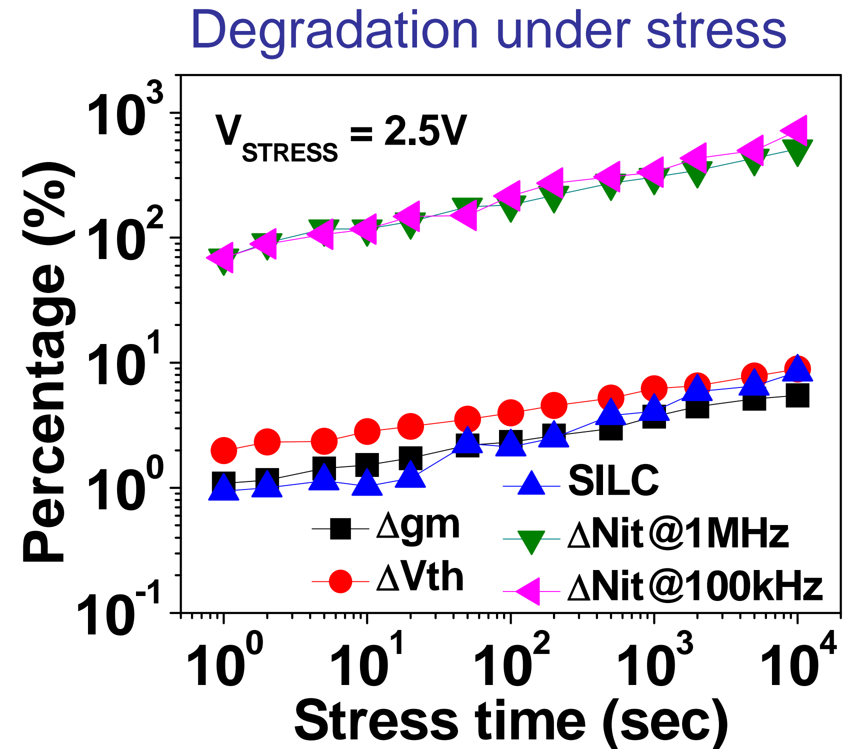
U. Modena

SILC simulation in high-k dielectric stacks with ultra-thin IL → the model still works?



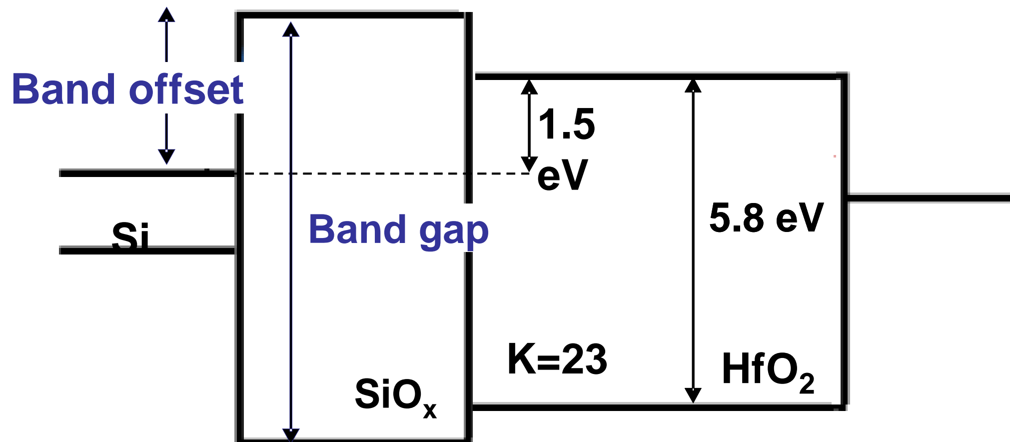
EOT=0.6 nm

Degradation under stress

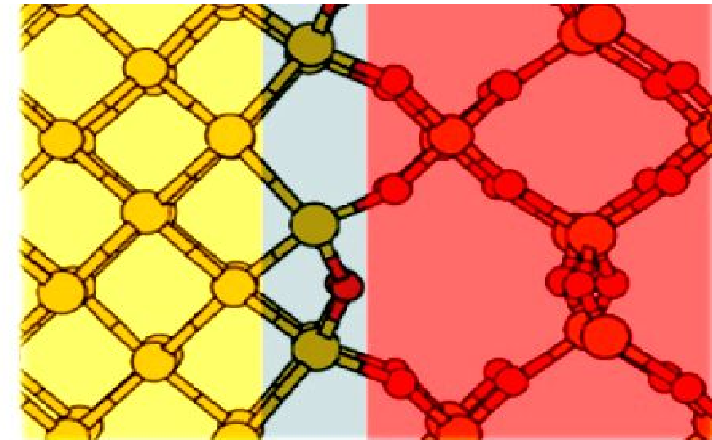


Similar slope for all parameters suggests that instability is dominated by the interface degradation

SILC Simulation: Energy Band of Thin Interfacial SiOx Layer

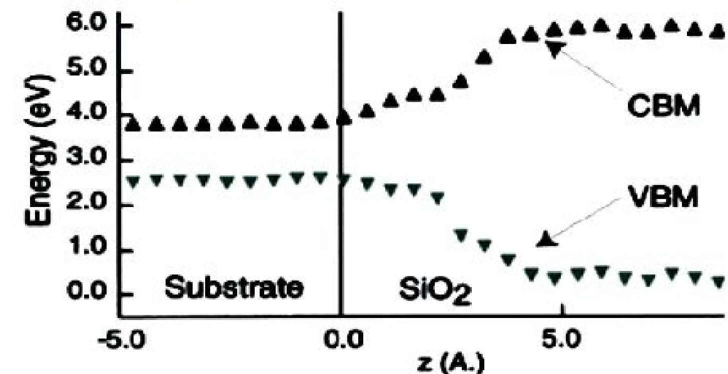


L. Larcher, U.Modena



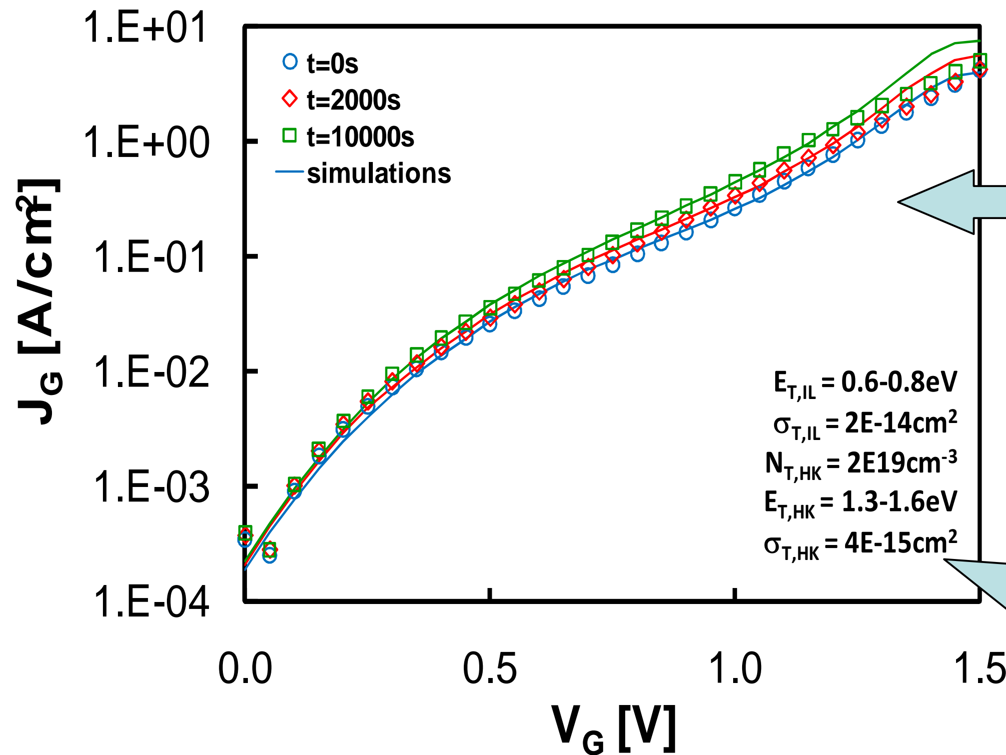
Zero-IL samples

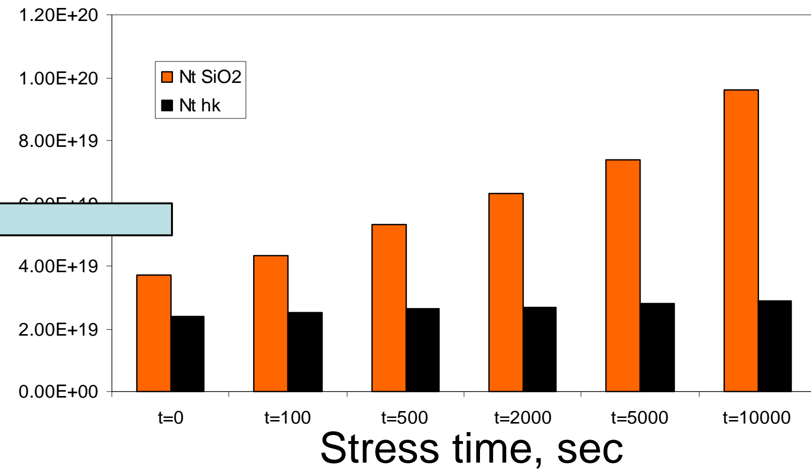
SiOx IL	3A (w/ 4nm HfO2)	5A (w/ 2nm HfO2
Band offset	1.3	2
Band gap	4.3	6.3
K-value	9	7.5
Total EOT	0.8	0.6

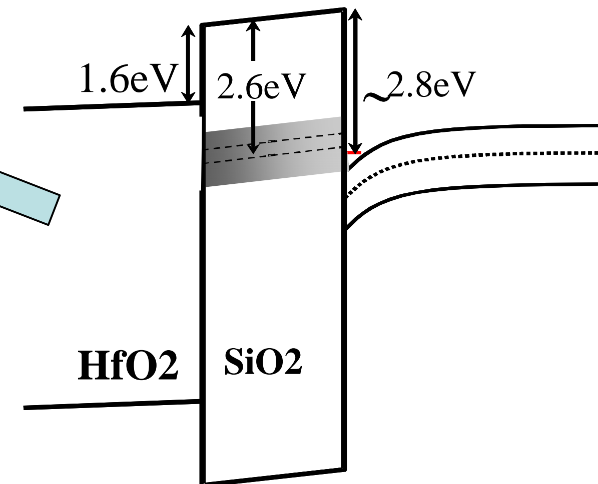


Gradual increase of band gap with SiO_2 thickness

Model verification: SILC simulation based on earlier extracted defect characteristics

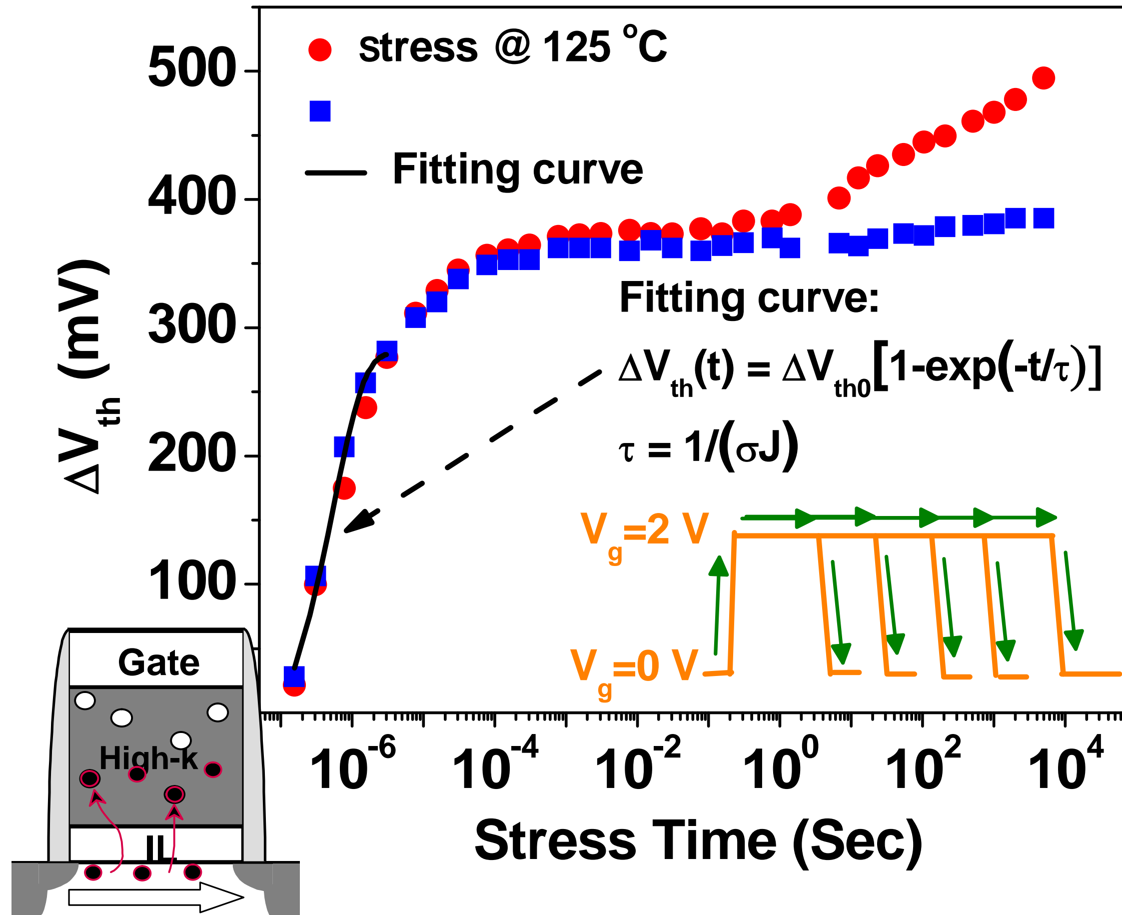






Predictive SILC simulation is possible!

Fast V_t instability: Accounting for fast trapping processes in high-k dielectrics



Extracted defect parameters:

Characteristic time

$\tau \sim 0.5\ \mu s$

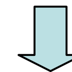
Trap capture x-section

$\sigma \sim 10^{-13}\ cm^2$

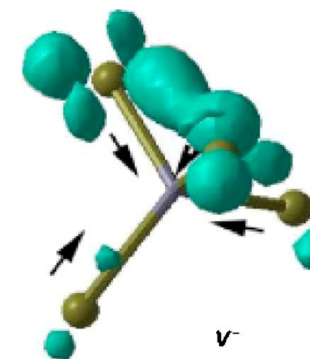
Trap density

$\geq 10^{13}\ cm^{-2}$

Energy ~ 0.5 eV



O-vacancies in m-HfO_2



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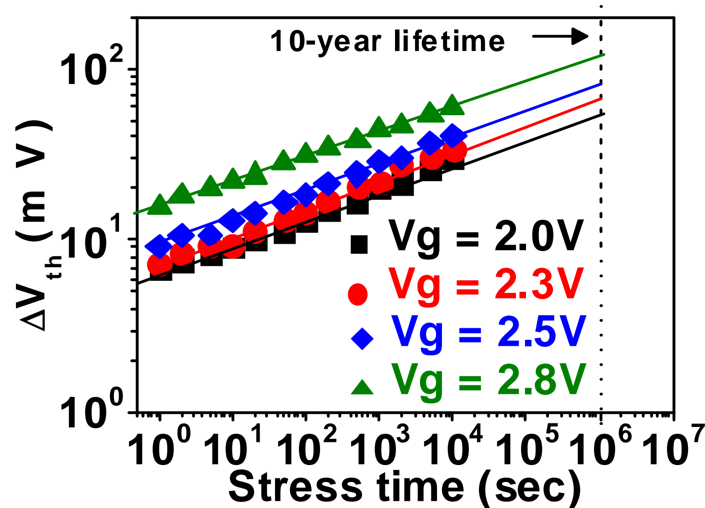
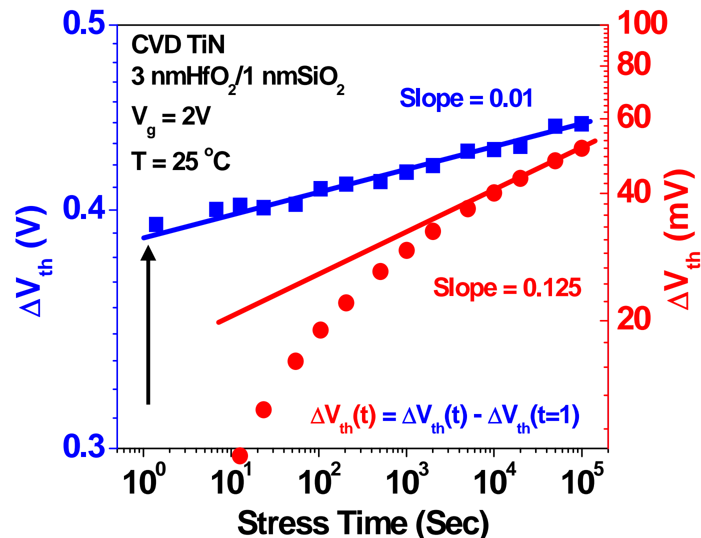
Reliability projections





- **Multi-layer, multi-component dielectric stacks**

  → Accelerated stress (high voltage/temperature) may activate additional degradation mechanism which <u>might not be relevant</u> under use conditions

  - PBTI model under development

- **High density of defects and defect precursors**

  → Fast transient effects may change reliability projection

Summary

- Mechanisms controlling device performance and reliability can be identified by combining electrical, physical and modeling methods
  → collaboration between characterization and modeling studies is critical to address challenges of future technology

- Physics-based models can successfully simulate evolution of device characteristics under operation conditions → may help to increase design margins