Compact Modeling of LDMOS Transistors for Extreme Environment Analog Circuit Design

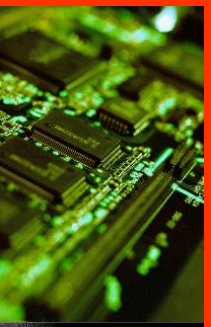
Avinash S. Kashyap, H. Alan Mantooth, Tuan Vo*, Mohammad Mojarradi*

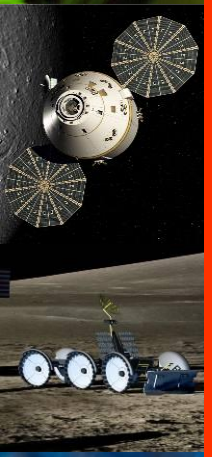
University of Arkansas, Fayetteville, AR
*Jet Propulsion Laboratory, Pasadena, CA

Outline

- Motivation
- LDMOS devices and characterization
- The MOS20 model and performance
- Cryogenic Model Development - New T-scaling equations
- Model validation
- Validating the model in a circuit configuration
- Conclusions

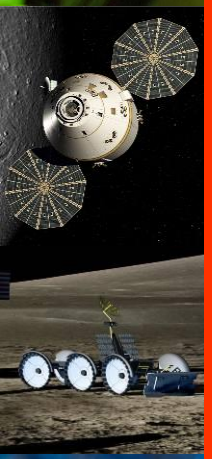
Motivation





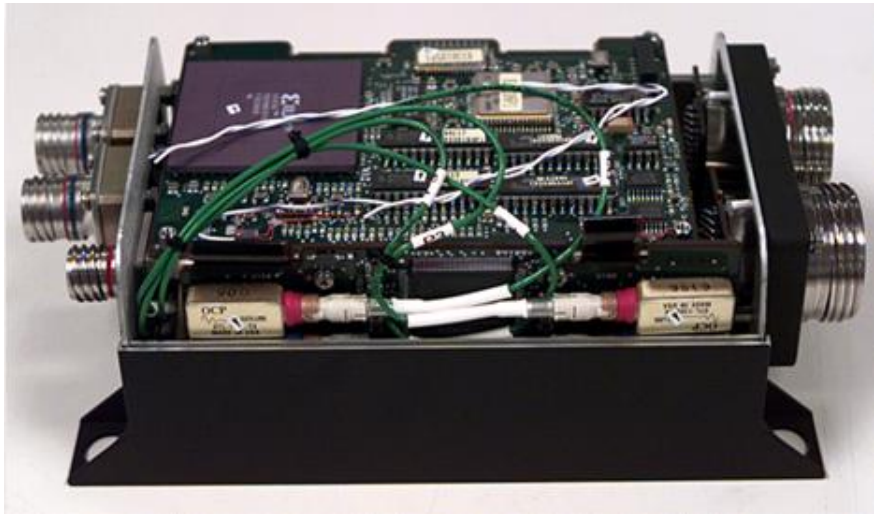
- Realizing analog circuit designs for Project Constellation (Ares series) – through a NASA ETDP consisting of universities and industrial partners
- One of the systems under consideration is a remote health monitoring node (RHN) to be placed all over the craft, keeping track of various parameters such as temperature, pressure, etc.
- Circuits should be capable operating in lunar environments from -180 ^{o}C to + 120 ^{o}C
- Specifically, this project pertains to studying, characterizing and modeling LDMOS devices (designed by JPL) used in the above circuits
- The model has to be T-scalable, i.e. one parameter set should replicate behavior for the entire operational range

SiGe ETDP Team

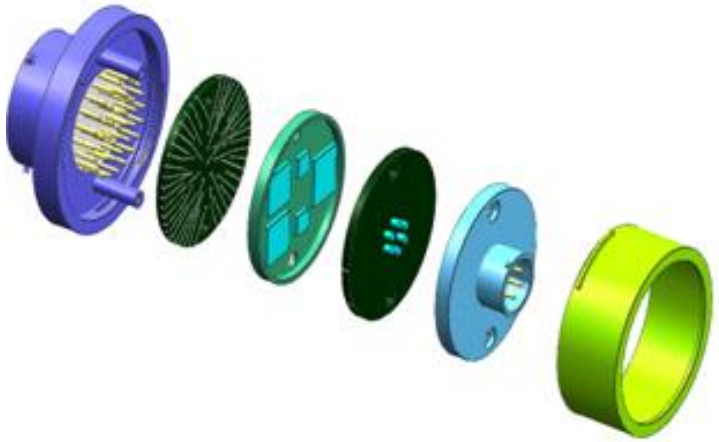



- **Georgia Tech** (Device Technology IPT lead)
  - John Cressler *et al.* (PI, devices, reliability, circuits)
- **University of Arkansas** (Modeling IPT lead)
  - Alan Mantooth *et al.* (modeling, circuits)
- **Lynguent**
  - Jim Holmes *et al.* (modeling and verification)
- **Auburn University** (Packaging IPT lead)
  - Wayne Johnson *et al.* (packaging); Foster Dai *et al.* (circuits); Guofu Niu (devices
- **University of Tennessee** (Circuits IPT lead)
  - Ben Blalock *et al.* (circuits)
- **University of Maryland** (Reliability IPT lead)
  - Patrick McCluskey *et al.* (reliability, package physics-of-failure modeling)
- **Vanderbilt University**
  - Mike Alles, Robert Reed *et al.* (radiation effects, TCAD modeling)
- **JPL** (Applications IPT lead)
  - Mohammad Mojarradi *et al.* (applications, reliability testing, circuits)
- **Boeing**
  - Leora Peltz *et al.* (applications, circuits)
- **BAE Systems**
  - Richard Berger, Ray Garbos *et al.* (REU architecture, maturation, applications)
- **IBM**
  - Alvin Joseph *et al.* (SiGe technology, fabrication)

Remote Health Node

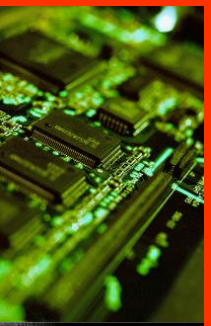
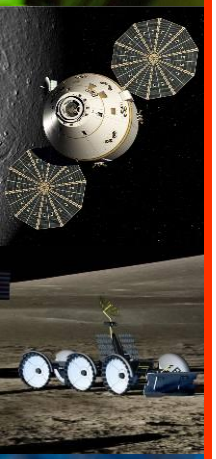


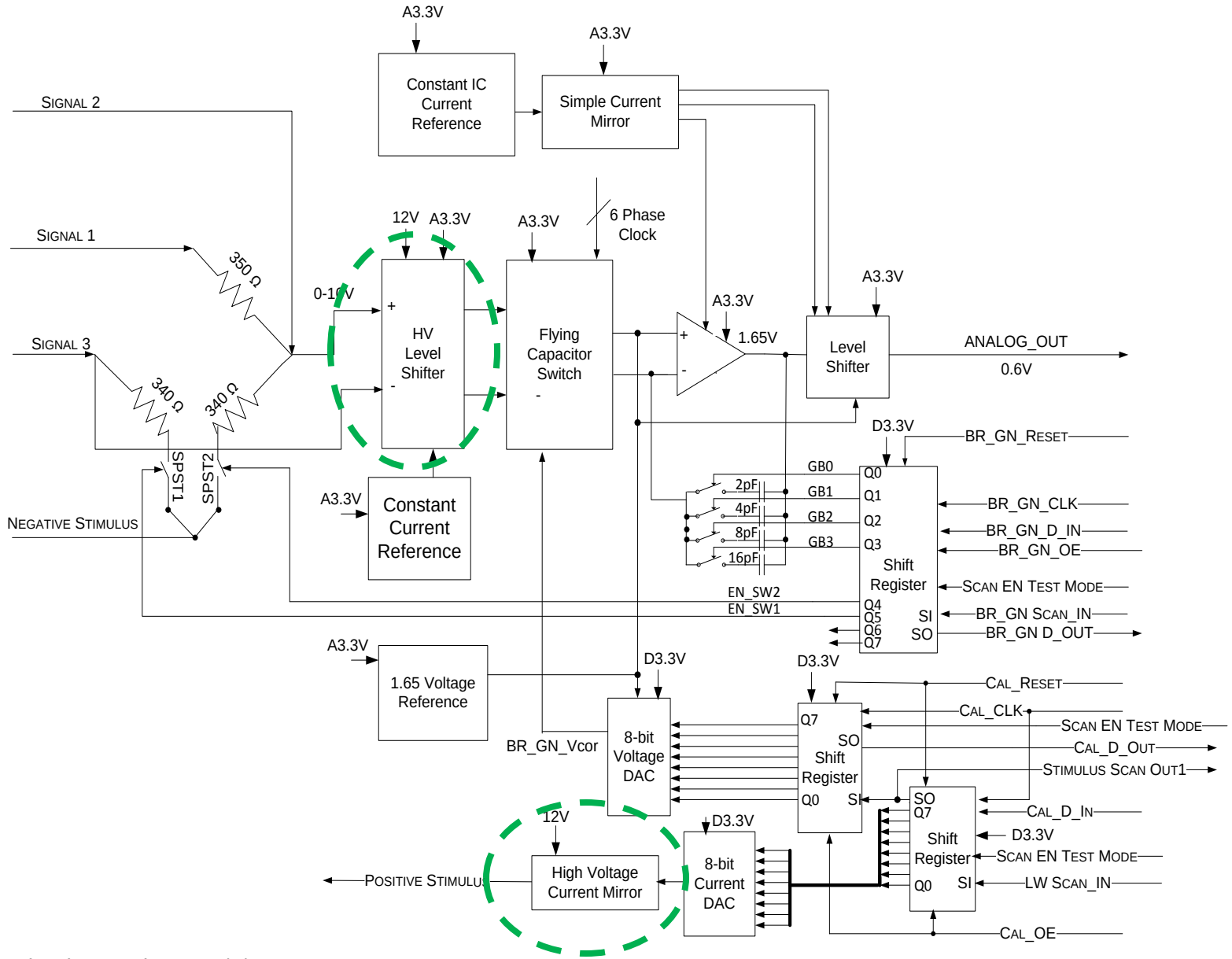
BAE's RHN developed for the X-33 project with COTS, weighing in at 11 kgs + auxiliary "warm box"



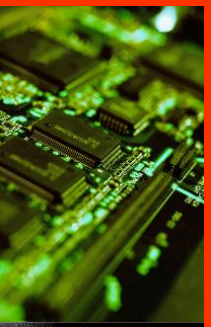
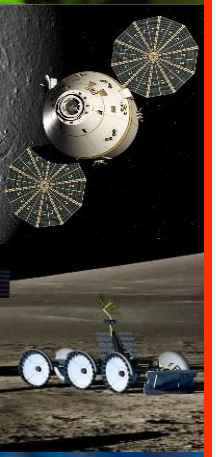
The proposed RHN from the ETDP, weighing only a few grams
100 X smaller
5X lower power consumption (120 mW)

Architecture of Low Speed Channel



Outline

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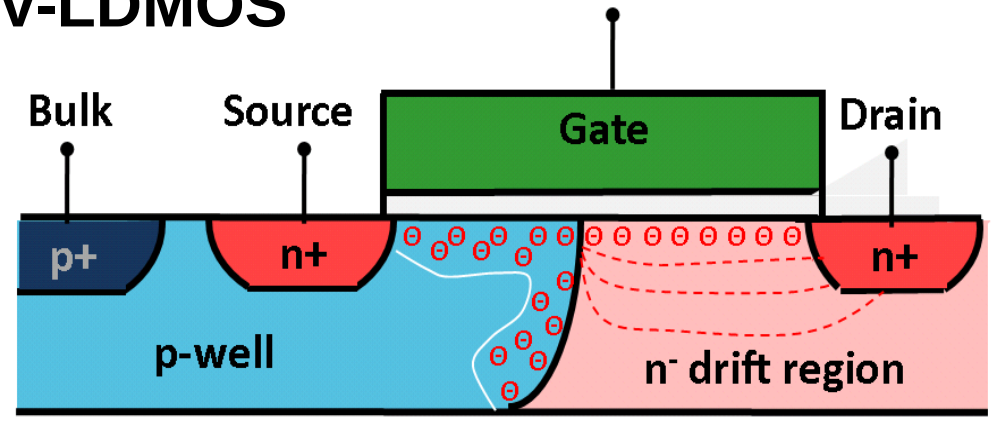
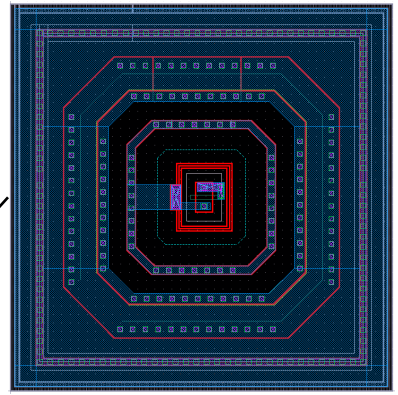
Introduction to LDMOS Devices

- Lateral structure aids in integration of the device with low voltage circuitry
- Used extensively in switch-mode power supplies, power amplifiers
- Applications in cell phone base stations, automotive circuits, consumer electronics, etc.
- Can be LV-LDMOS or HV-LDMOS, i.e. drain voltage can range between 12 V to 1200 V

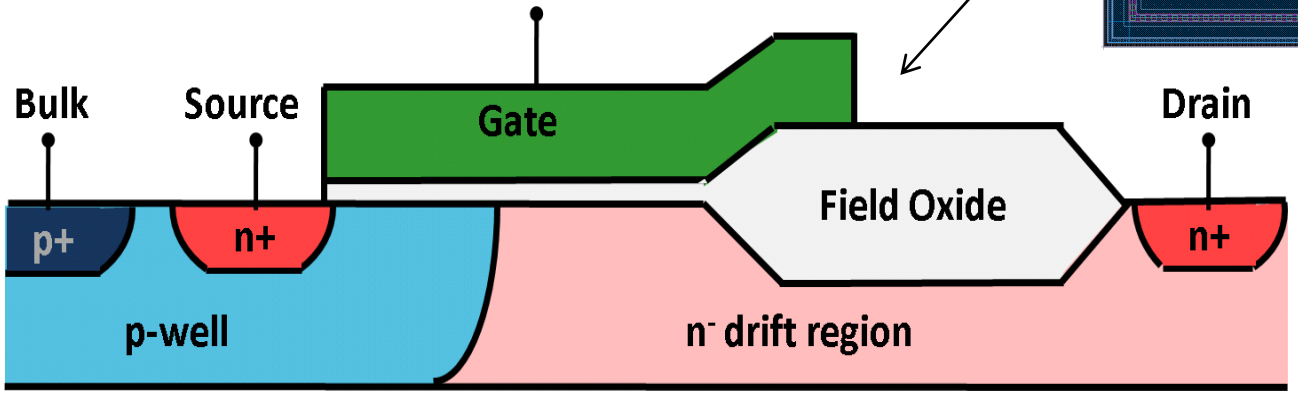
Device Physics

LV-LDMOS





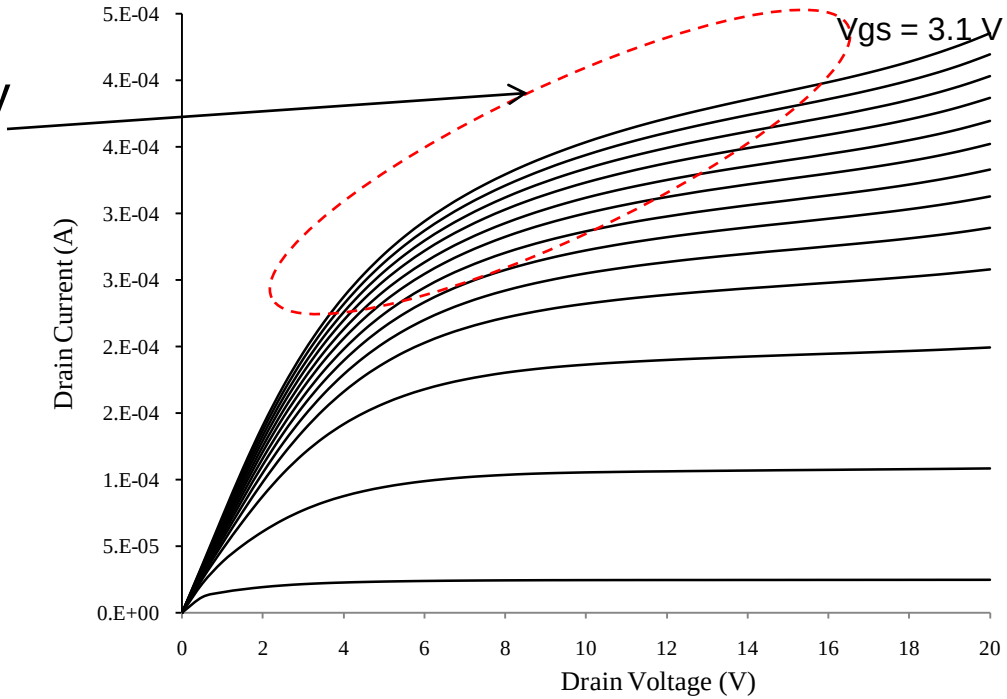
HV-LDMOS

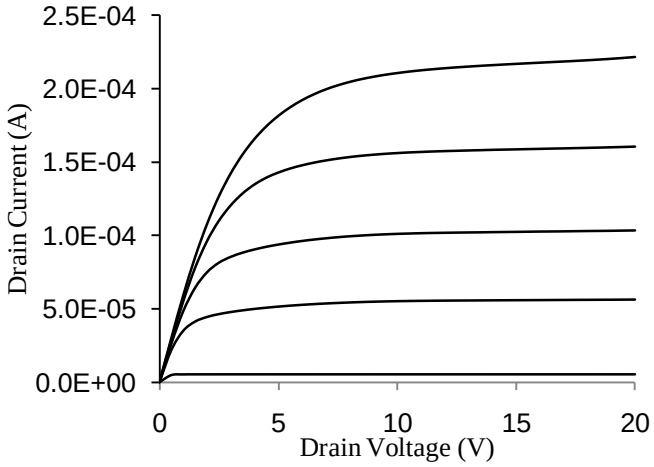


L = 2 u, W = 40.45 u, Ldr = 4.45 u

Quasi-saturation in the JPL Device

Quasi-saturation clearly seen for Vgs > 1.3 V

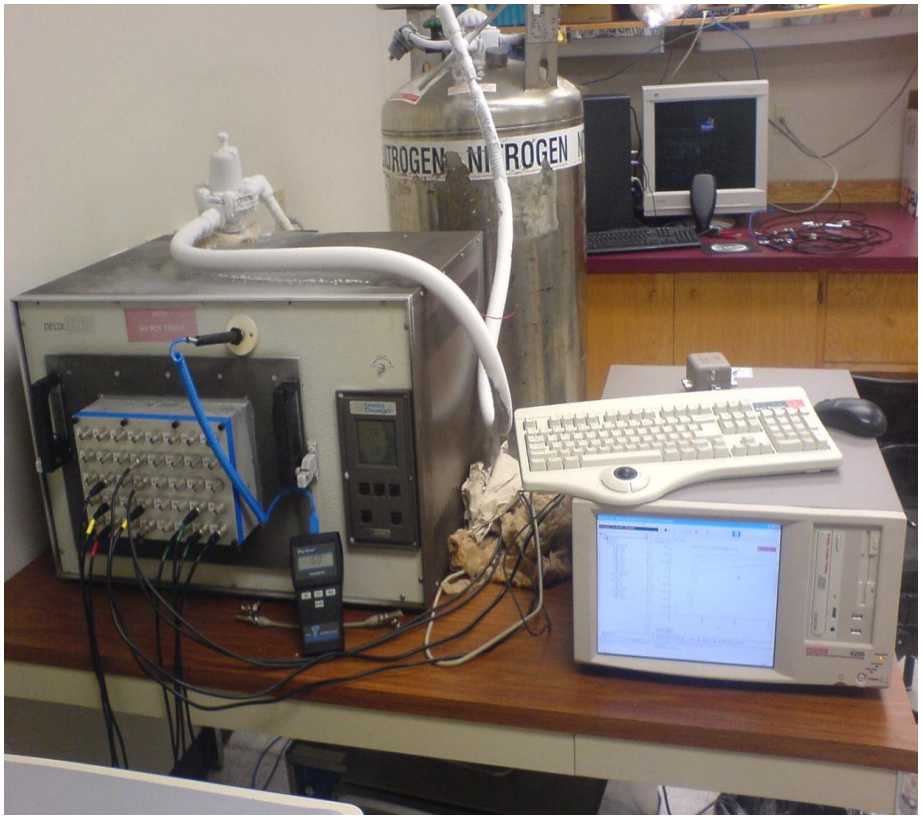




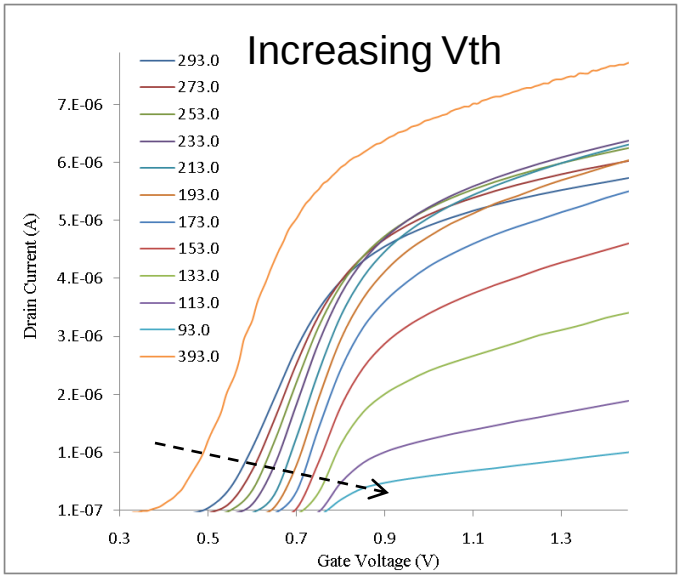
← No quasi-saturation seen for low gate bias (Vgs = 0.7 V – 1.1 V)

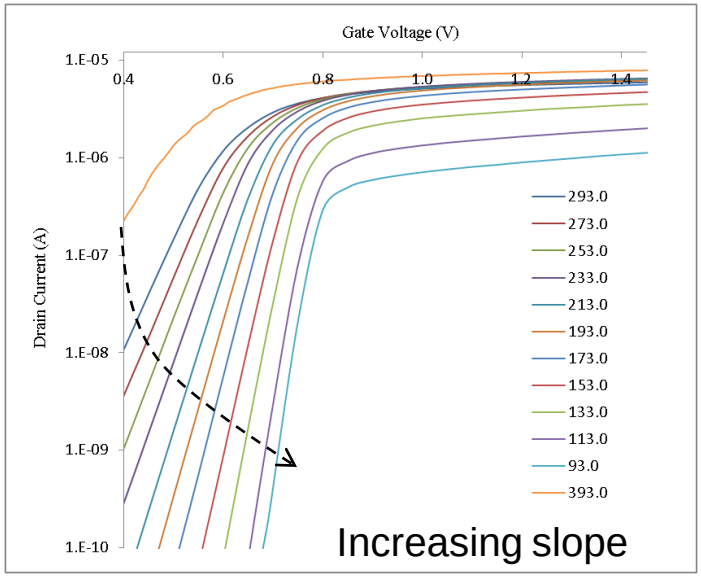
Cryogenic Characterization

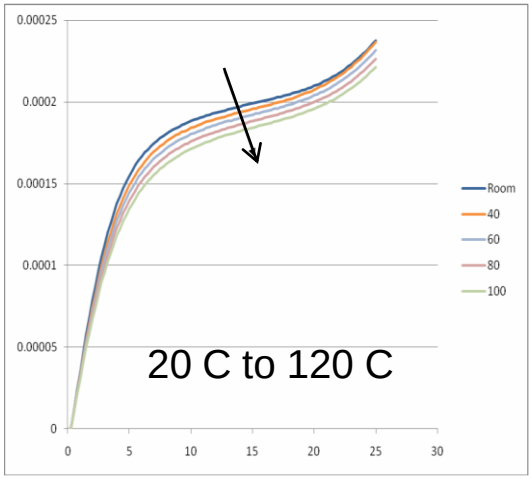
- Keithley 4200 system used for DC and CV measurements
- Cryogenic testing is performed in an environment chamber connected to liquid nitrogen @ 80 psi
- Cryo characterization performed down to -180 C in steps of 20 C

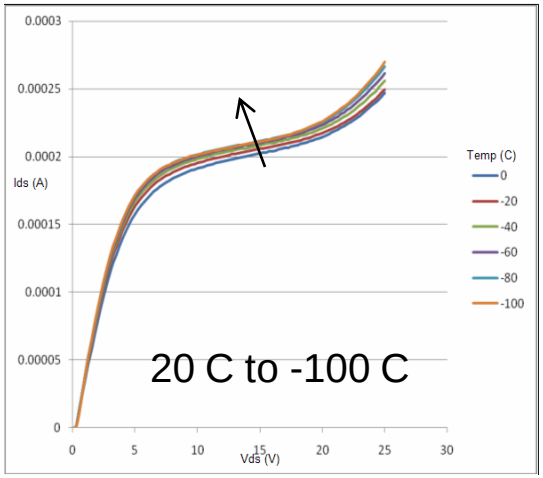


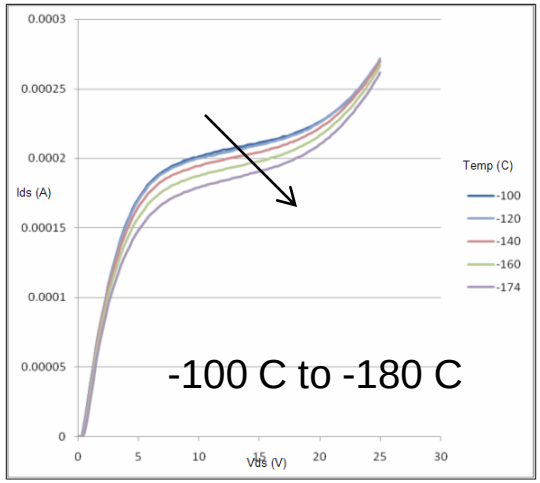
Input & Output Characteristics





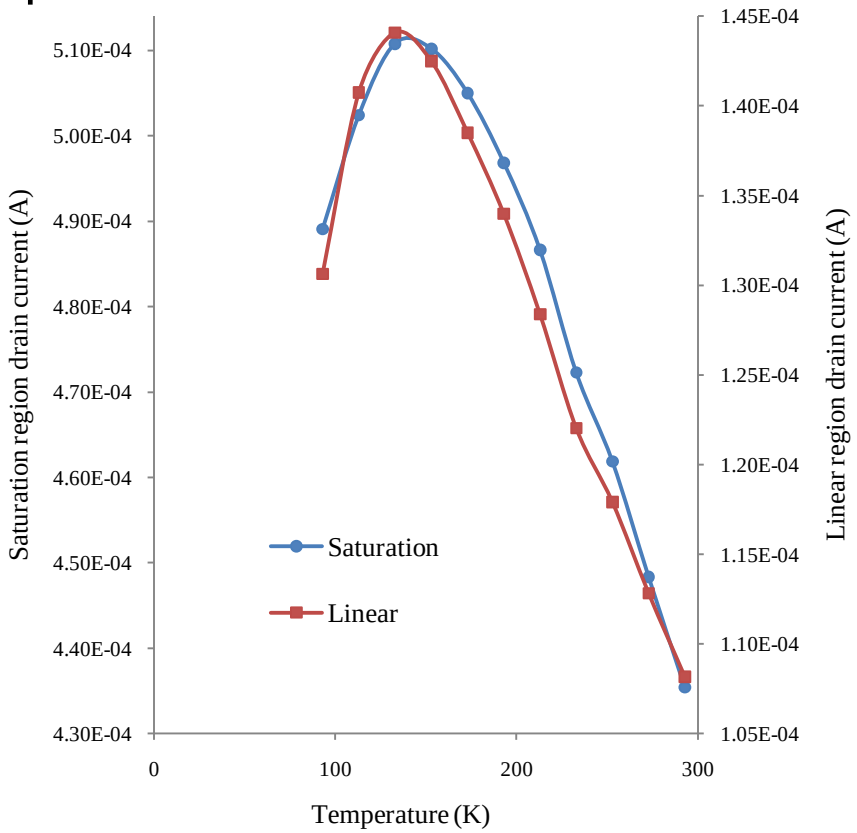






Anomalous output characteristics

Drain current at Vgs = 3.1 V and Vds = 2 V and 20 V for different temperatures

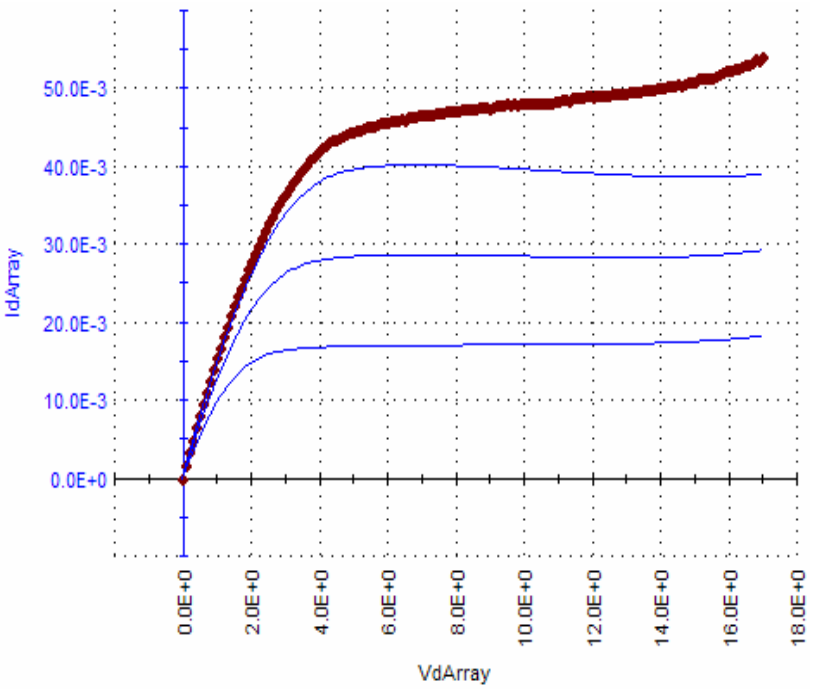


- Output current rolls off below 133 K
- Phenomenon not observed in MOSFETs until 20 K or below

Could it be self-heating?

- An important consideration in high voltage devices is self-heating
- But it is ruled out due to the following reasons:
  - No characteristic droop in current in higher drain biases
  - Current decrease seen in both linear and saturation regions, while self-heating limited to saturation region
  - Verified with pulsed measurements

Typical self-heating behavior in MOSFETs

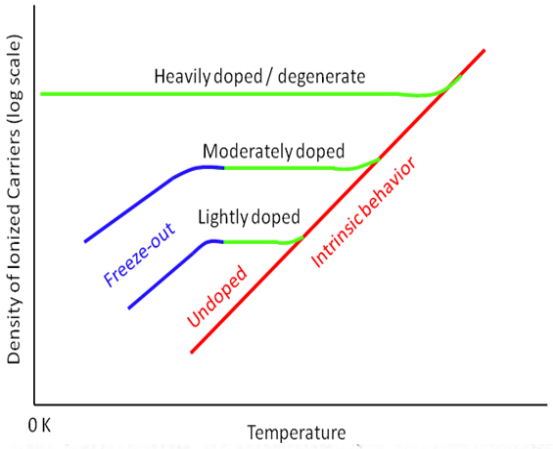


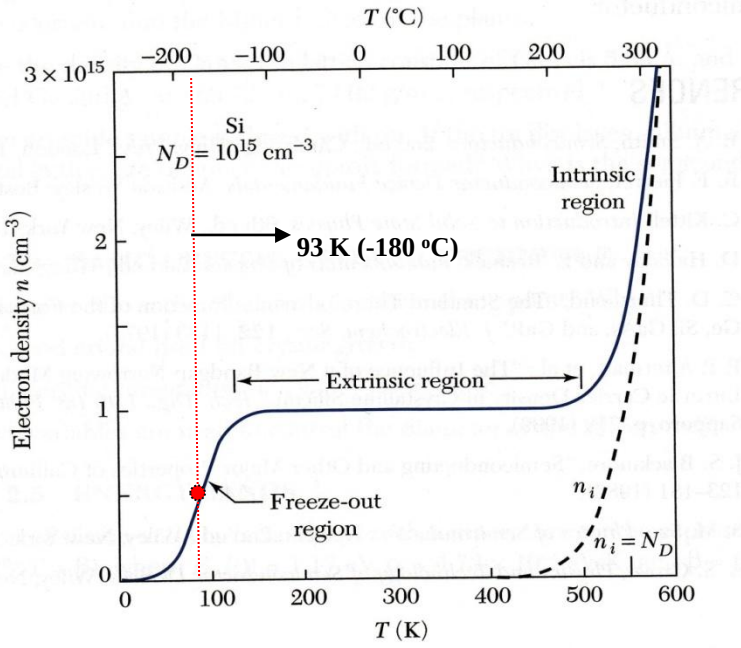
Blue – Normally measured device exhibiting self-heating
Brown – Pulsed device, no self-heating

Impurity freeze-out

- Postulated to be the carrier freeze-out phenomenon happening in the drift region
- Notice that lightly doped regions have much lower number of ionized carriers and also freezes-out at higher temperatures

Carrier behavior with temperature





Impurity freeze-out

- Si MOSFETs and CMOS circuits are often used at deep cryogenic temperatures, below the freeze-out of Si (< 40K)
- But in LDMOS devices, the gate's electric field is shielded from the drift region, which is doped low to start with
- This creates a lower ionization of carriers in the drift region as the temperature is decreased and therefore it can be seen that current considerably decreases after a transition temperature
- This poses a risk to circuits operating with LDMOS devices as they have the propensity to completely freeze-out and not operate in temperatures considered operable to normal MOSFETs

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LDMOS Modeling

- LDMOS modeling is an active research area
- Traditionally, sub-circuit approach was used for LDMOS modeling
- BSIM3 core + external resistor in series for drift region
- Disadvantages
  - Model fails under various conditions
  - Parameter extraction strategy complicated
  - Model behavior can be non-physical
  - BSIM3 like models can be unwieldy and not favored anymore
- Other models such as Level 66, EKV, Hi-Sim considered
- NXP's MOS Model 20 chosen

MOS20 Model - Equations

- The temperature scaling equations in the MOS20 model are purely empirical consisting of relations that are either linear extrapolations or simple exponentials
- Scaling is performed by processing the parameters used in the core model rather than directly incorporating temperature coefficients in the core model equations
- This makes it easier to :

  (a) understand the model behavior

  (b) sort through parameters that need modifications and those that do not

  (c) decouple one temperature effect from another and

  (d) perform changes to the temperature scaling equations without adversely affecting model performance in another regime or breaking the model

MOS20 Model - Equations

$$I_{ch} = \frac{W\mu_{eff}C_{ox}}{L_{ch}} \frac{\left(V_{invo} - \frac{1}{2}\xi V_{DiS}\right)V_{DiS}}{1+\theta_3 V_{DiS}}$$

- In the channel current equation above, β_i replaces $\frac{W\mu_{eff}C_{ox}}{L_{ch}}$
- β_i scales with temperature as follows:

$$\beta_T = \beta_i \cdot \frac{T_{ref}}{T_{ambient}}^{\eta_\beta}$$

- ETABET (η_β) is the lone control that the user has to define the temperature behavior of the gain factor
- Other temperature scaling equations include:

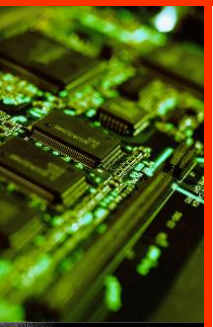
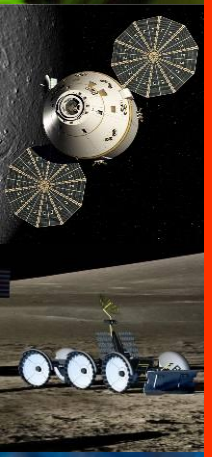
$$V_{FBT} = V_{FB} + \Delta T \cdot S_{TVFB}$$

$$R_{D_T} = R_D \cdot \frac{T_{ambient}}{T_{ref}}^{\eta_{R_D}}$$

$$\varphi_{BT} = \varphi_B + \Delta T \cdot S_T\varphi_B$$

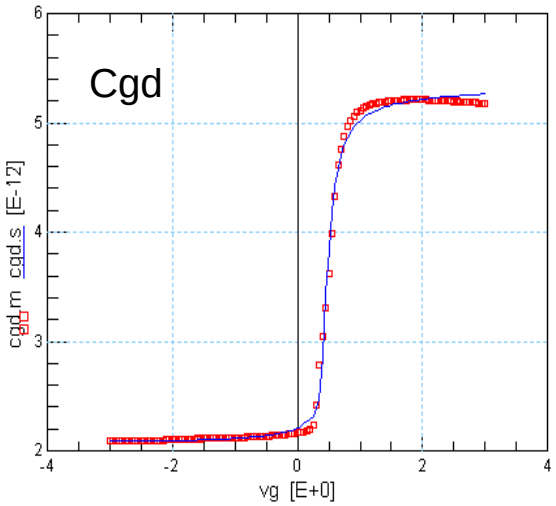
$$\theta_{3_T} = \theta_3 \cdot \frac{T_{ref}}{T_{ambient}}^{\eta_{\theta_3}}$$

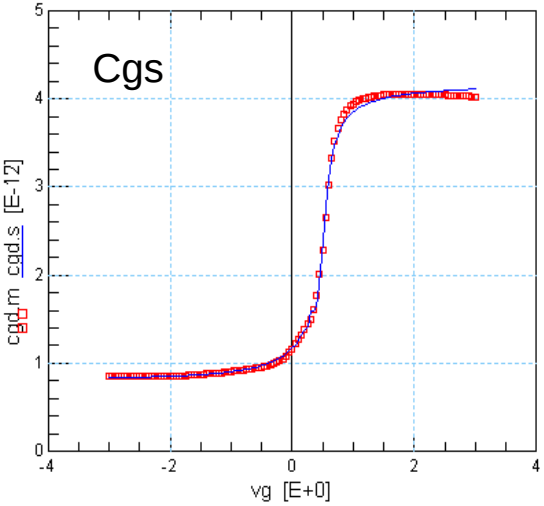
Native model performance

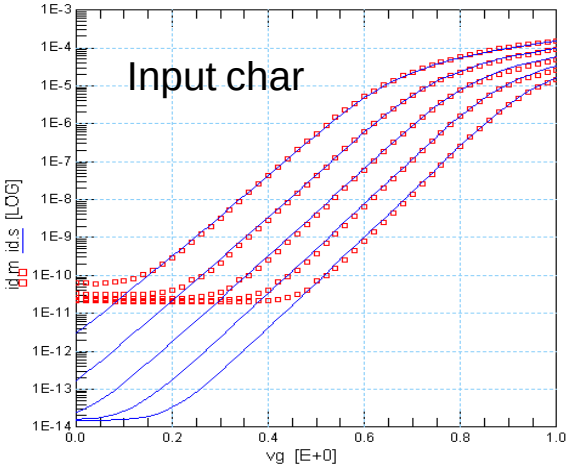



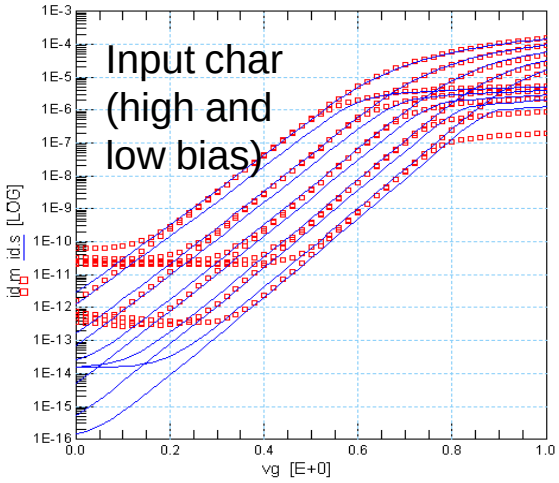
- The performance of the MOS20 model has to be tested to see if the model can track the measured data, especially over temperature
- Extreme environment designers often have to make-do with binned iso-thermal models
- They have many disadvantages
  - effects such as self-heating will not be accounted for
  - may not be very accurate if many temperatures points are not considered
  - cannot be used to design circuits that require a continuous replication of the device performance over the temperature range – (e.g. bandgap reference)
  - would require greater time and effort for realizing the design
  - the possibility of human errors increase due to switching between various parameter sets

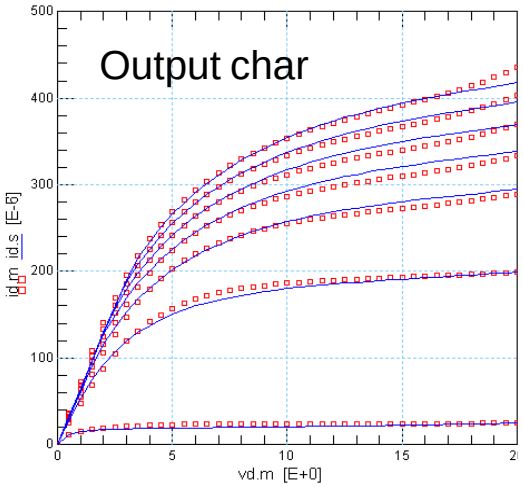
Iso-thermal extraction – room temperature

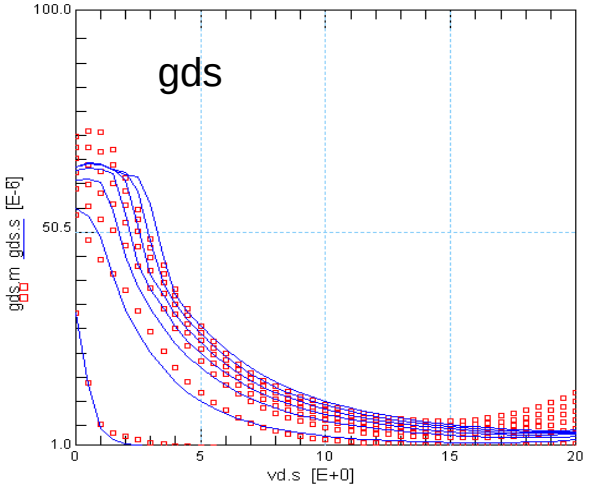




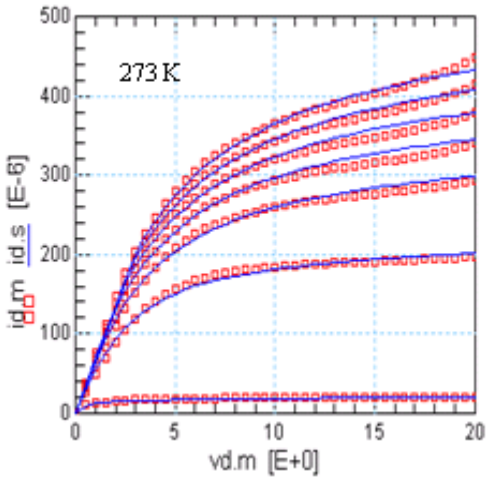


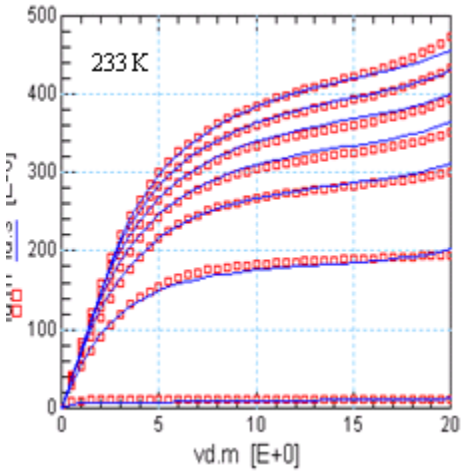


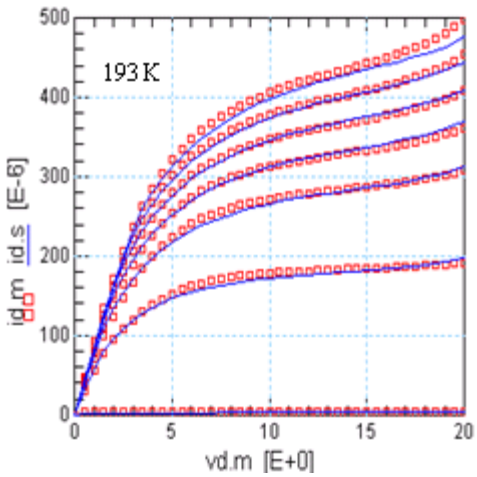


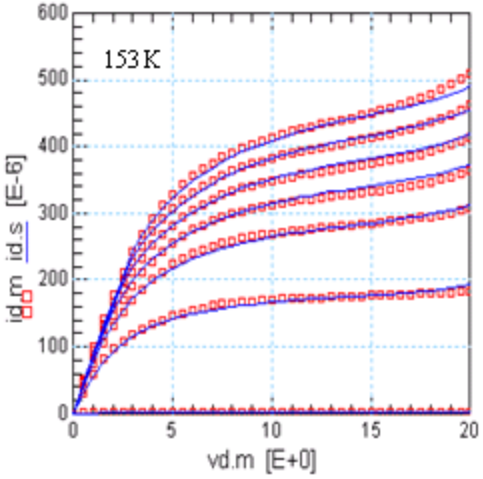


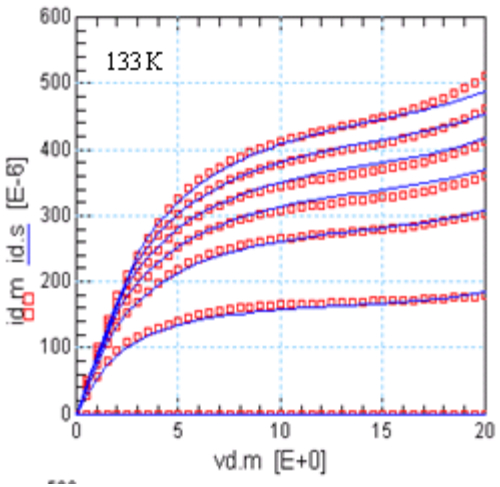
Iso-thermal extraction – all temperatures

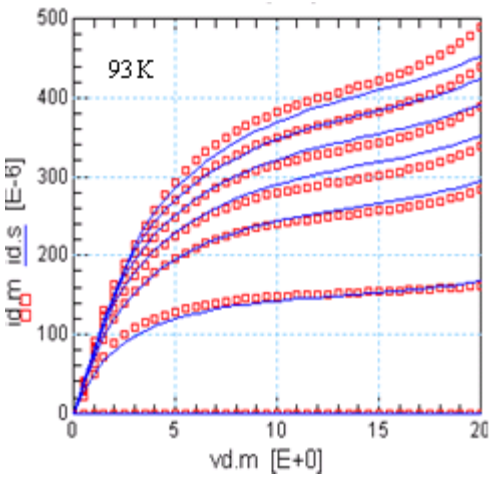










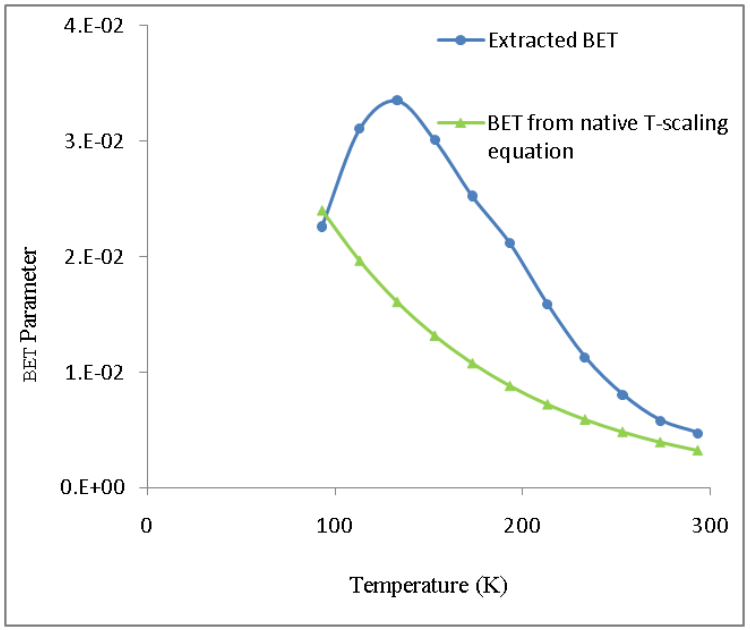


Parameter Audit

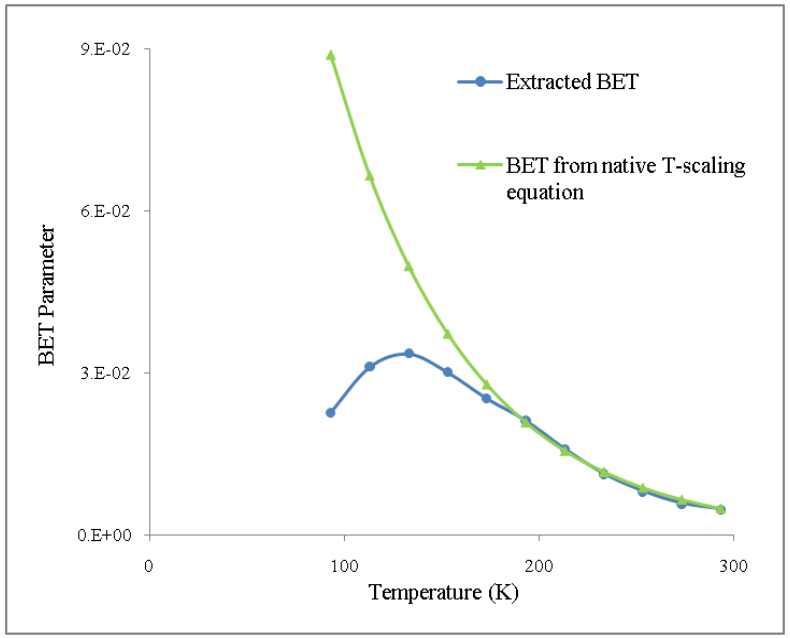
- After the completion of the iso-thermal extractions, the values of the parameters that scale with temperature were plotted against the temperature
- This will give an idea as to what parameters scale with temperature, how they vary and if the scaling relations in the native model are sufficient to describe them or not.
- Parameters audited include BET, BETACC, RD, THE3, PHIB etc.
- These plots were then superimposed with the same parameters calculated by the temperature scaling equations.

Parameter Audit

Method I

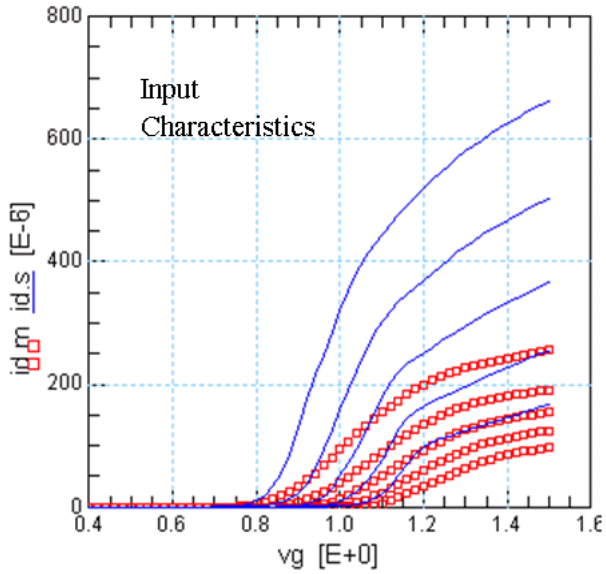


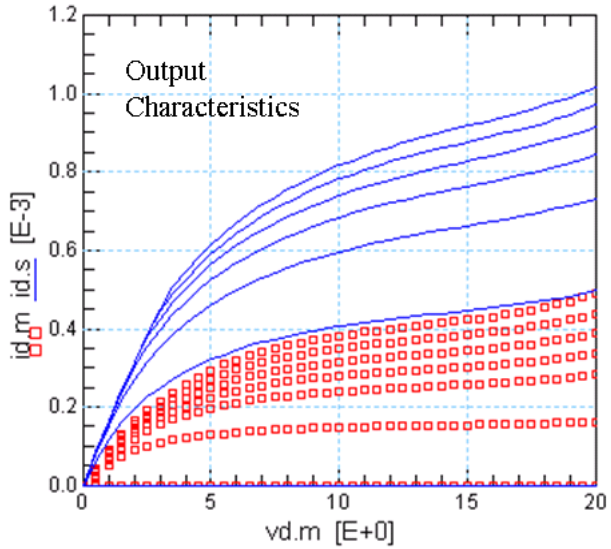
Method II

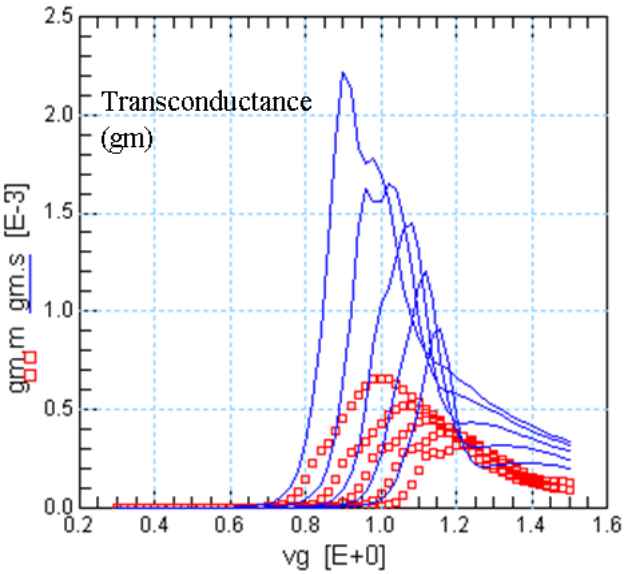


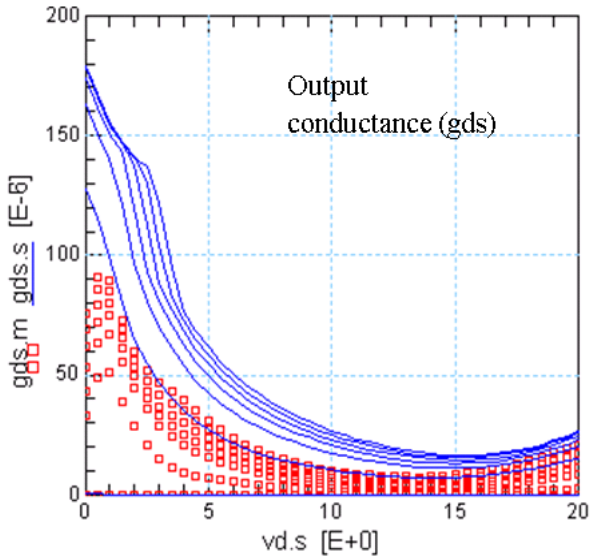
- This was repeated for other parameters
- Clearly the native T-scaling equations grossly under- or overestimate the parameter values in deep cryo temperatures
- But it should be noted that the native T-scaling equations work accurately for temperatures down to 193 K (-80 C), which is sufficient for commercial specifications (120 C $<T_A<$-55 C)

Performance of the native model at 93 K (-180 C)









Outline

- Motivation
- LDMOS devices and characterization
- The MOS20 model and performance
- Cryogenic Model Development - New T-scaling equations
- Model Validation
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- Conclusions

New T-scaling equations development

- When new equations are being developed – the physical vs. empirical debate arises
- While modelers generally favor physics based models, it is often a trade-off between using physically meaningful equations and model performance (speed, convergence etc.)
- This issue gets more complicated when temperature equations are considered
- Often “physics based” equations on temperature effects on mobility have their own arbitrary constants and relations
- Convergence is not easy – manual states many iterations may be required for cryo simulations (for *ONE* device) and may often fail to converge
- Analog circuits have many dozens of transistors or passives – not a practical solution to use such equations

New T-scaling equations development

- Freeze-out in compact modeling terms can be visualized as the decrease in mobility and the consequent increase in the drift region resistance
- Instead of reducing the % of active carriers – the mobility and resistance terms can be made to vary non-monotonically
- These equations should have (a) at least some physical relevance (b) should be compact model friendly
- Analog circuits have many dozens of transistors or passives – not a practical solution to use such equations
- Various mathematical functions were evaluated to represent the non-monotonic parameter behavior
- An extreme value distribution function (Gumbel distribution) was finally selected because it satisfies both the criteria above

New T-scaling equations development

- The function is of the form

$$f(x) = \frac{e^{-\frac{x-\mu}{\eta}} \cdot e^{-e^{-\frac{x-\mu}{\eta}}}}{\eta}$$

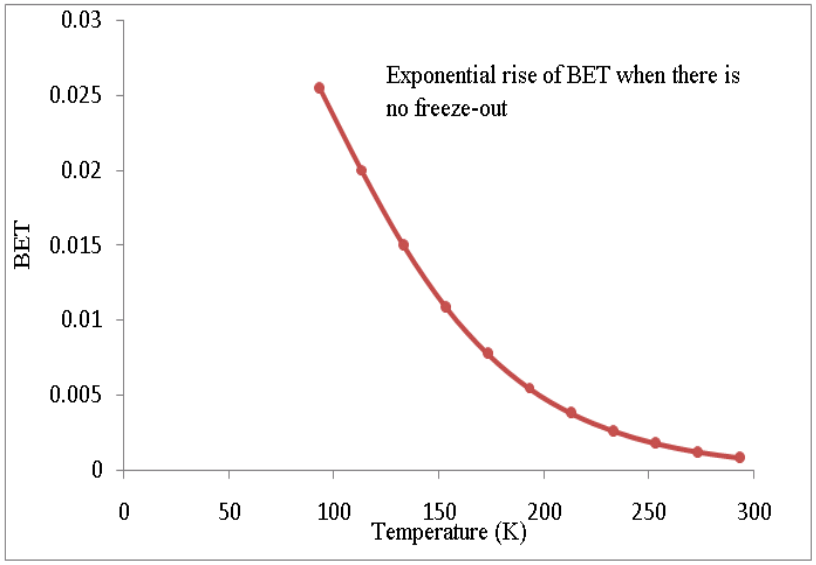
- μ is the location parameter and η is the scale parameter
- For the parameter BET, the above formulation was adapted using mathematical tools as;

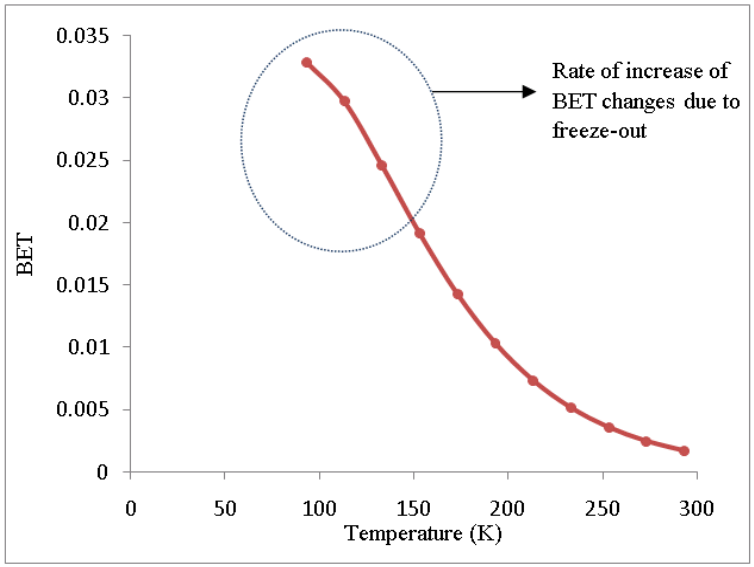
$$\beta_T = \frac{e^{-\beta_{tmp}} \cdot e^{-e^{-\beta_{tmp}}}}{\beta_{mult}}$$

$$\beta_{tmp} = \frac{T_A - T_T}{\beta_i \cdot \beta_{EXP}}$$

New T-scaling equations development

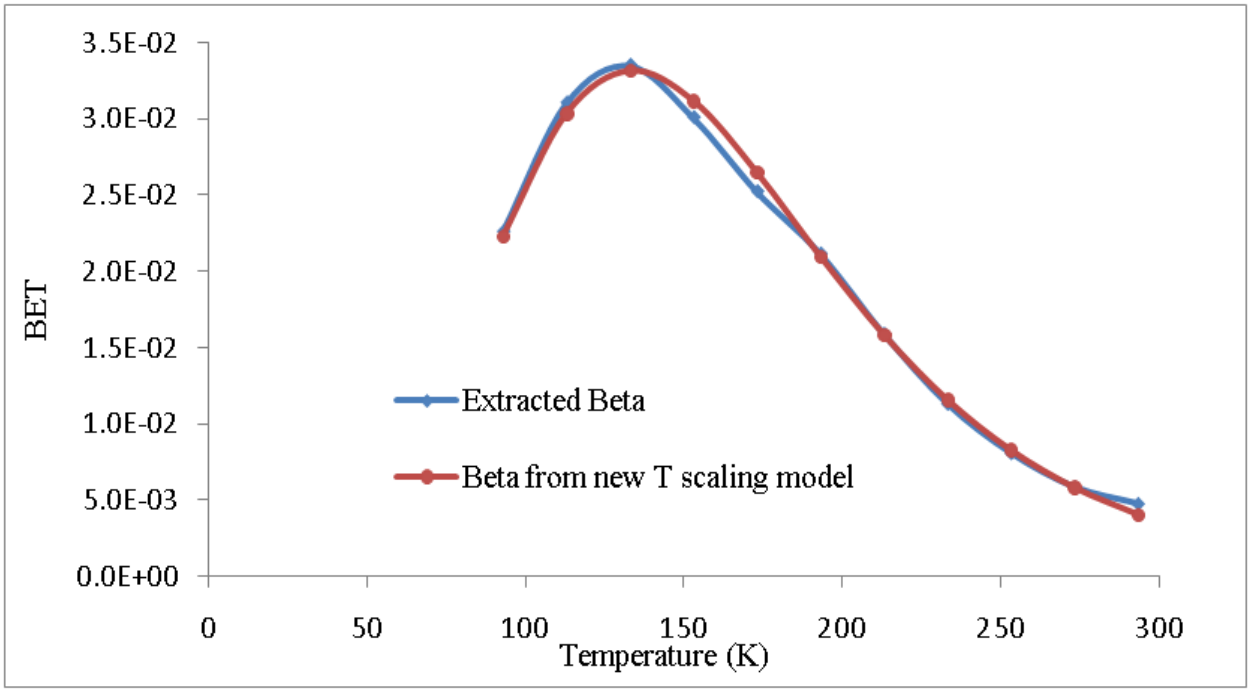
- ETABET parameter replaced by two new parameters – BETMULT and BET, TT is the transition temperature and can be varied to adjust roll-off location
- Equation is very flexible in modeling minimal, moderate and extreme freeze-out behavior



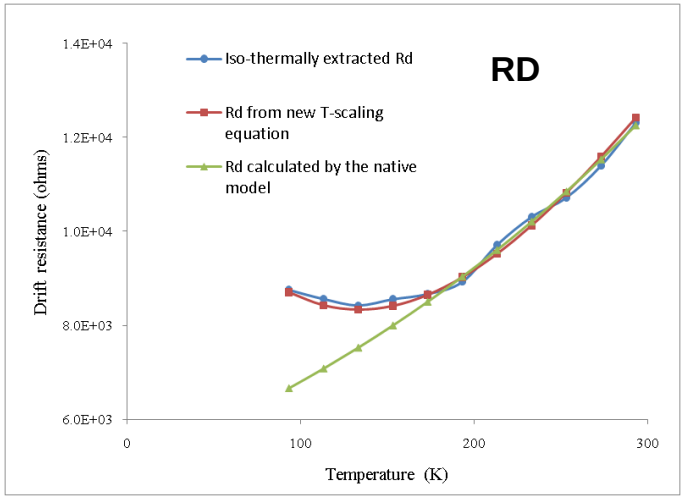


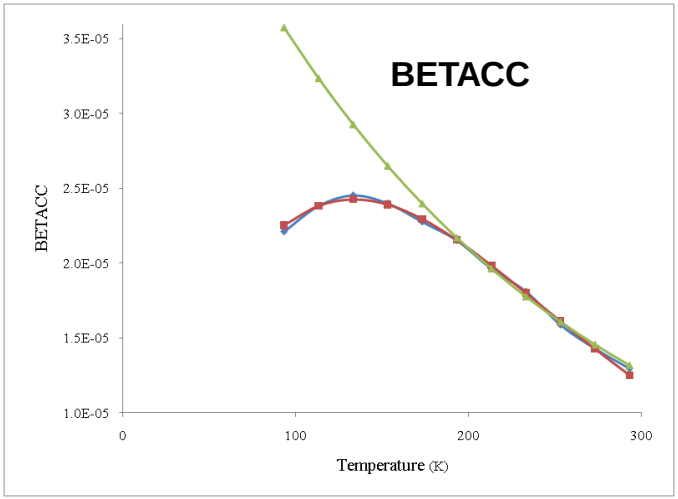
New T-scaling equations development

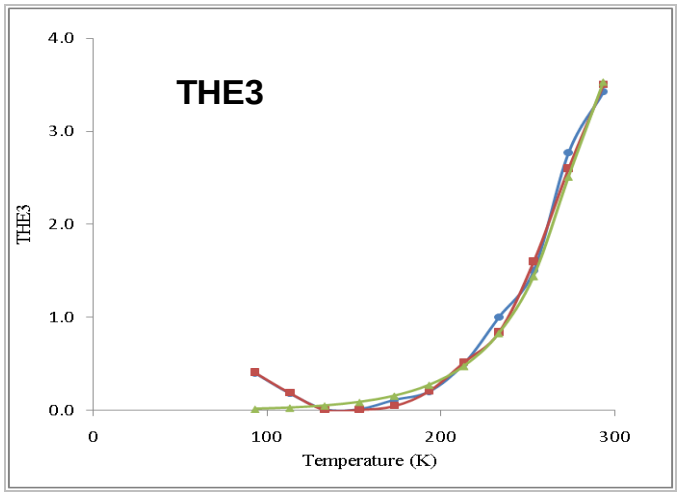
- For this device, TT was set at 133 K
- The new equation is able to replicate BET behavior to a great level of accuracy (error < 0.5%)

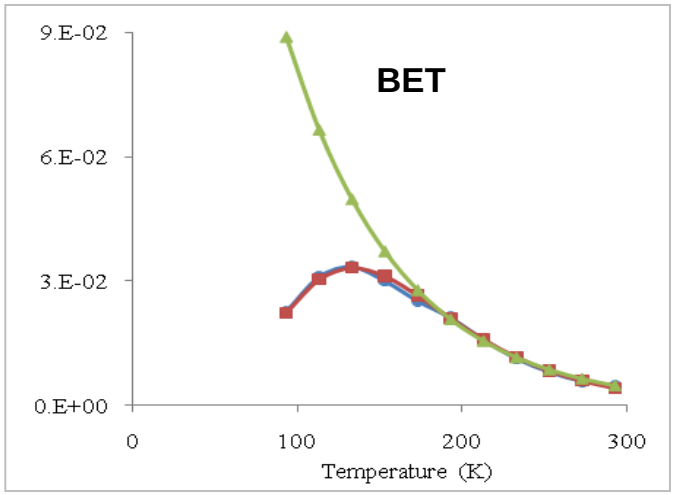


New T-scaling equations development



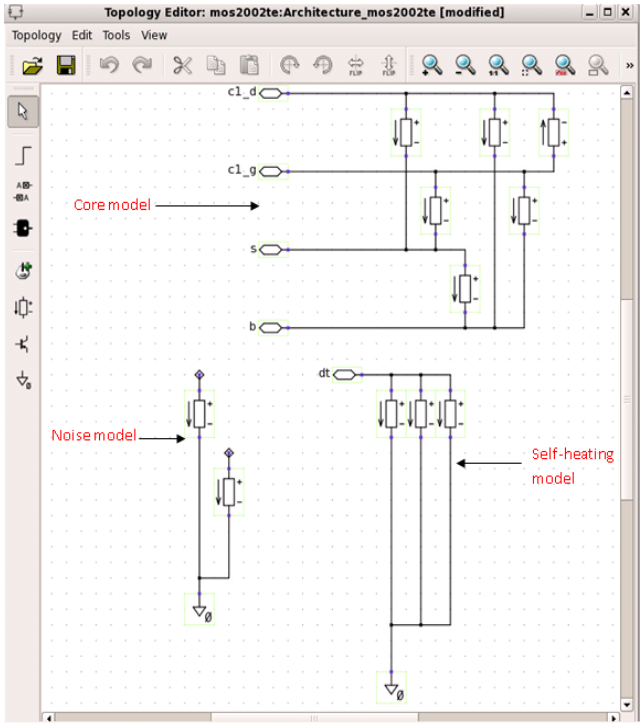


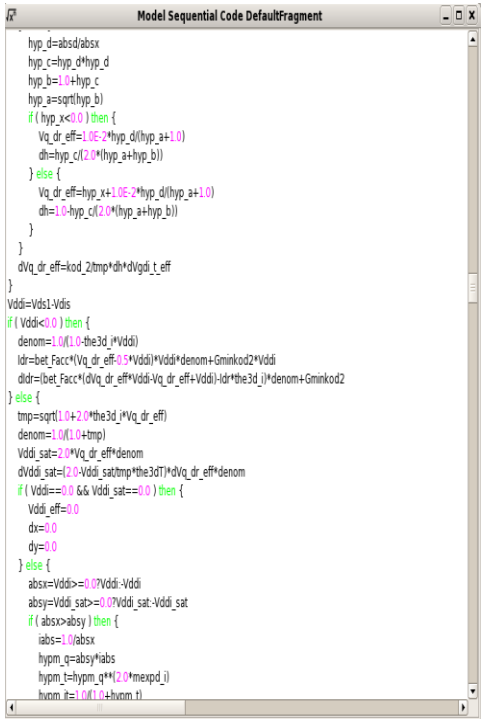


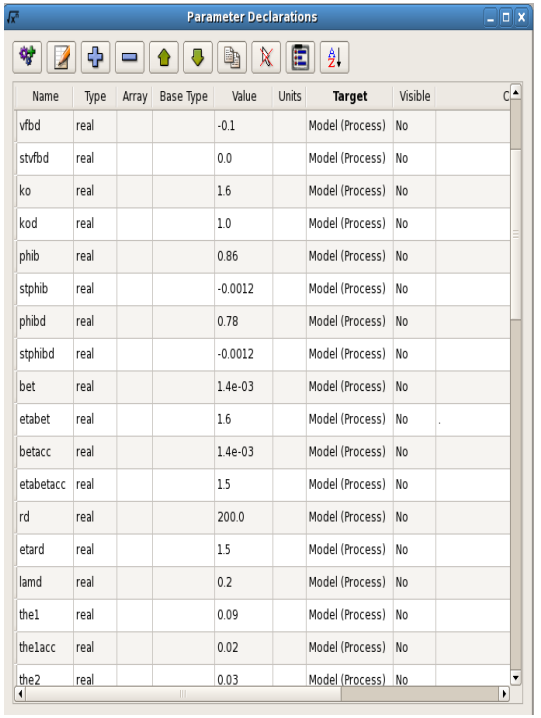


Model Implementation

- The equations hence developed have to be implemented in the model code
- Difficult to modify C code, all changes made in Verilog-A code received from NXP
- Code imported into ModLyng tool







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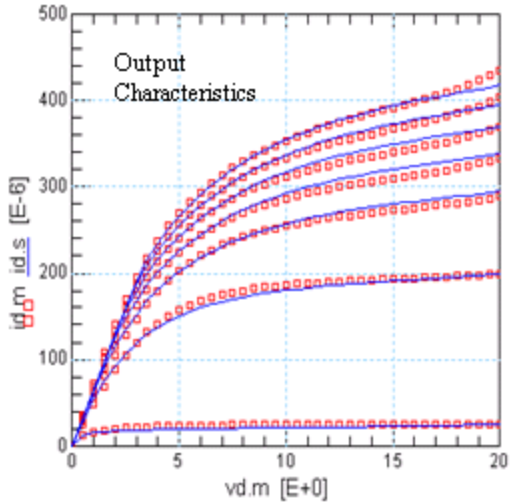
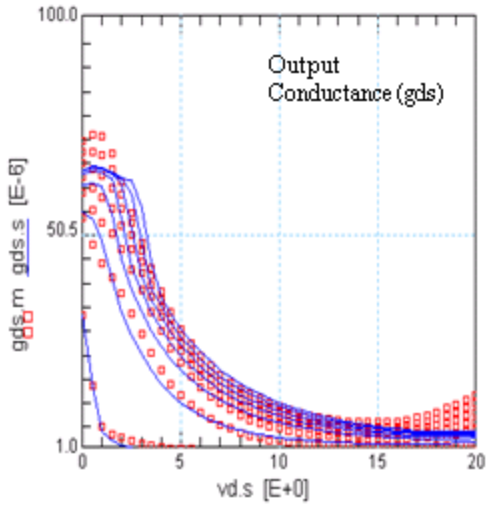
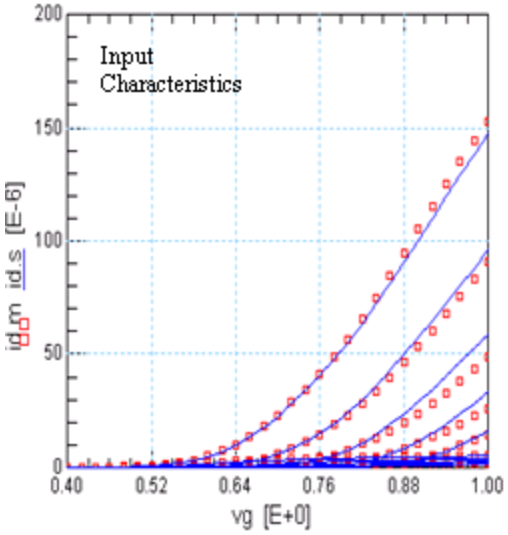
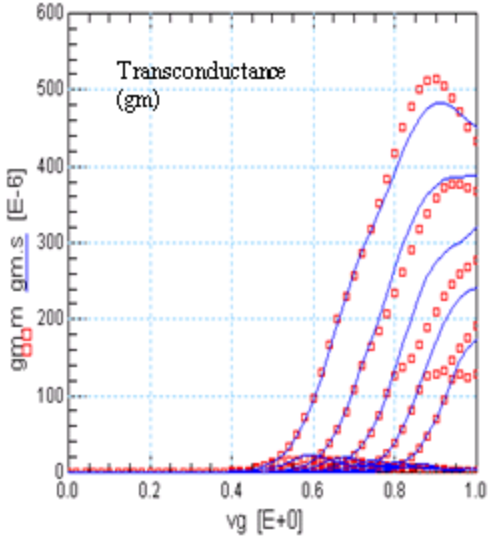
Model Validation – Room temperature

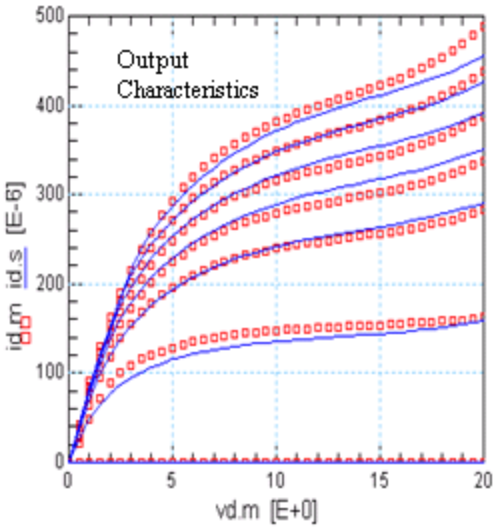


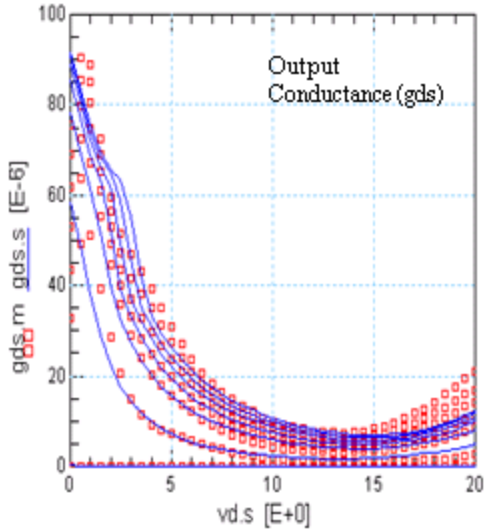


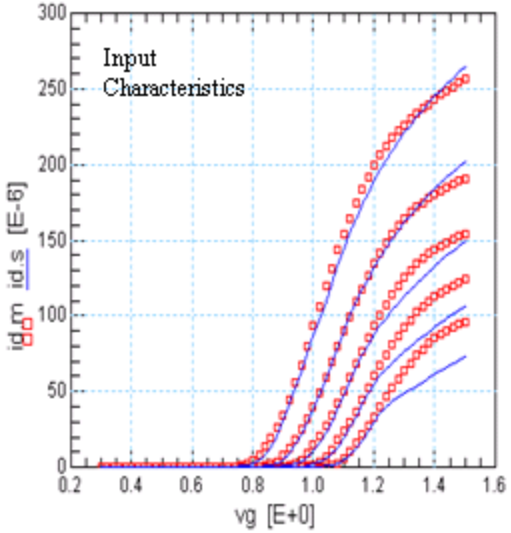


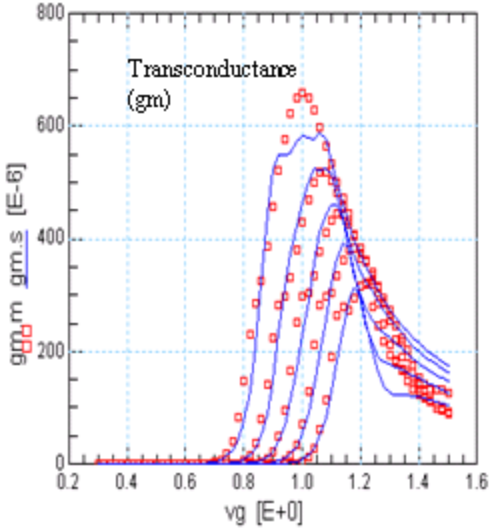


Model Validation – 93 K









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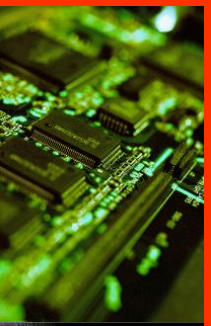
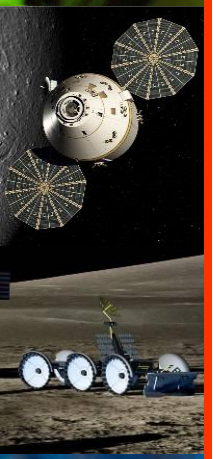
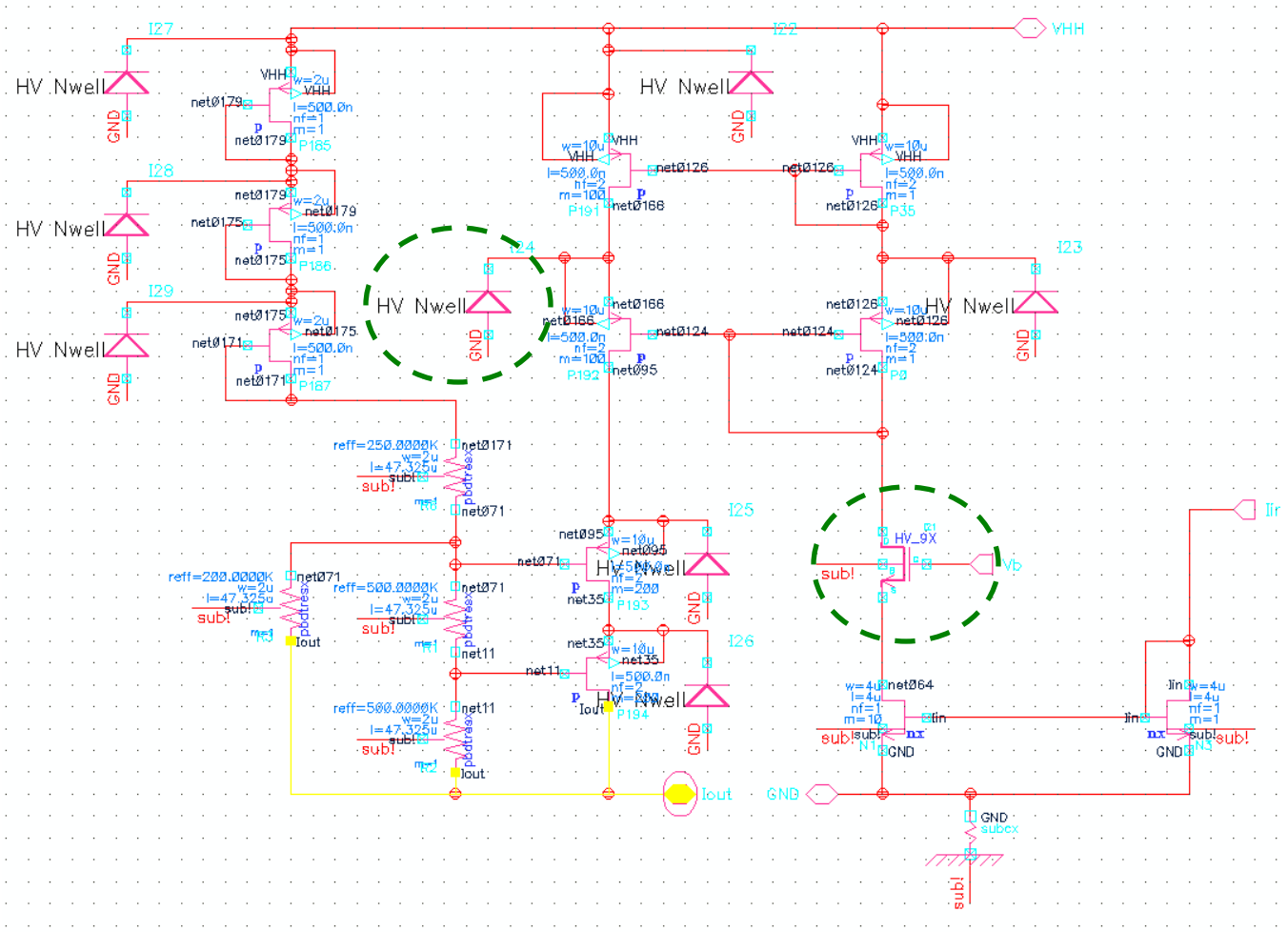
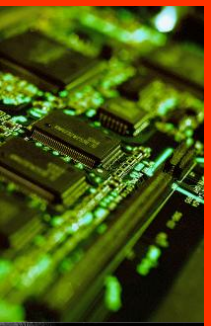
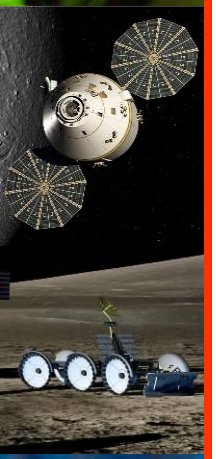
HV Current Mirror



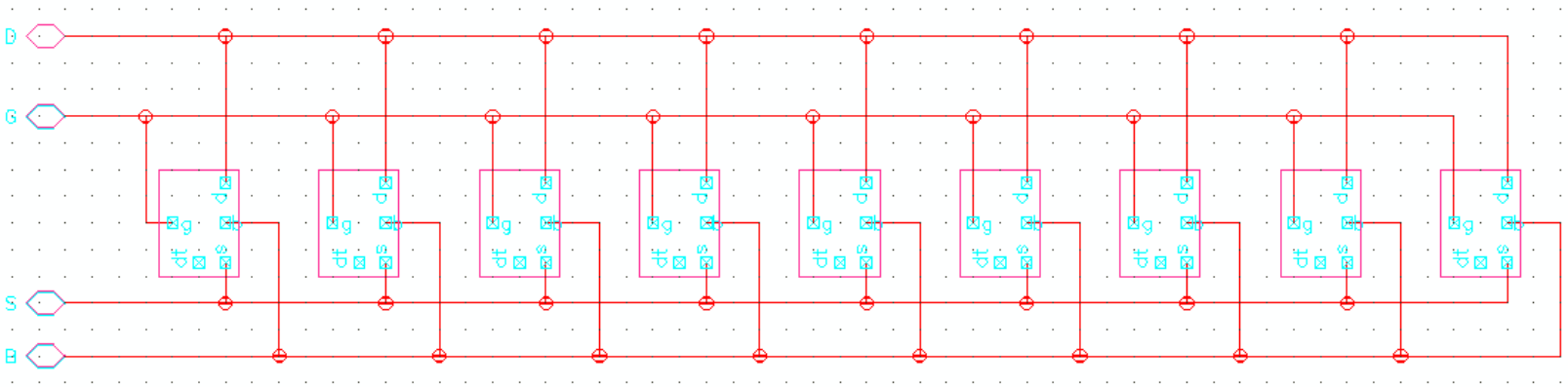




HV Current Mirror

HV9X



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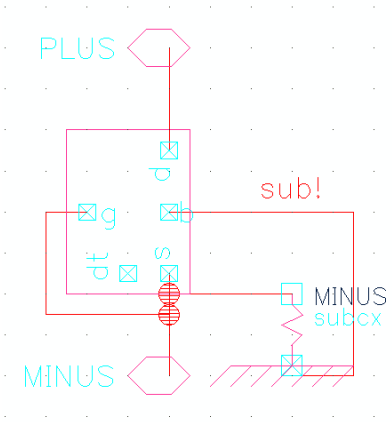

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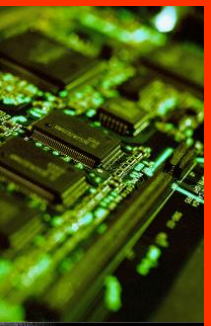
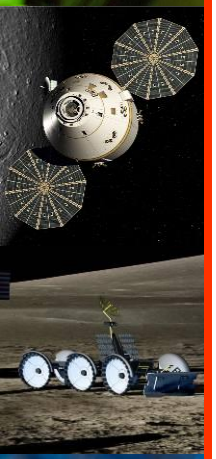

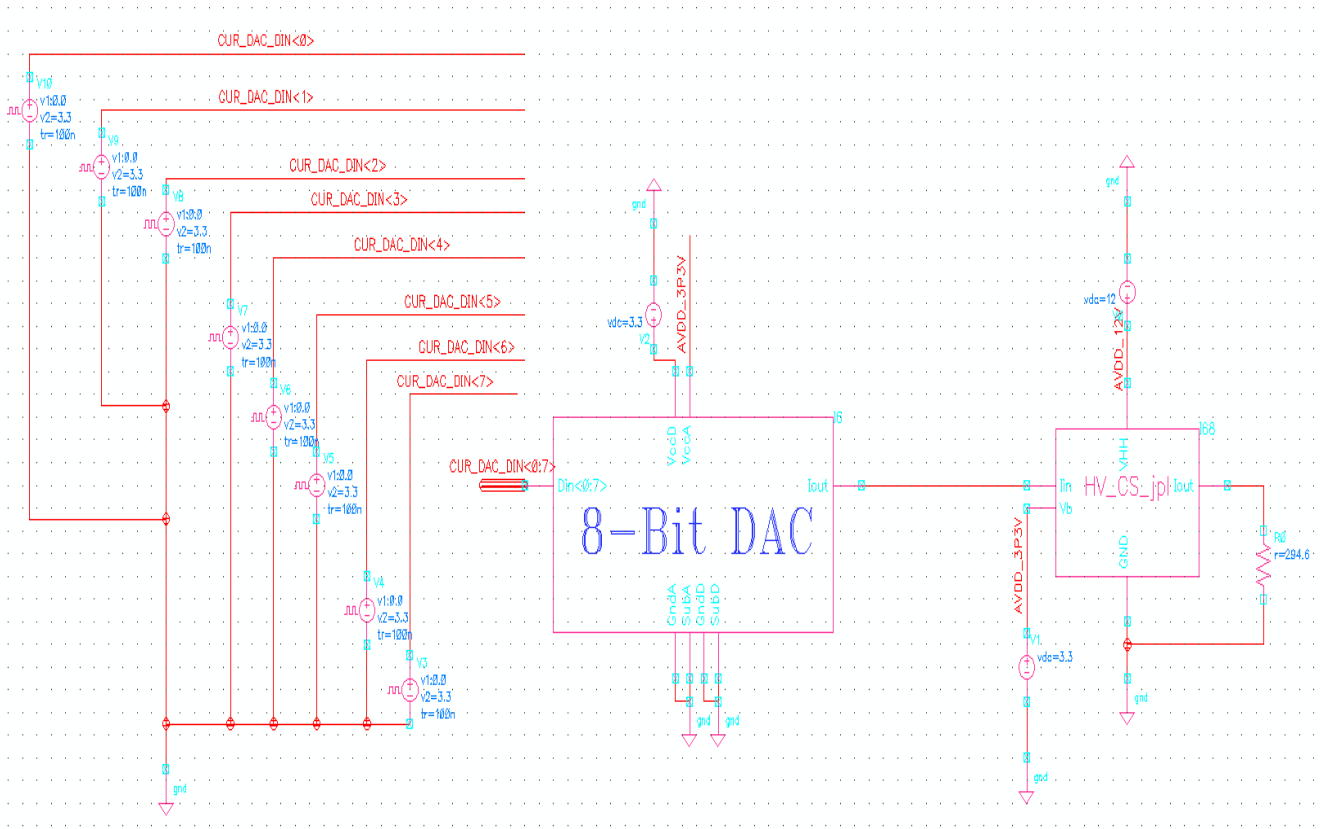

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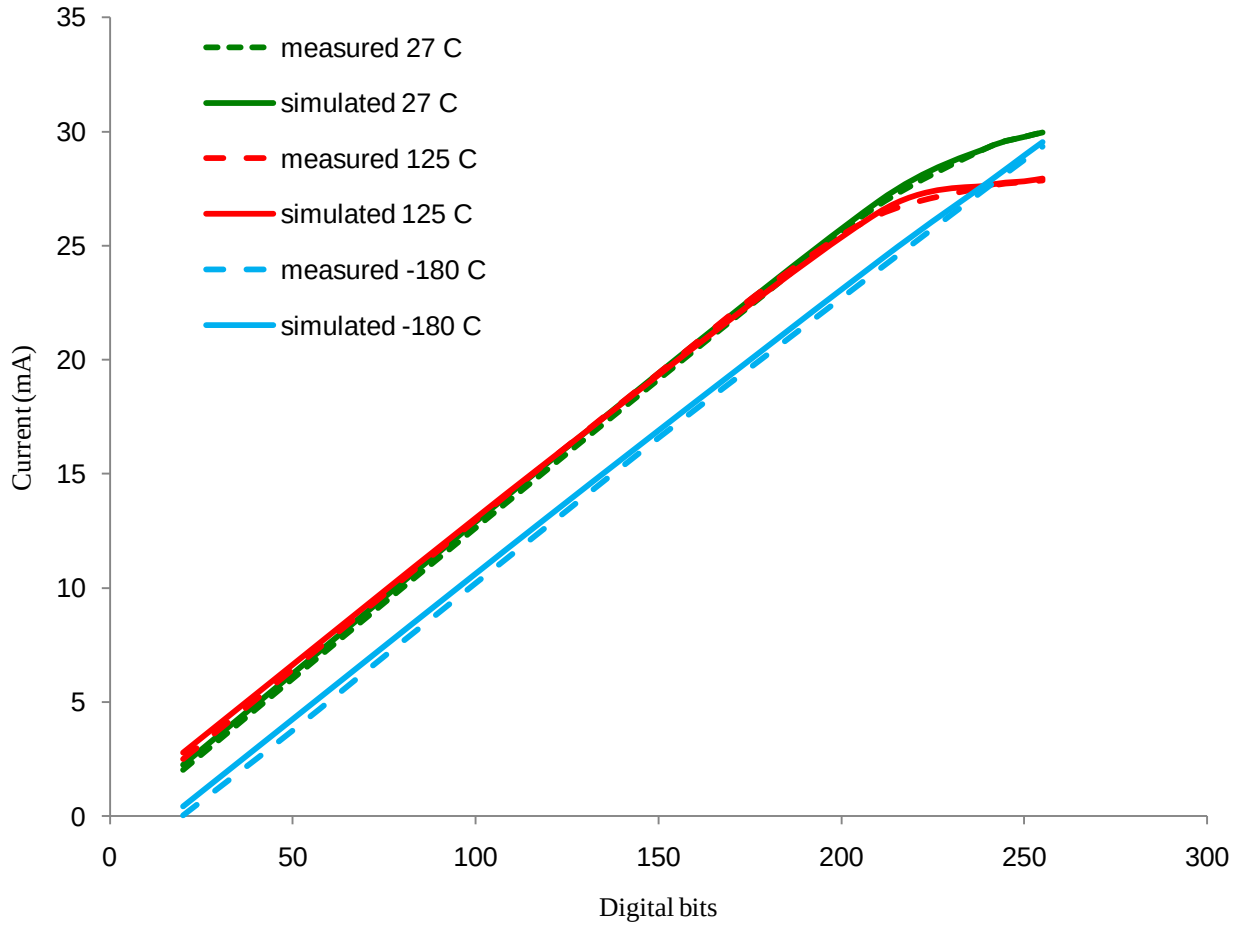
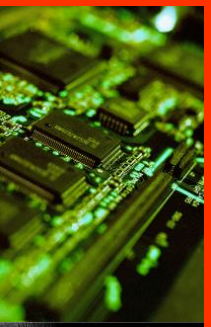
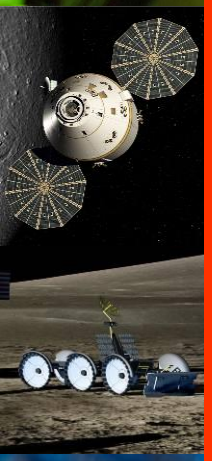


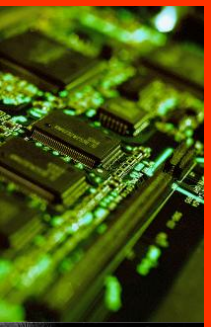
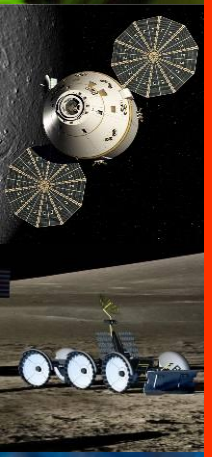
Materials International Space Station Experiment (MISSE)





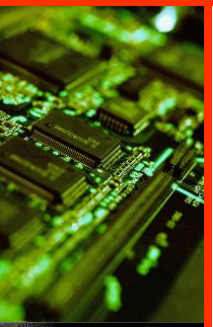
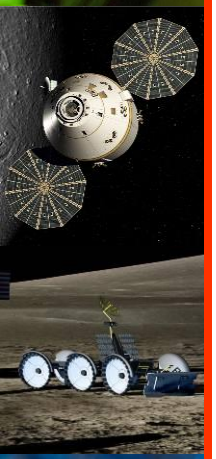
On Spacewalk #5 of the Endeavor crew, UA electronics are now attached to the outside of the International Space Station

Conclusions

- LDMOS devices were characterized from 393 K to 93 K
- Anomalous effect was seen in output characteristics
- Identified as carrier freeze-out caused by incomplete ionization
- The MOS Model 20 model was selected
- Through iso-thermal extractions and model auditing, it was shown that the native T-scaling equations were insufficient to model this device
- New equations were developed, implemented and validated - that can replicate current roll-off due to impurity freeze-out
- Can be used to model other non-monotonic effects such as radiation.
- Device model used to simulate analog extreme environment circuits for lunar applications
- One model scales the entire temperature range

Acknowledgements

- NASA
- The entire SiGe ETDP Team
- NXP Semiconductor for providing the source code of the MM20 model
- Lynguent Inc. for providing ModLyng

Questions