MOS-AK Workshop – Johns Hopkins University, Baltimore, USA

Unification of MOS Compact Models with the Unified Regional Modeling Approach

Xing Zhou

School of Electrical and Electronic Engineering &
Institute for Sustainable Nanoelectronics,
Nanyang Technological University, Singapore

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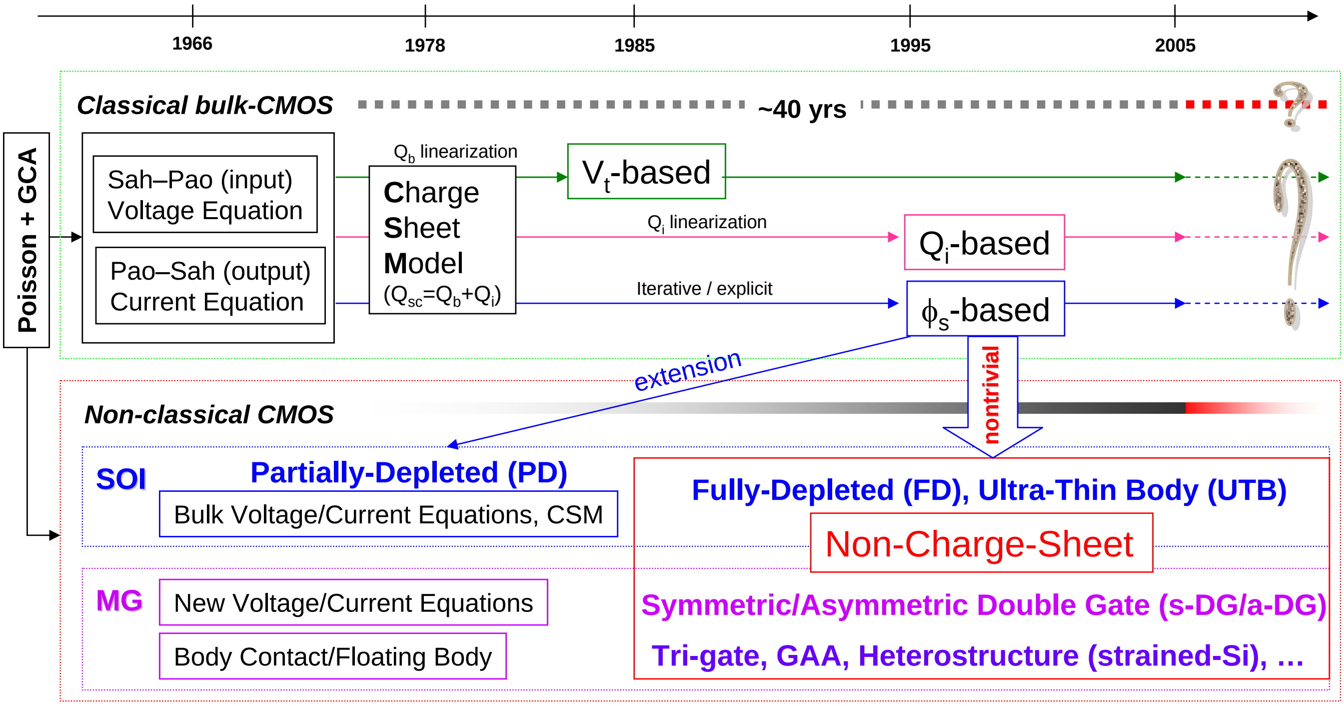
Email: exzhou@ntu.edu.sg

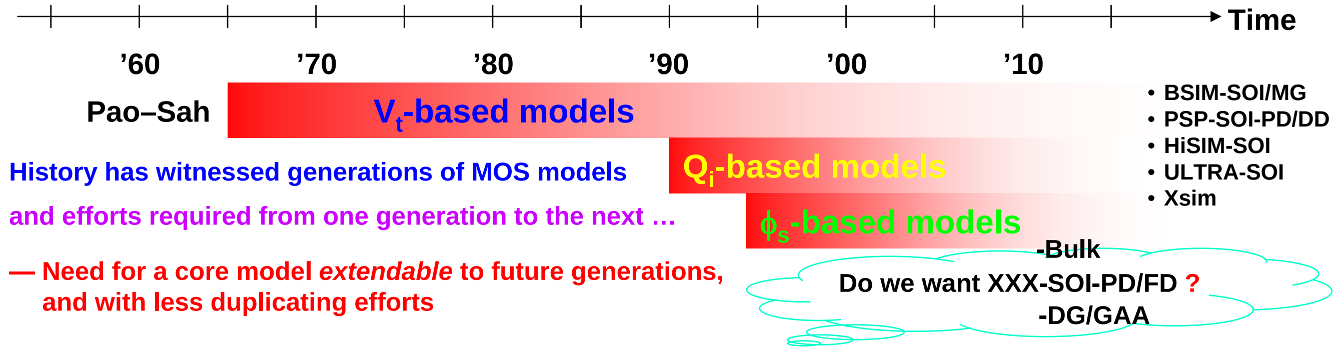
Presentation Outline

- **Motivation for MOS Model Unification**
    - **Model extendibility and modeling efforts**
    - **Seamless physical scalability**
- **Unified Regional Modeling (URM) Approach**
    - **<u>Key challenges</u>:** symmetry and body contact, doping scaling (non-charge-sheet), contact effect (SB/DSS)
    - **<u>Unique features</u>:** decoupled regional surface-potential solution, bulk/ground-reference and source/drain by label, ambipolar SB model, and subcircuit model for DSS
- **Xsim Model Results and Ultimate Goals**
    - **Bulk-MOS current and charge models**
    - **FB-SOI and s-DG FinFETs**
    - **SiNW and SB/DSS MOSFETs**
    - **Xsim: history, evolution, and future goals**

MOSFET Compact Models: History and Future



Need for an Extendable Core Model for Future Generation

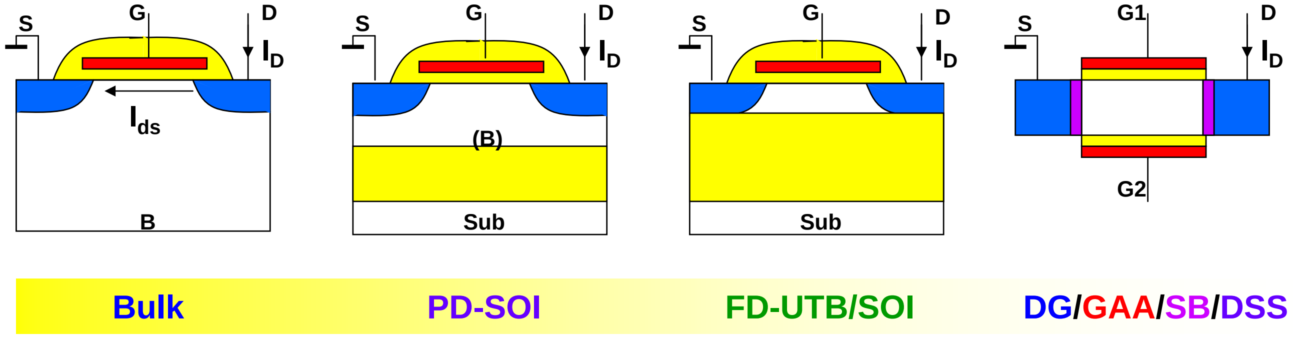


History has witnessed generations of MOS models

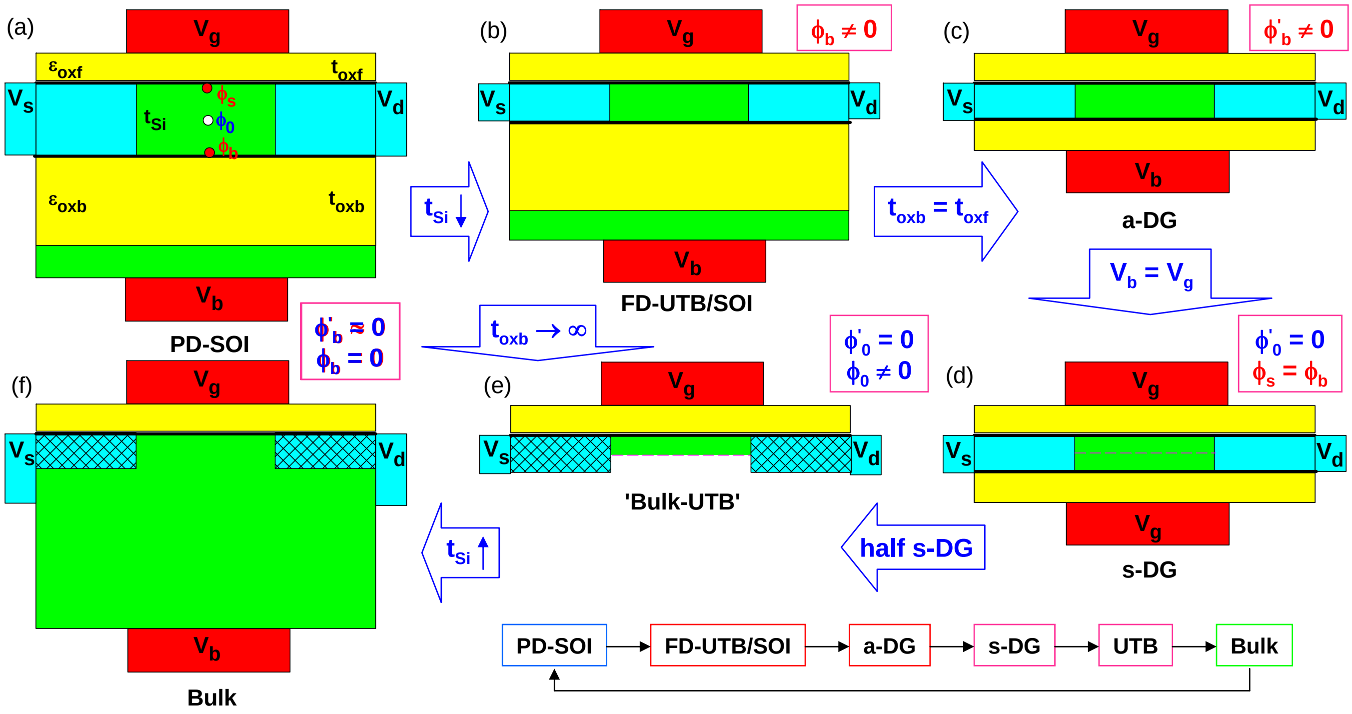
and efforts required from one generation to the next …

— Need for a core model *extendable* to future generations, and with less duplicating efforts

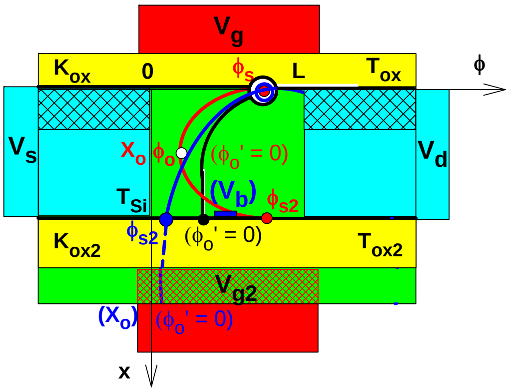
- **BSIM-SOI/MG**
- **PSP-SOI-PD/DD**
- **HiSIM-SOI**
- **ULTRA-SOI**
- **Xsim**



Seamless Transformation and Unification of MOSFETs



Common/Independent Symmetric/Asymmetric-DG MOSFET



Since Poisson equation cannot be integrated twice when doping is considered, we do not solve combined solutions at the two Si/SiO$_2$ interfaces; instead, we solve the two separately with zero-field as the other 'boundary'.

❑ **Common/symmetric-DG** [FinFET]

- $V_{g1} = V_{g2} = V_g$: two gates with one bias
- $C_{ox1} = C_{ox2}$: **s-DG** ($X_o = T_{Si}/2$)
- **Full-depletion**: $V_{FD} = V_g(X_d{=}T_{Si}/2)$
- $C_{ox1} \neq C_{ox2}$: **ca-DG** ($X_o < T_{Si}$)

❑ **Independent/asymmetric-DG** [SOI]

- $V_{g1} \neq V_{g2}$: **ia-DG**, biased independently
- Zero-field location may be outside body
- Consider two "independent" gates; linked through **full-depletion** condition:

$$\boxed{X_{d1} + X_{d2} = T_{Si}}$$

❑ **Unification of MOS**

- SOI ← $\boxed{\textbf{ia-DG}}$ ↔ ca-DG ↔ $\boxed{\textbf{s-DG}}$ → bulk (s-DG ↑ SiNW)

➢ **Zero-field potential**: $\boldsymbol{\phi_o}$ [$\phi_o'(X_o) = 0$]

Our Approach: Unified Regional Model (URM)

- ❑ **Start with s-DG with doped body** (two unknowns, ϕ_s and ϕ_o)

$$p_0 = n_i e^{\phi_{Fp}/v_{th}}$$

$$\phi_{s1} = \phi_{s2} = \phi_s \qquad E_s = -\phi_s' = +\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V_{gf} - \phi_s}{T_{ox}}$$

$$E_o = 0 \qquad \left(V_{gf} \equiv V_g - V_{FB}\right)$$

$$\boxed{\begin{aligned} V_{gf} - \phi_s &= \mathrm{sgn}\left(\phi_s - \phi_o\right) \Upsilon \sqrt{f_\phi}, \quad \Upsilon = \sqrt{2q\varepsilon_{Si} p_0} \big/ C_{ox}, C_{ox} = \varepsilon_{ox} / T_{ox} \\ v_{gf} - \varphi_s &= \mathrm{sgn}\left(\varphi_s - \varphi_o\right) \gamma \sqrt{f_\varphi}, \quad \gamma \equiv \Upsilon \big/ \sqrt{v_{th}}, \varphi \equiv \phi / v_{th}, v \equiv V / v_{th} \end{aligned}}$$

$$\boxed{f_\varphi\left(\varphi_s, \varphi_o, v_{cr}\right) = e^{v_r}\left(e^{-\varphi_s} - e^{-\varphi_o}\right) + \left(\varphi_s - \varphi_o\right) + e^{-(2\varphi_F + v_{cr})}\left[e^{-v_r}\left(e^{\varphi_s} - e^{\varphi_o}\right) - \left(\varphi_s - \varphi_o\right)\right]}$$

- ❑ **Highly-doped body: Charge-sheet approximation (CSA), similar to bulk**
- ❑ **Undoped/(lowly-doped) body: Non-CSA (2nd integral of Poisson)**
- ❑ **Extend URM approach to ϕ_s solution — finding the "full-depletion voltage" V_{FD}**
  - ➢ Scale with N_{ch}, T_{Si}, T_{ox}, K_{ox} in all regions — ϕ_s readily applicable in bulk $I_{ds}(\phi_s)$
  - ➢ Bulk model for short-channel/higher-order effects can be easily extended
- ❑ **Extending to a-DG — two 'independent' s-DG coupled by one $V_{FD}(V_{g1},V_{g2})$**
  - ➢ Without solving coupled solutions, which is impossible (rigorously) for doped body
  - ➢ Recoverable to s-DG, FD/PD-SOI, undoped, bulk — unification of MOS models

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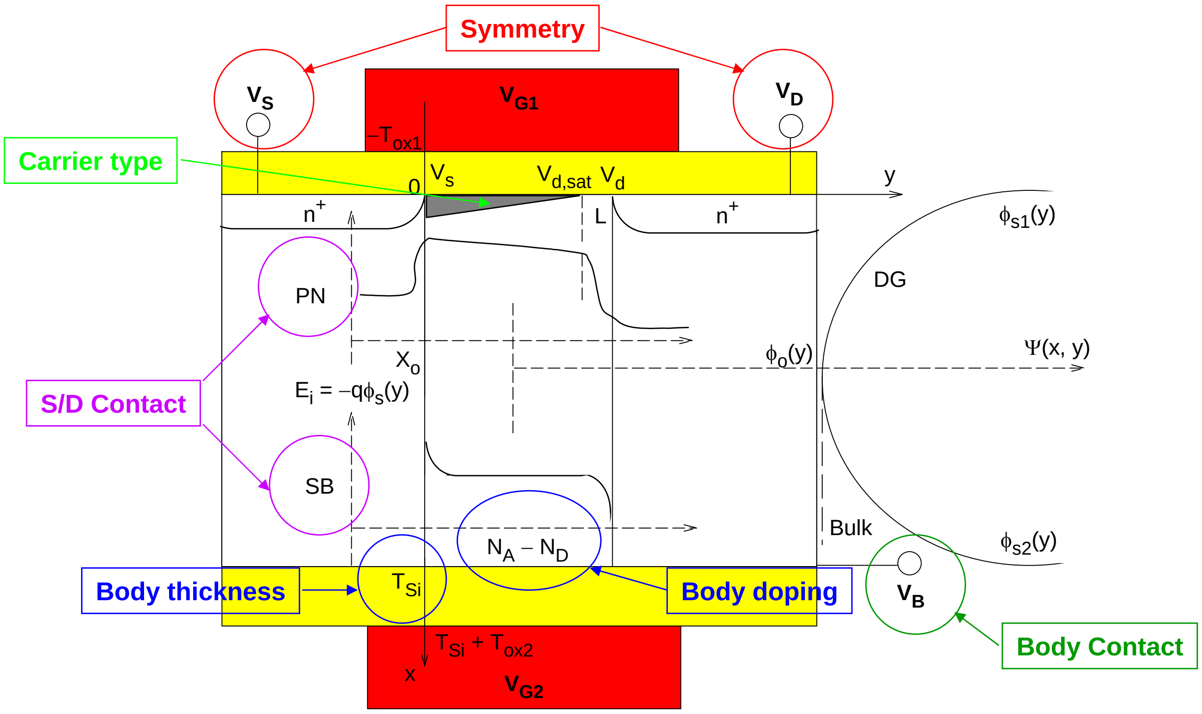
Generic DG/SOI-MOSFET With/Without Body Contact



Regional ϕ_s Solutions and Full-Depletion Voltage

FD condition: $\boxed{X_{d1,FD}\left(V_{g1,FD}\right)+X_{d2,FD}\left(V_{g2,FD}\right)=T_{Si}}$

s-DG: $\boxed{X_{d,FD}\left(V_{g,FD}\right)=T_{Si}/2}$

$$\phi_s-\phi_o=\frac{qN_AX_o^2}{2\varepsilon_{Si}}\quad\left(X_o=T_{Si}/2\right)$$

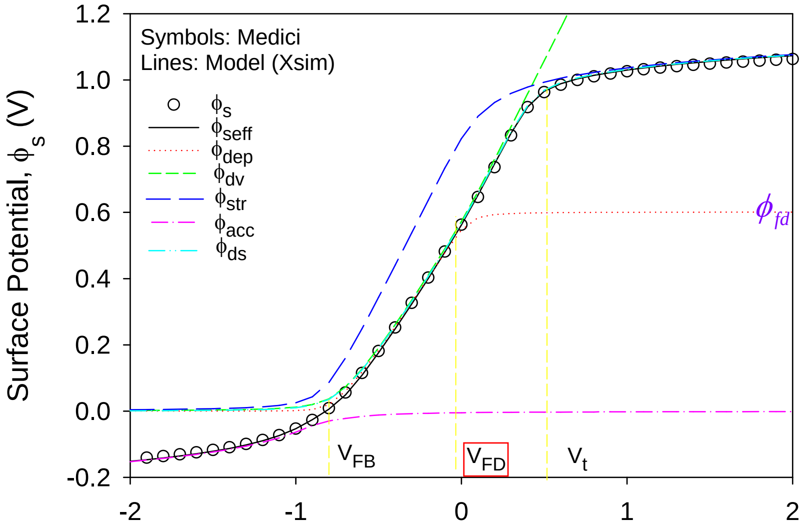
$$\boxed{\phi_{str}=V_{gbf}-2v_{th}\mathcal{L}\left\{W\right\}}$$

$$\phi_{fd}=\frac{qN_AX_{d,FD}^2}{2\varepsilon_{Si}}=\left(-\frac{\Upsilon}{2}+\sqrt{\frac{\Upsilon^2}{4}+V_{gf,FD}}\right)^2$$

$$\boxed{\phi_{dv}=V_{gf}+\Upsilon\sqrt{\phi_{dep}}}$$

$$\boxed{\phi_{dep}=\vartheta_{eff}\left\{\phi_{sub},\phi_{fd};\delta_d\right\}}$$

$$\boxed{\phi_{ds}=\vartheta_{eff}\left\{\phi_{dv},\phi_{str};\delta_\phi\right\}}$$

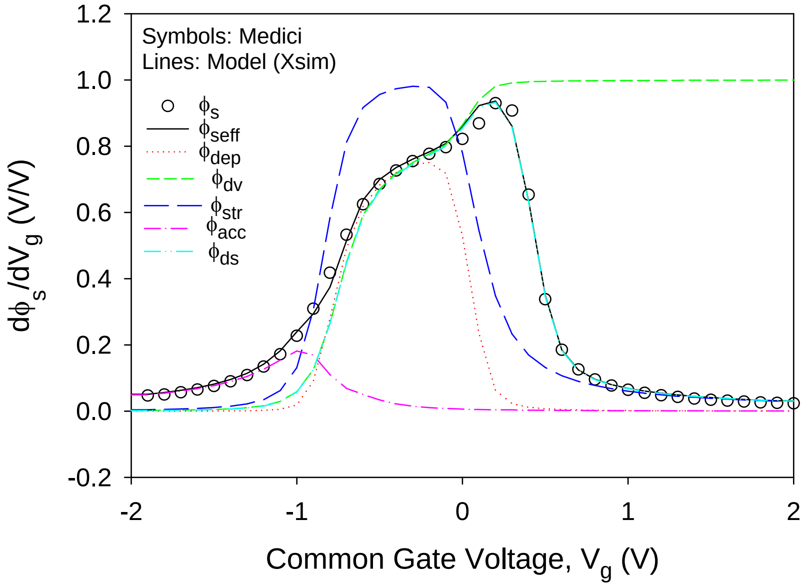


$$\boxed{\phi_{seff}=\phi_{acc}+\phi_{ds}}$$

$$\boxed{\phi_{acc}=V_{gbr}+2v_{th}\mathcal{L}\left\{W\right\}}$$

$$\phi_{sub}=\left(-\frac{\Upsilon}{2}+\sqrt{\frac{\Upsilon^2}{4}+V_{gbf}}\right)^2$$

Surface-Potential Derivatives and Regional Components



- ☐ **Regional solutions scale with body doping (N_A), body thickness (T_{Si}), oxide thickness (T_{ox}), and all terminal biases**
- ☐ **Smooth higher-order derivatives**
- ☐ **Regional charge model – key to physically-based parameter extraction**
- ☐ **Foundation to unification of MOS compact models (bulk/SOI/DG/NW/SB/DSS)**

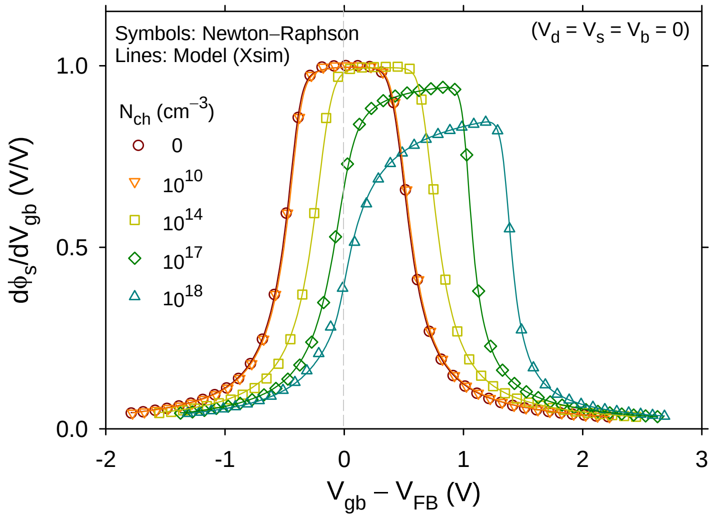
Body-Doping Scaling: High to Zero (“Undoped”)

N_{ch} = 0: exactly symmetric

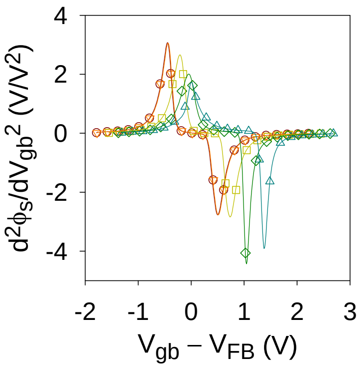
N_{ch} = n_i: not exactly symmetric

Key: $\Upsilon = \sqrt{2q\varepsilon_{Si}p_o}/C_{ox}$ has to be p_0, not N_A

$$p_0 = n_i e^{\phi_F/v_{th}} = n_i \exp\left[\sinh^{-1}\left(\frac{N_A - N_D}{2n_i}\right)\right]$$



Seamless doping scaling



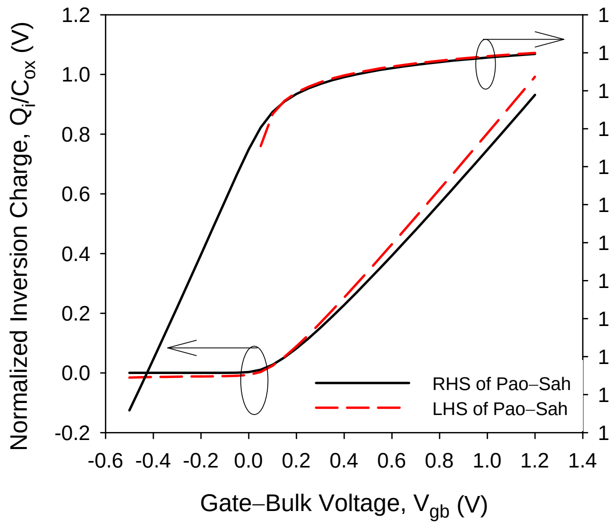
Extrinsic: $N_A - N_D > n_i$ ⇩ High temperature

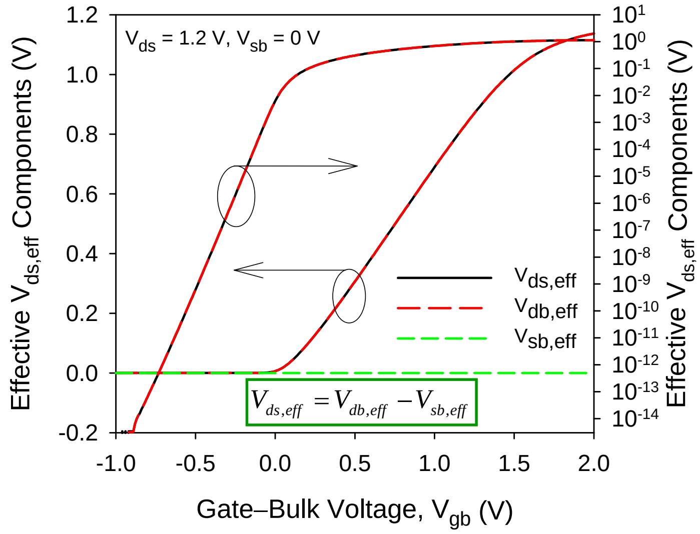
Undoped = “pure” (ideal): $N_A = N_D = 0$

“Intrinsic”: $N_A - N_D = n_i$ (temp-dependent)

Inversion Charge and Effective Drain–Source Voltage

$$q_i(y) = V_{gb} - V_{FB} - \phi_s(y) - \Upsilon\sqrt{\phi_s(y)} \xleftarrow{\text{LHS}} q_i = \frac{Q_i(y)}{C_{ox}} = V_{gt} \xrightarrow{\text{RHS}} V_{gt}(y) = \Upsilon\sqrt{\phi_s(y) + v_{th}e^{(\phi_s(y) - 2\phi_F - V_{cb})/v_{th}}} - \Upsilon\sqrt{\phi_s(y)}$$





Key to without requiring very accurate ϕ_s

Key to symmetry without V_{sb} clipping

Undoped-Body DG FinFET vs. GAA SiNW

❑ **FinFET (DG)**

$$\frac{d^2\phi}{dx^2} = \frac{qn_i}{\varepsilon_{Si}} e^{(\phi - V_c)/v_{th}}$$

❑ **First integration**

$$\boxed{V_{gf} - \phi_s = \Upsilon_i \sqrt{v_{th}\left(e^{(\phi_s - V_c)/v_{th}} - e^{(\phi_o - V_c)/v_{th}}\right)}}$$

Ignore the ϕ_o term

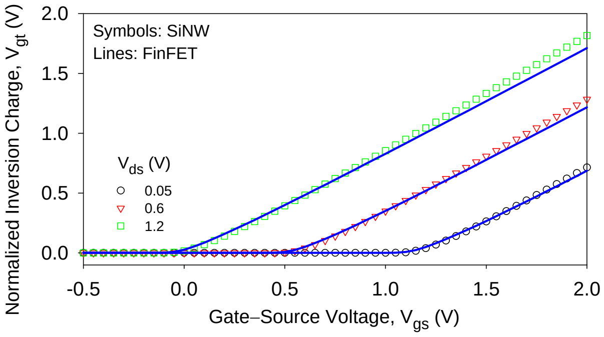
$$\boxed{\phi_s\left[V_c(y)\right] = V_{gf} - 2v_{th}\mathcal{L}\left\{\frac{\Upsilon_i}{2\sqrt{v_{th}}} e^{\left(V_{gf} - V_c\right)/2v_{th}}\right\}}$$

❑ **Second integration** $C_{ox} = \varepsilon_o K_{ox}/T_{ox}$

$$\boxed{V_{gt,c}(V_c) = \Upsilon_i \sqrt{v_{th} e^{\frac{\phi_s(V_c) - V_c}{v_{th}}}} \sin\left(\frac{\Upsilon_i C_{ox}}{\varepsilon_{Si}} \frac{T_{Si}}{4v_{th}} \sqrt{v_{th} e^{\frac{\phi_o(V_c) - V_c}{v_{th}}}}\right)}$$

❑ **SiNW (GAA)**

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right) = \frac{qn_i}{\varepsilon_{Si}} e^{(\phi - V_c)/v_{th}}$$



$$C_{ox} = \varepsilon_o K_{ox}/R\ln\left(1 + T_{ox}/R\right)$$

$$\boxed{V_{gt,c}(V_c) = \frac{Rqn_i}{2C_{ox}} e^{(\phi_s + \phi_o - 2V_c)/2v_{th}}}$$

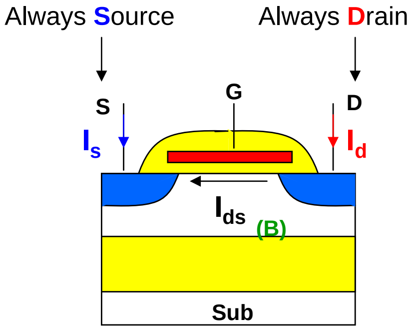
Bulk/Ground-Reference and Source/Drain by Label

❑ **S/D by convention** (nMOS)

- $V_d > V_s$: $I_{ds} > 0$ (‘D’ → ‘S’)
- $V_d < V_s$: $I_{ds} > 0$ (‘D’ ↔ ‘S’)

- By convention, nMOS I_{ds} always flows from ‘D’ to ‘S’
- Terminal swapping for $-V_{ds}$: involving $|V_{ds}|$ in model

❑ **S/D by label (layout)**



- $V_d > V_s$: $I_{ds} > 0$ (D → S)
- $V_d < V_s$: $I_{ds} < 0$ (S → D)

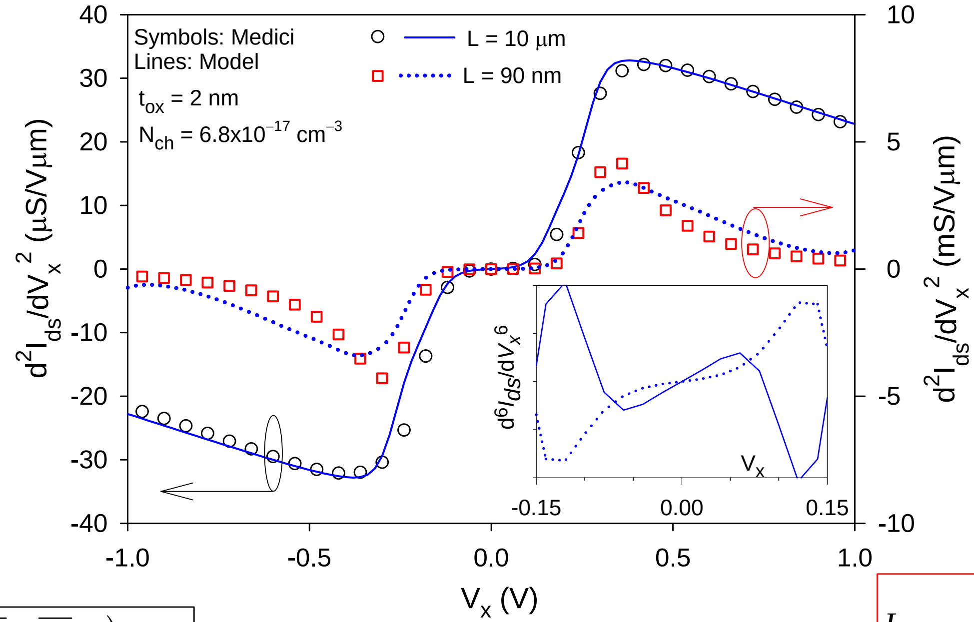
❑ **Effective drain–source voltage ($V_{ds,eff}$)**

FB: $\boxed{V_{ds,eff} = V_{d,eff} - V_{s,eff}}$ BC: $\boxed{V_{ds,eff} = V_{db,eff} - V_{sb,eff}}$

$$\boxed{\begin{aligned} I_{ds} &= \overline{\beta}\left(\overline{q_i} + \overline{A_b}v_{th}\right)V_{ds,eff} = I_d - I_s \\ &= \overline{\beta}\left(\overline{q_i} + \overline{A_b}v_{th}\right)V_{db,eff} - \overline{\beta}\left(\overline{q_i} + \overline{A_b}v_{th}\right)V_{sb,eff} \end{aligned}}$$

- **Key**: **Bulk/Ground-reference** — auto switch to B/G-ref when body is biased or floating
- Intrinsic I_{ds} is an *exact* odd function of V_{ds}
- Physical modeling of asymmetric MOS (nontrivial with “terminal swapping” for negative V_{ds})

Gummel Symmetry Test on Long/Short-Channel Bulk



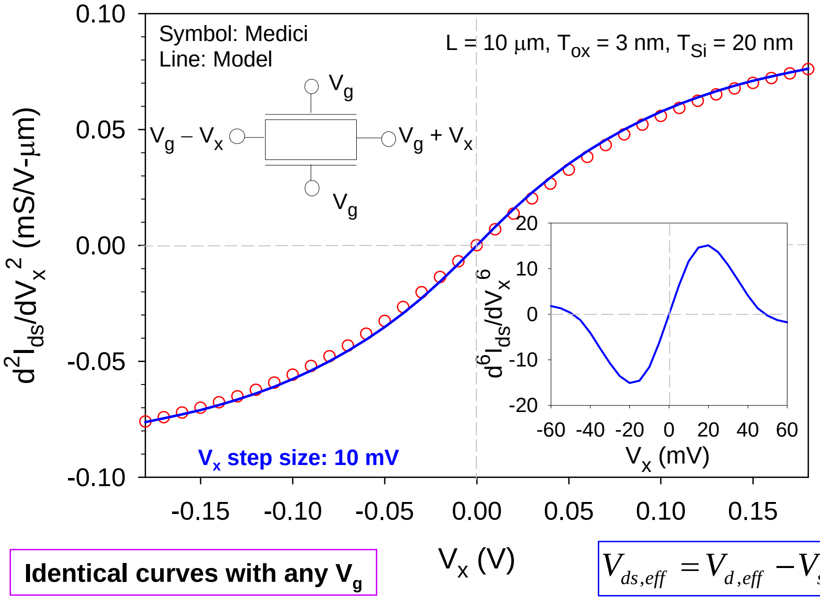
$$I_{ds0} = \overline{\beta}\left(\overline{q_i} + \overline{A}_b v_{th}\right) V_{ds,eff}$$

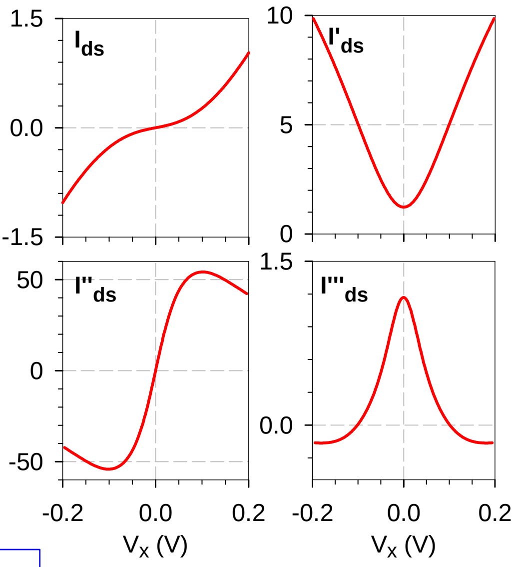
G. H. See, *et al*., T-ED, 55(2), p. 624, Feb. 2008.

$$I_{ds} = \frac{\overline{g_{vo}} I_{ds0}}{1 + R_{sd} I_{ds0} / V_{ds,eff}}$$

Gummel Symmetry Test on Undoped s-DG Without BC

“Floating body” (without body contact): **Key – “ground-referenced” model**



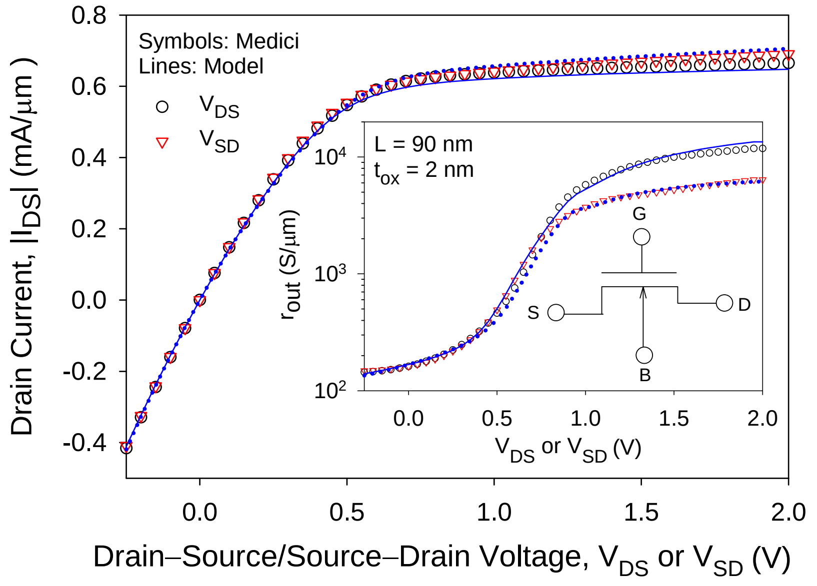


Identical curves with any V_g

$$V_{ds,eff} = V_{d,eff} - V_{s,eff}$$

G. J. Zhu, *et al*., T-ED, 55(9), p. 2526, 2008.

Modeling Asymmetric MOSFET

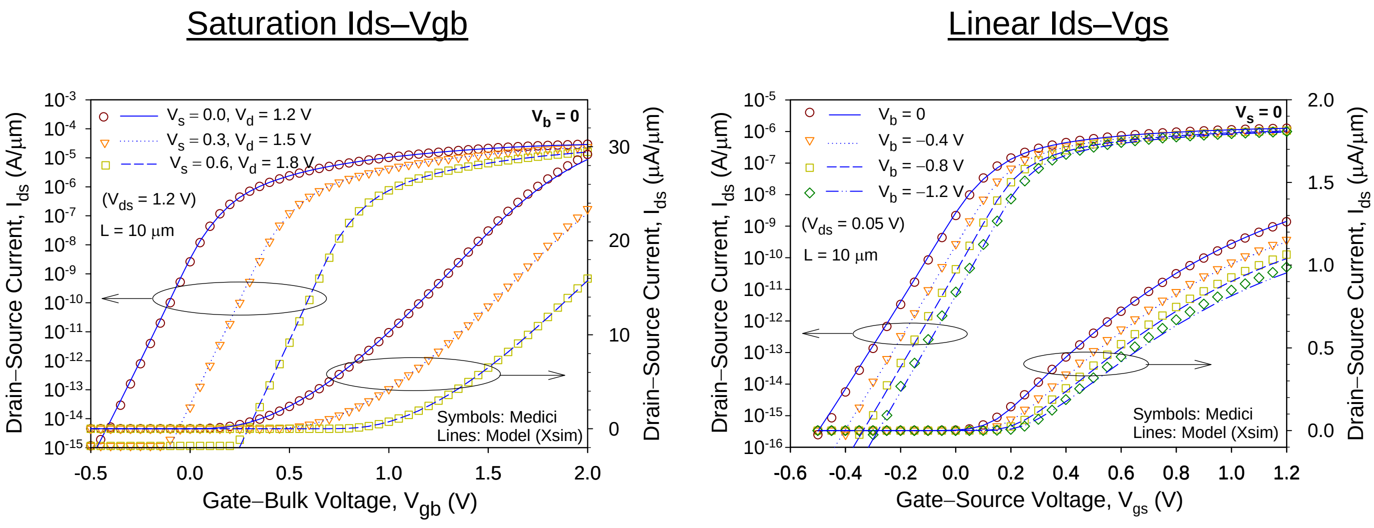


$X_{j,s}$ = 80 nm, $N_{D,s} = 10^{19}$ cm^{-3}; $X_{j,d}$ = 30 nm, $N_{D,d} = 10^{18}$ cm^{-3}

G. H. See, *et al*., T-ED, 55(2), p. 624, Feb. 2008.

- **"Source" and "Drain" by label (rather than by MOS convention); i.e., V_{DS} and V_{SD} are different**
- **Structural asymmetry (e.g., X_j, N_D) can be captured by refitting physical parameters (e.g., $v_{sat,s}$ and $v_{sat,d}$)**
- **Models based on S/D terminal swapping for negative V_{ds} at circuit level can never model asymmetric device easily (need to have two sets of symmetric model parameters)**

Bulk-Referenced Model: Transfer Characteristics

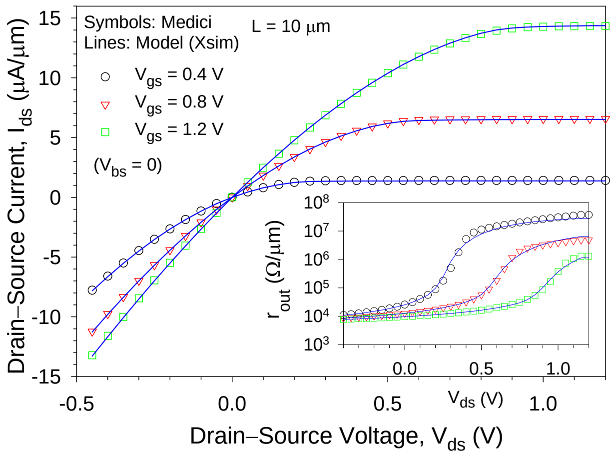

Saturation Ids–Vgb

Linear Ids–Vgs

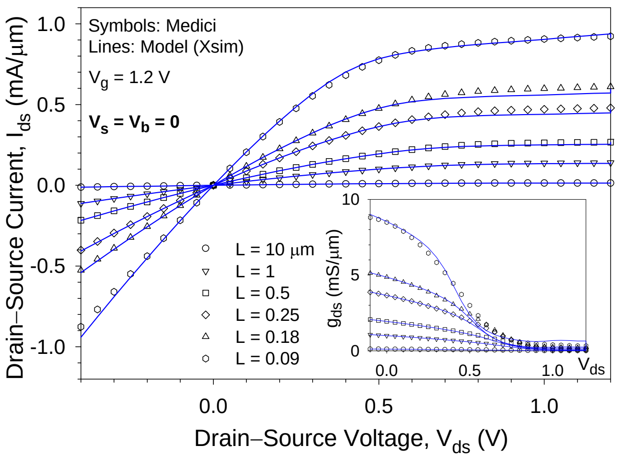
G. H. See, *et al*., T-ED, 55(2), p. 624, Feb. 2008.

Bulk-Referenced Model: Output Characteristics

Long-Channel Ids–Vds



L-Dependent Ids–Vds

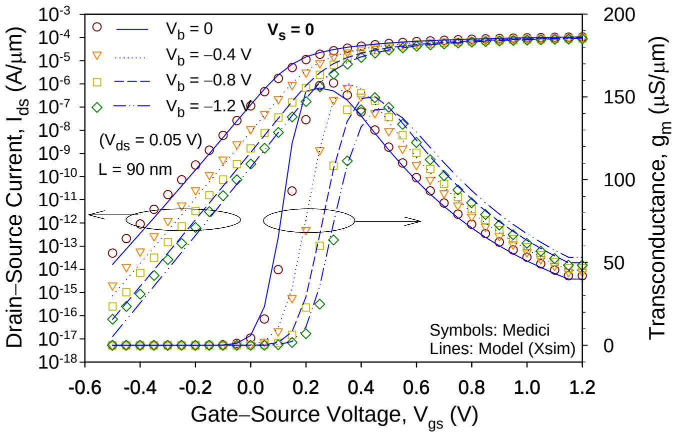


(A single smoothing δ_s)

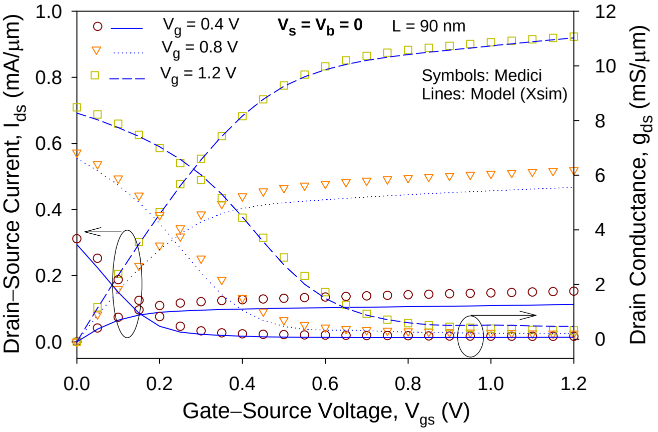
G. H. See, *et al.*, T-ED, 55(2), p. 624, Feb. 2008.

Bulk-Referenced Model: Short-Channel Characteristics

Linear Ids/gm–Vgs



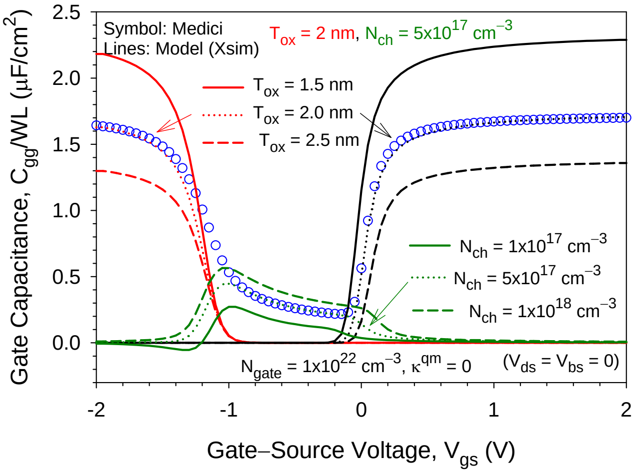
Output Ids/gds–Vds

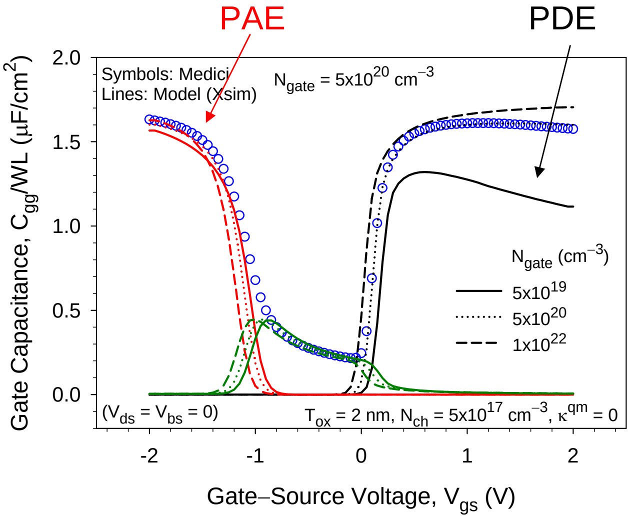


G. H. See, *et al.*, T-ED, 55(2), p. 624, Feb. 2008.

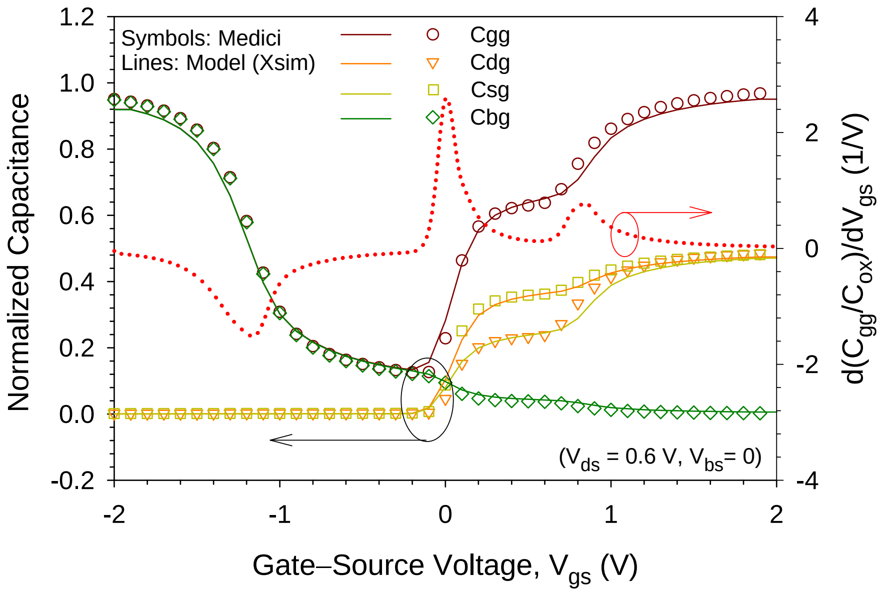
Regional Charge Model Variation: T_{ox}, N_{ch}, and N_{gate}

Using URM surface-potential solutions, physical effects can be separated in the regional charge model for meaningful and decoupled parameter extraction.

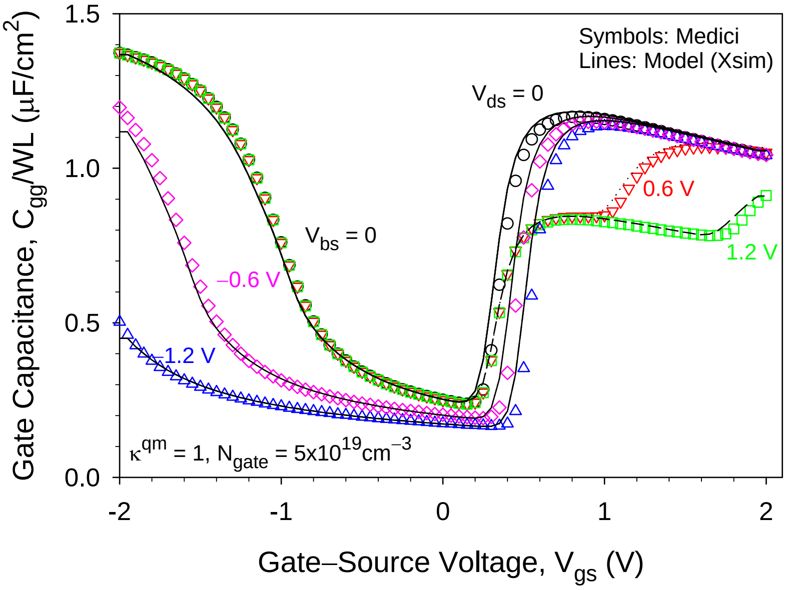




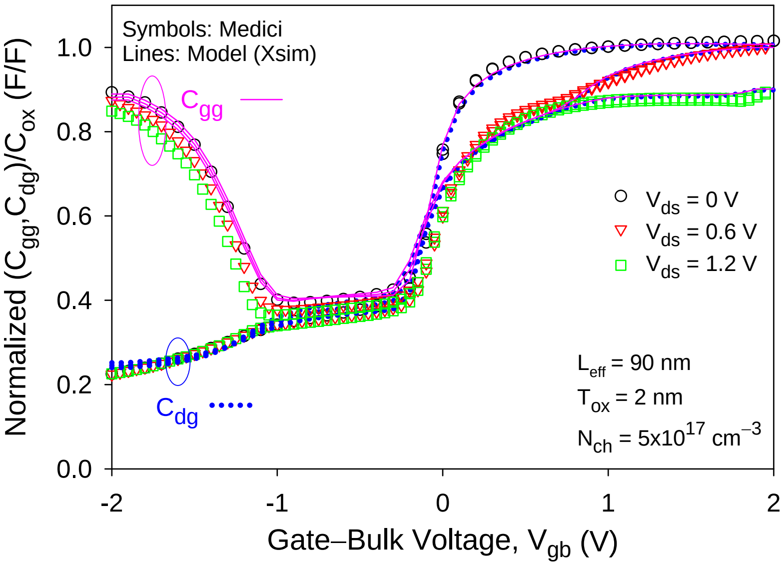
Long-Channel (Normalized) Transcapacitances



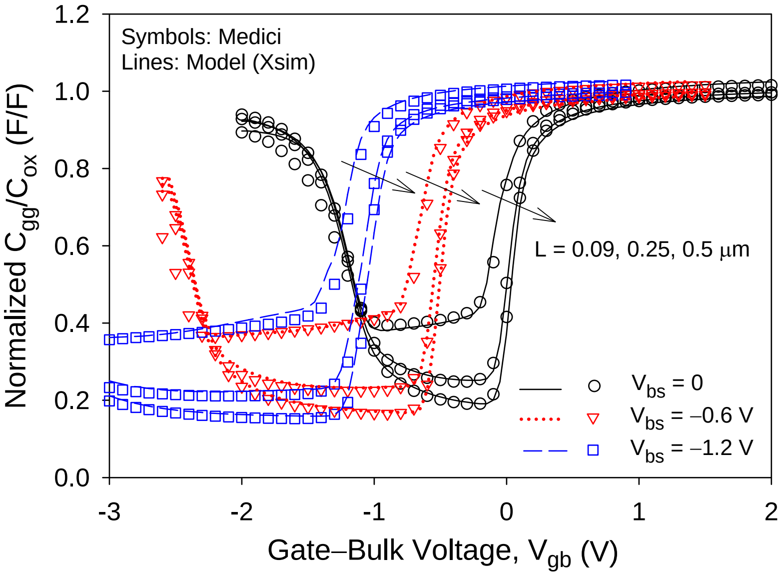
Gate Capacitance with Coupled PDE and QME



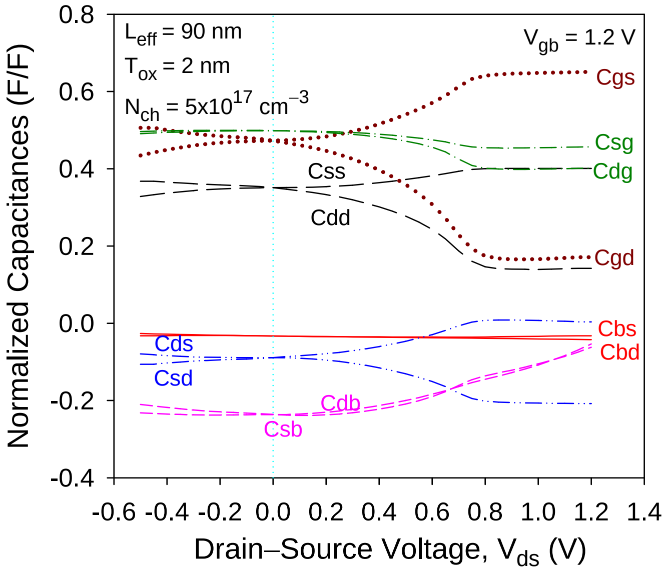
Short-Channel C_{gg} and C_{dg} with Drain-Bias Variation

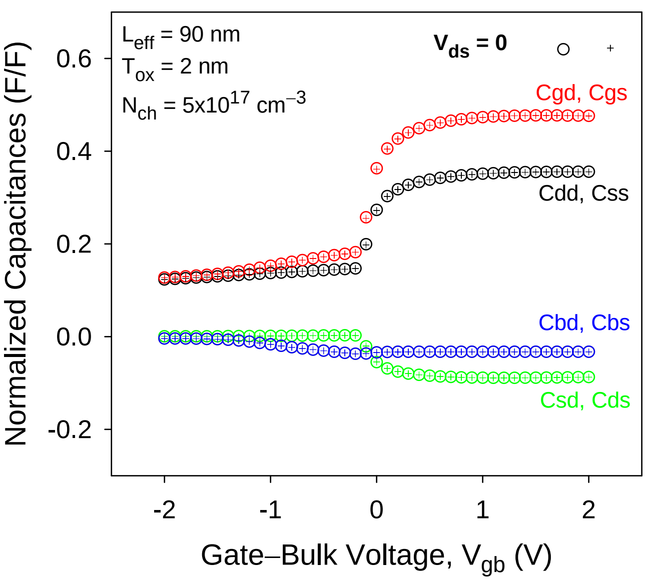


Length-Dependent C_{gg} with Body-Bias Variation



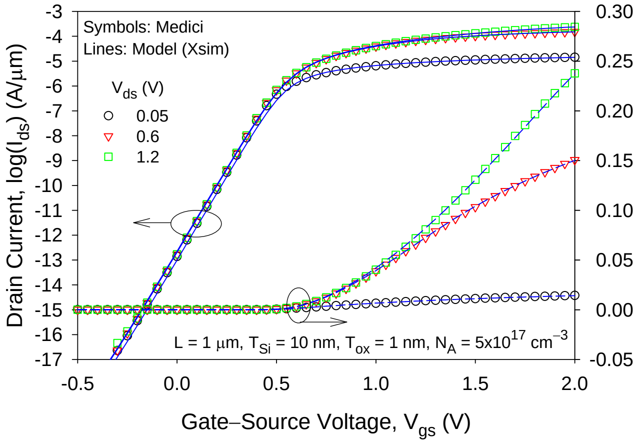
Short-Channel Transcapacitance Symmetry/Reciprocity



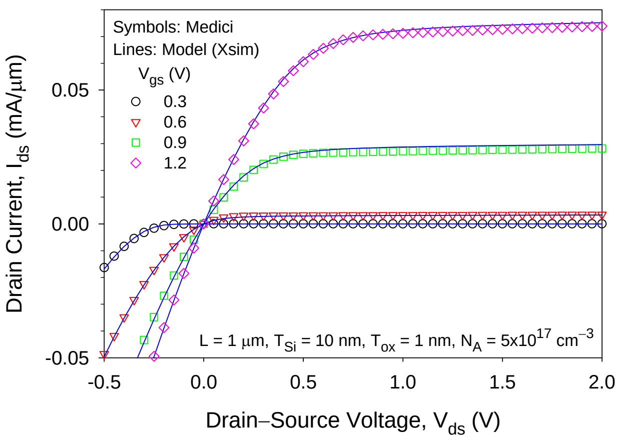


FB-SOI: Long-Channel Characteristics

Transfer Ids–Vgs



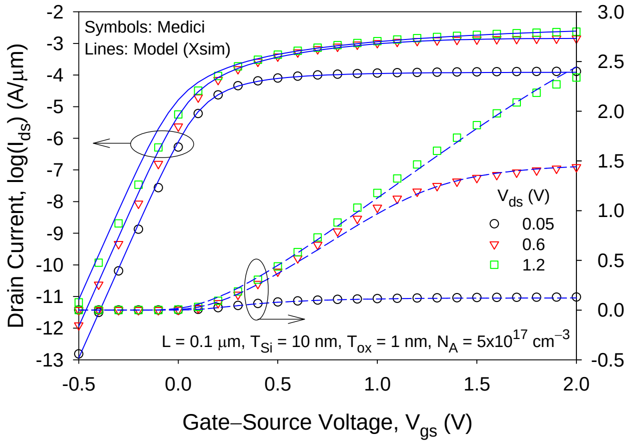
Output Ids–Vds



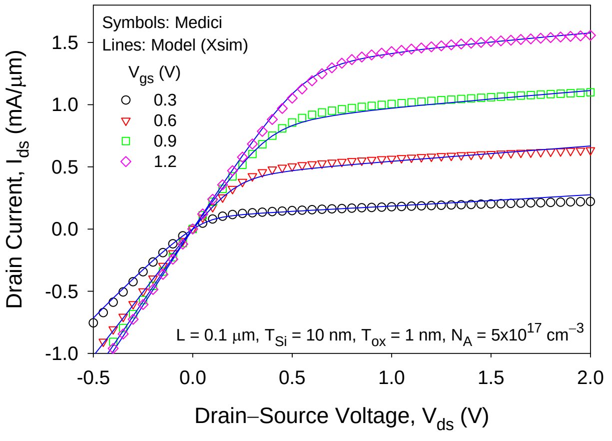
“Floating-body” SOI model comparison with Medici device.

FB-SOI: Short-Channel Characteristics

Transfer Ids–Vgs



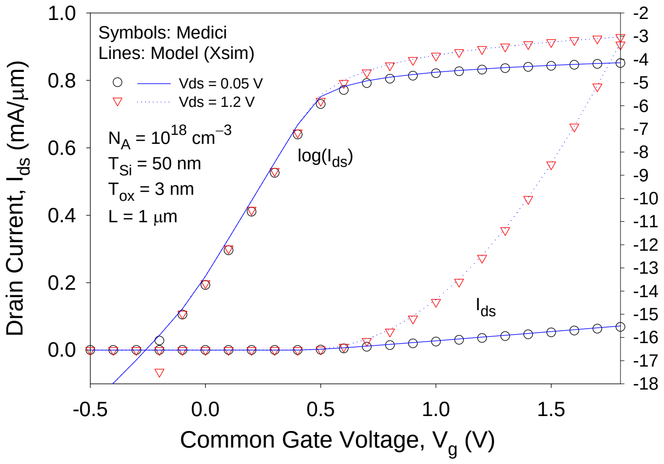
Output Ids–Vds



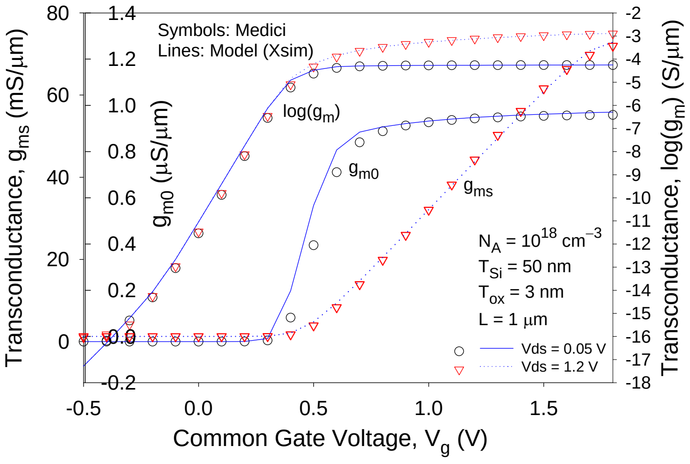
“Floating-body” SOI model comparison with Medici device.

s-DG: Evaluation in Surface-Potential-Based $I_{ds}(\phi_s)$ Model

Linear/Saturation Current



Transconductance



Doped symmetric-DG model (with depletion/volume-inversion) comparison with Medici device.

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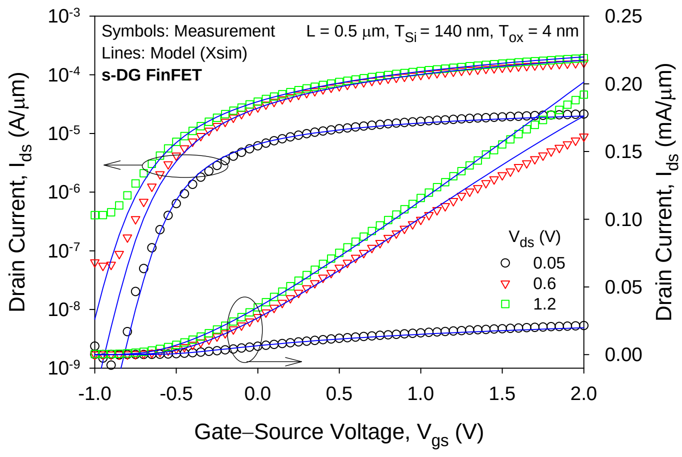
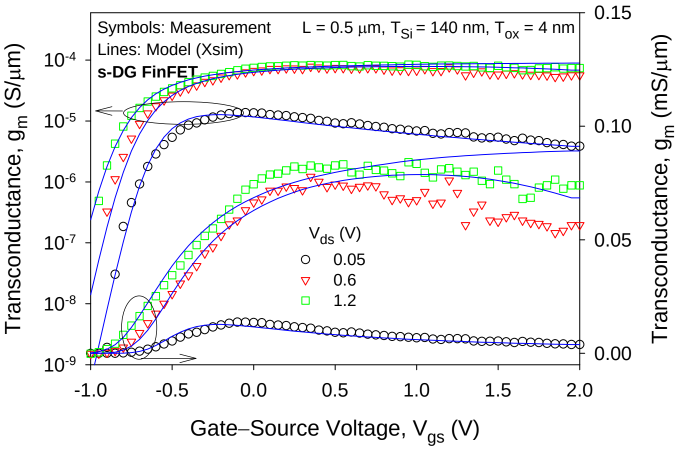
s-DG/FinFET: Short-Channel Transfer Characteristics

Transfer Ids–Vgs



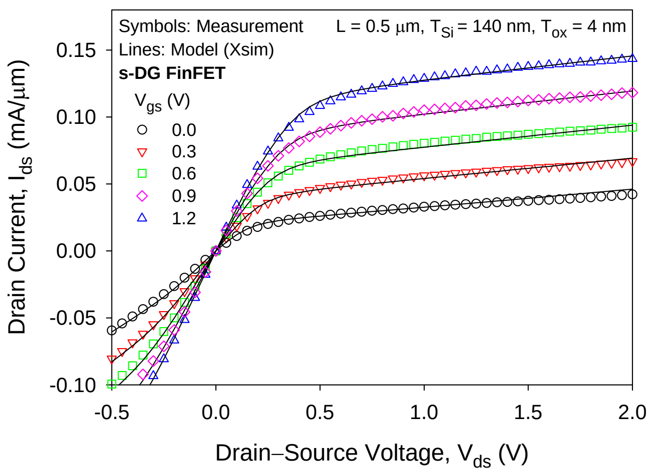
Transfer gm–Vgs



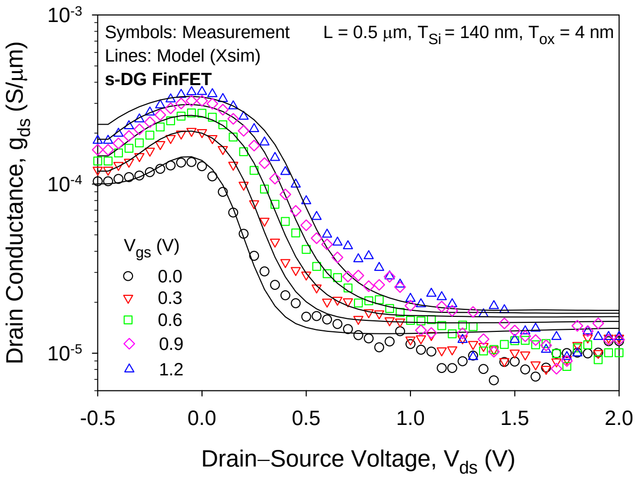
Symmetric-DG FinFET model comparison with Measurement.

s-DG/FinFET: Short-Channel Output Characteristics

Output Ids–Vds



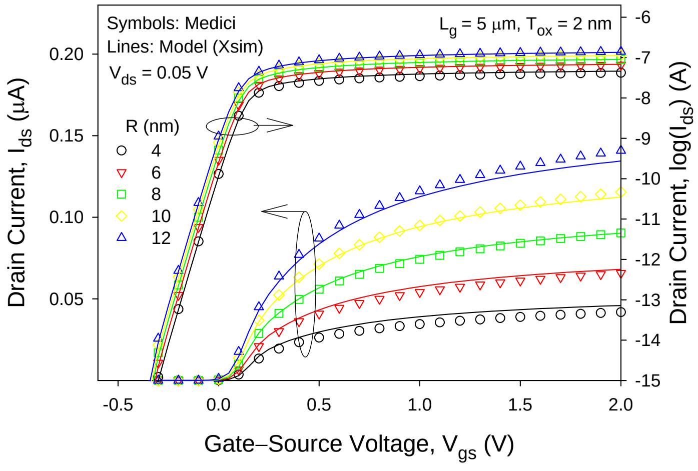
Output gds–Vds



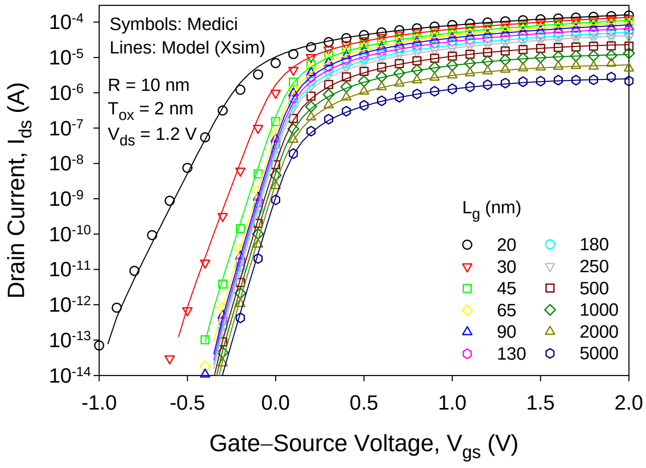
Symmetric-DG FinFET model comparison with Measurement.

SiNW: Model Scalability with Radius and Gate Length

Radius Variation



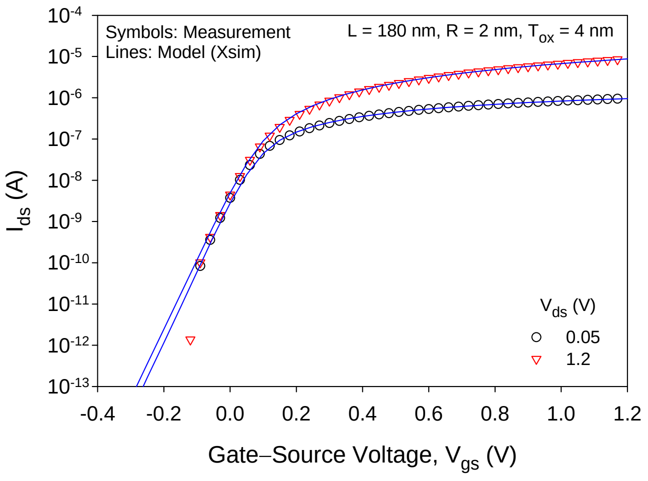
Gate Length Variation



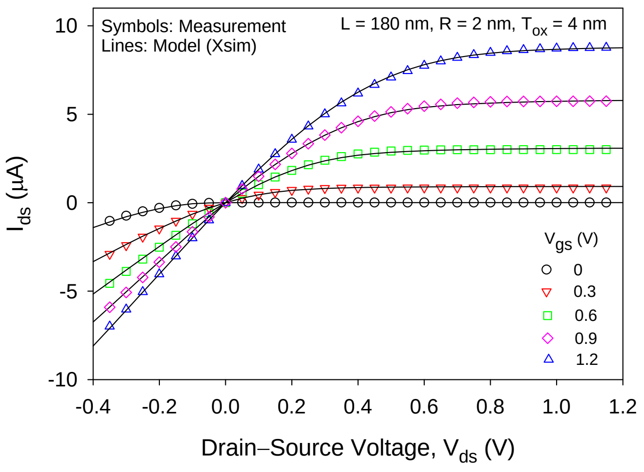
Si-nanowire model comparison with Medici device.

SiNW: Model Applied to Measured SiNW

Transfer Ids–Vgs



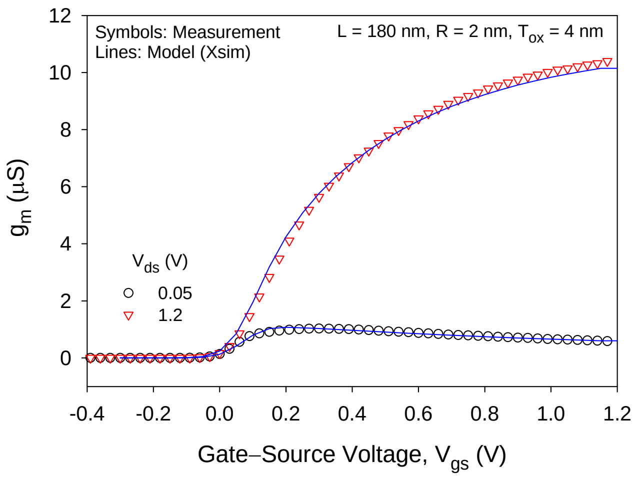
Output Ids–Vds



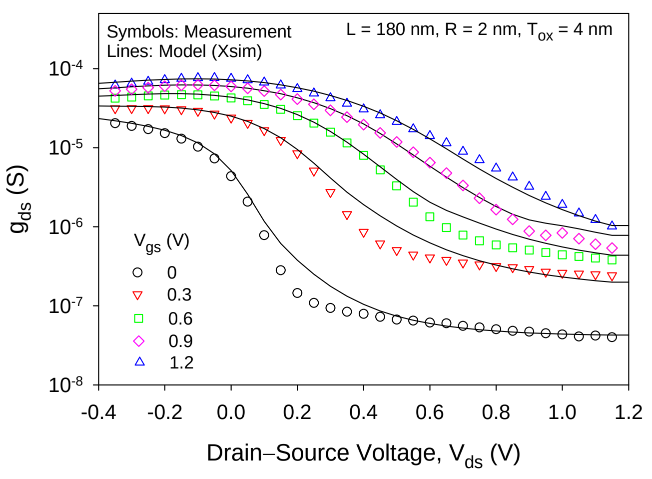
Si-nanowire model comparison with Measurement.

SiNW: Model Applied to Measured SiNW

1st-order Transfer gm–Vgs



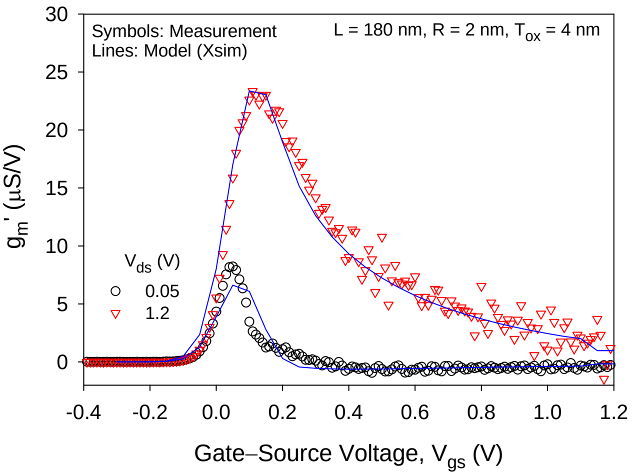
1st-order Output gds–Vds



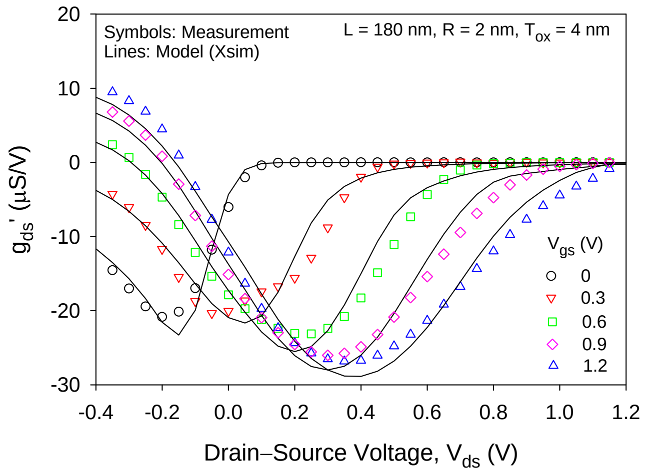
Si-nanowire model comparison with Measurement.

SiNW: Model Applied to Measured SiNW

2nd-order Transfer gm'–Vgs

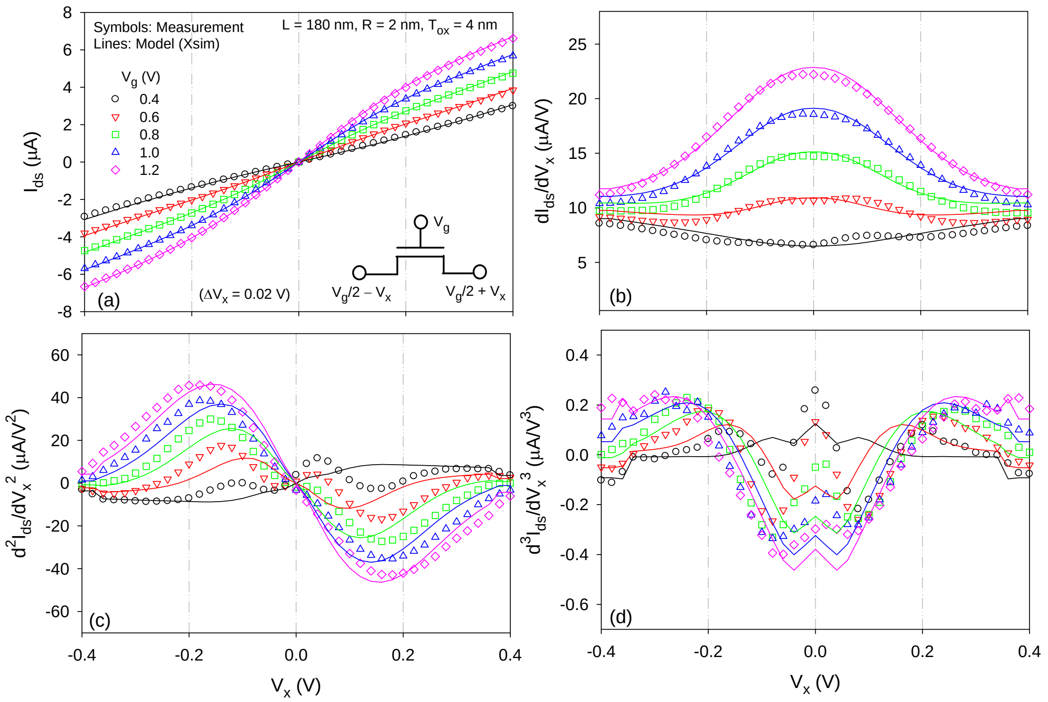


2nd-order Output gds'–Vds

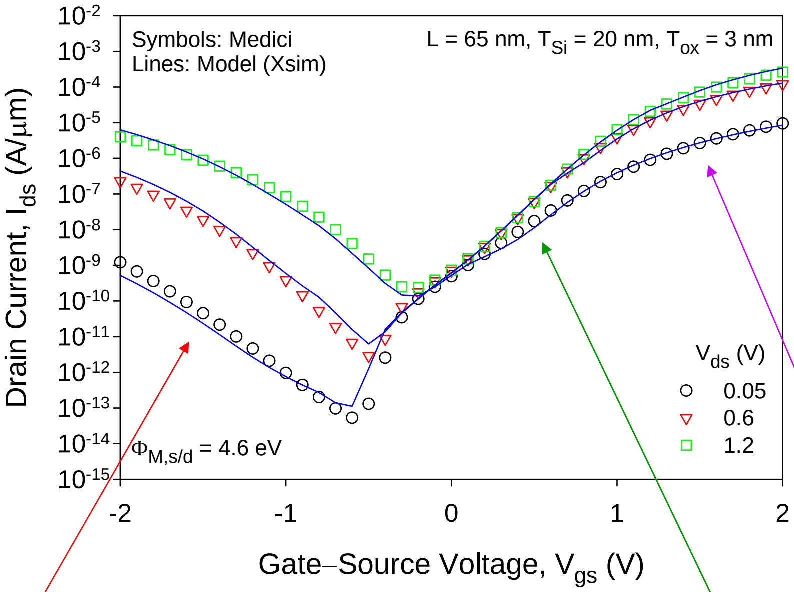


Si-nanowire model comparison with Measurement.

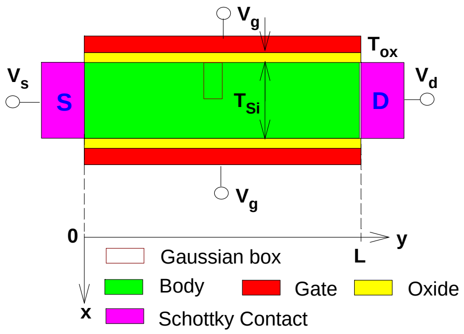
GAA SiNW: Gummel Symmetry Test (Measurement)



Schottky-Barrier MOSFET: Ambipolar Current



Ambipolar possible in undoped SB-MOS with mid-gap $\Phi_{M,s/d}$



- Medici: two-carrier
- Xsim: sum of two unipolar ($I_{ds,n}$ + $I_{ds,p}$)

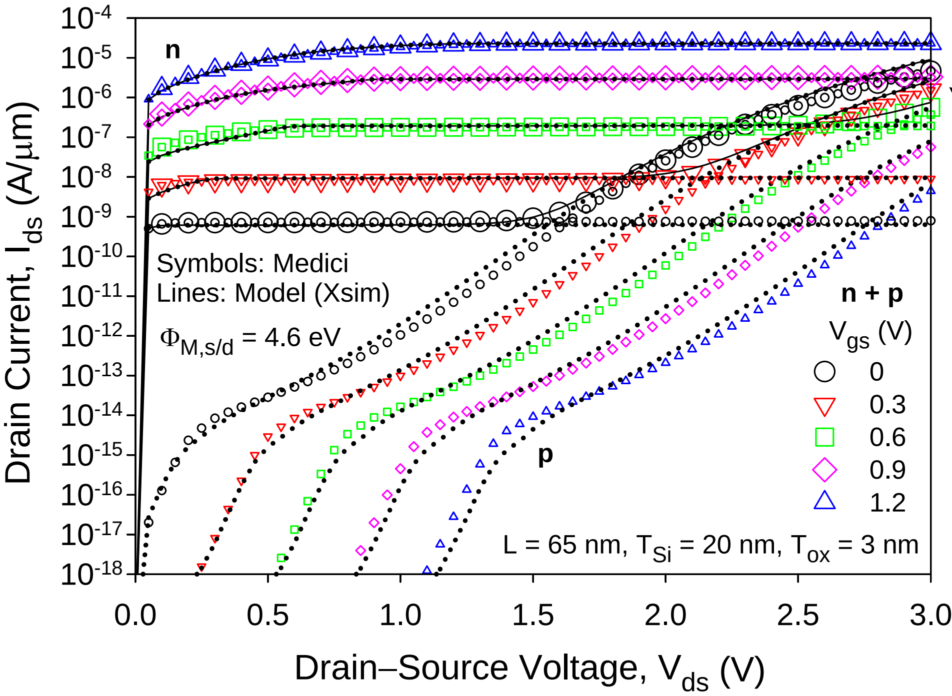
Hole tunneling

No drift-diffusion!

Electron thermionic

Electron tunneling

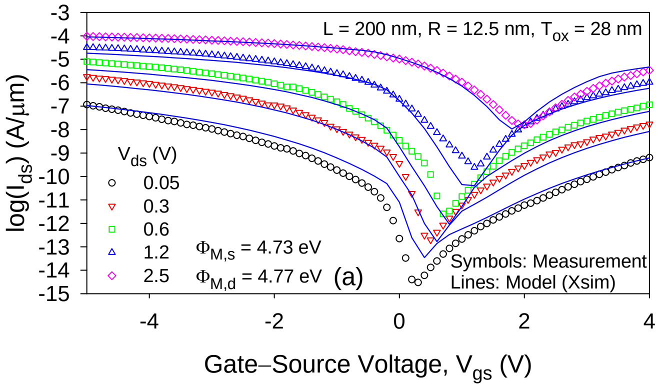
SB-MOS: Total Current = (Electron + Hole) Currents



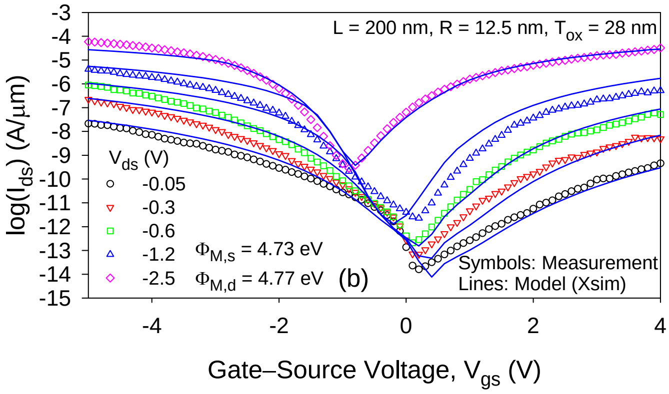
Ambipolar (In + Ip) current

SB-MOS: Model Applied to Measured SB-MOS

nMOS operation (+Vds)



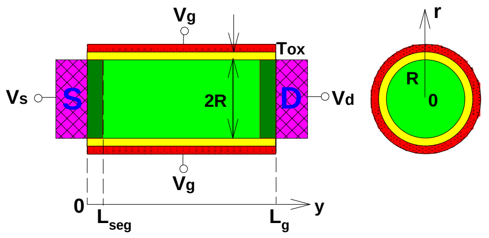
pMOS operation (–Vds)



SB-MOS model comparison with Measurement.
(Same model and same device with different bias)

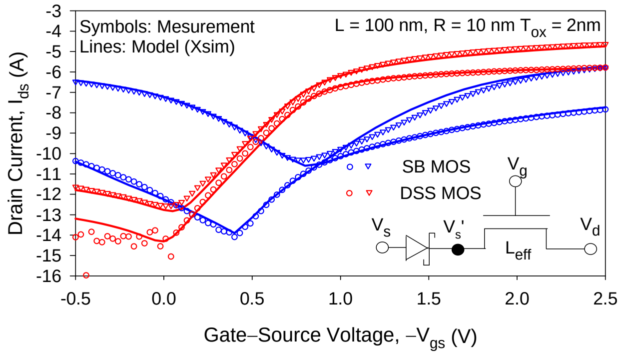
G. J. Zhu, *et al*., T-ED, 56(5), p. 1100, May 2009.

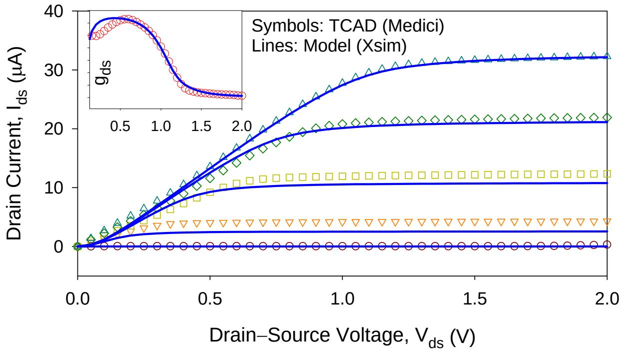
DSS-SiNW: Subcircuit Model



Dopant-Segregated Schottky (DSS) SiNW:

- Thermionic/tunneling (TT) + drift-diffusion (DD)
- The unique **convex** curvature in Ids–Vds can only be modeled by a subcircuit model: SBD (TT) + MOS (DD)





DSS-SiNW MOS **subcircuit model** comparison with Measurement.

G. J. Zhu, *et al*., SSDM, p. 402, Oct. 2009.

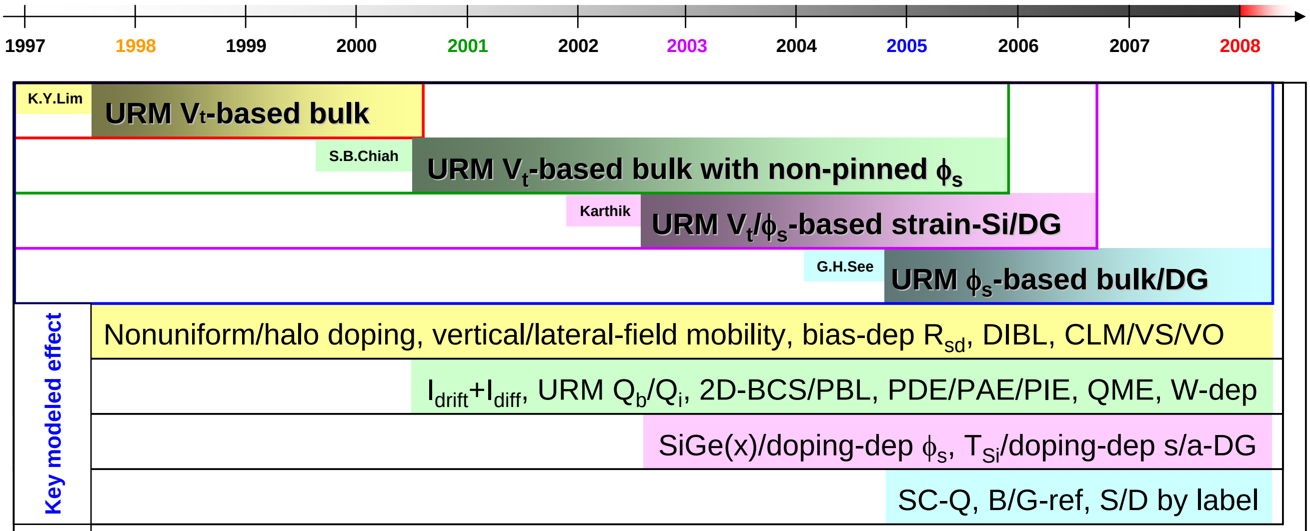
Xsim: Basic Model Parameters

Total: 33 basic parameters

DG/SiNW has less parameters

- ☐ **Physical parameters [6]**
  - Oxide thickness (T_{ox}), S/D junction depth (X_j)
  - Doping: channel (N_{ch}), gate (N_{gate}), S/D (N_{sd}), overlap (N_{ov})
- ☐ **AC/Poly/QM parameters [8]**
  - Bulk charge sharing (BCS): channel (λ_c), gate (λ_p), overlap (λ_{ov})
  - Potential barrier lowering (PBL): accumulation (α_{acc}), depletion/inversion (α_{ds})
  - Extrinsic: lateral spread (σ), inversion/bulk charge factor (ν_i, ν_b)
- ☐ **DC parameters [19]**
  - Mobility: vertical-field mobility (μ, μ_2, μ_3, ν)
  - Effective field: vertical (ζ_n, ζ_b), lateral (δ_L)
  - PBL: accumulation (α_{acc}), depletion/inversion (α_{ds}), long-channel DIBL (α_{dibl})
  - BCL/lateral-doping: BCL (λ), halo-peak (κ), halo-spread (β), halo-centroid (l_μ)
  - Series resistance: bias-dependent (υ), bias-independent (ρ)
  - Velocity saturation (v_{sat}), velocity overshoot (ξ), effective D/S voltage (δ_s)
- ☐ **Smoothing parameters** — internal model requirement

Xsim: History, Evolution, and Philosophy



URM V_t-based bulk

URM V_t-based bulk with non-pinned ϕ_s

URM V_t/ϕ_s-based strain-Si/DG

URM ϕ_s-based bulk/DG

Nonuniform/halo doping, vertical/lateral-field mobility, bias-dep R_{sd}, DIBL, CLM/VS/VO

$I_{drift}+I_{diff}$, URM Q_b/Q_i, 2D-BCS/PBL, PDE/PAE/PIE, QME, W-dep

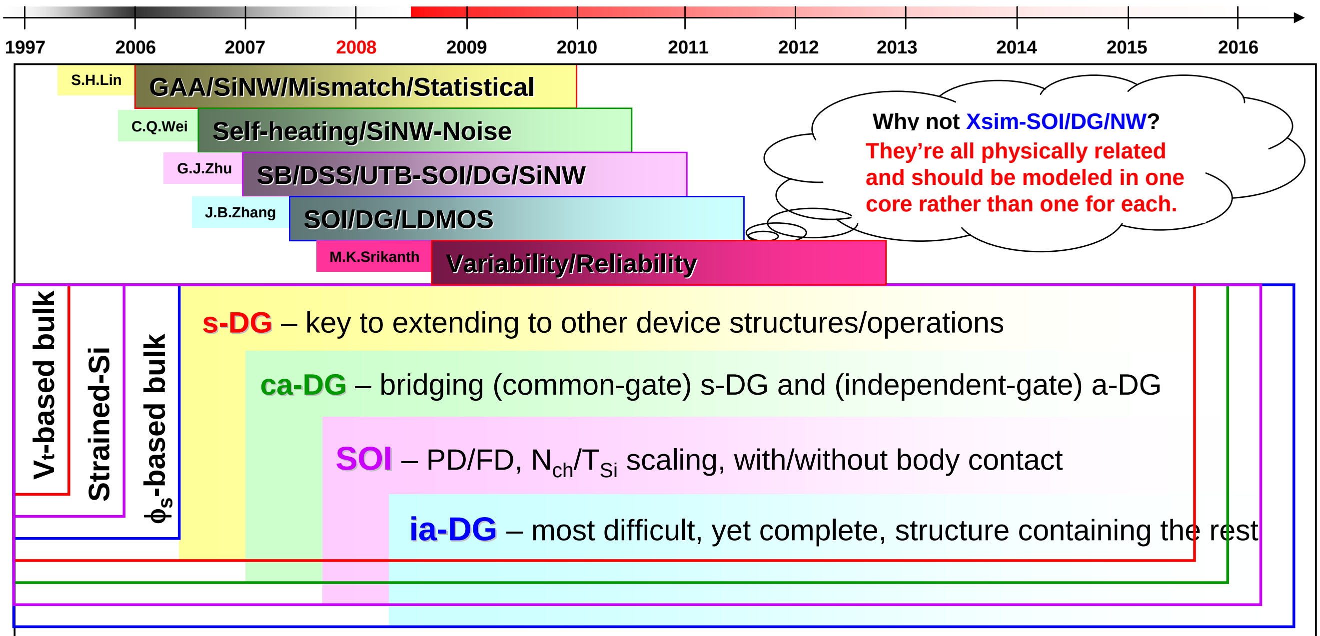
SiGe(x)/doping-dep ϕ_s, T_{Si}/doping-dep s/a-DG

SC-Q, B/G-ref, S/D by label

Philosophy

- **URM**: Unified Regional Modeling approach — ***single-piece*** physics-based regional solutions
- New model/effect includes old ones as special cases — ***extendibility*** and backward compatibility
- One/two-iteration parameter extraction — minimum data requirement and ***predictability***
- **Selectable accuracy** within one parameter set — consistent full/simple model for **design**/**verification**

Xsim: Future and Ultimate Goal



Why not **Xsim-SOI/DG/NW**?
They're all physically related and should be modeled in one core rather than one for each.

s-DG – key to extending to other device structures/operations

ca-DG – bridging (common-gate) s-DG and (independent-gate) a-DG

SOI – PD/FD, N_{ch}/T_{Si} scaling, with/without body contact

ia-DG – most difficult, yet complete, structure containing the rest

Ultimate Goal — Unification of MOS models, with *seamless* transitions across device types/operations

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❑ **Current team members (PhD students)**

- ***Shihuan Lin***
- ***Chengqing Wei***
- ***Guojun Zhu***
- ***Junbin Zhang***
- ***Machavolu Srikanth***

Research Staff:

- ***Dr Zuhui Chen***
- ***Ramachandran Selvakumar***
- ***Yafei Yan***
- ***William Chandra***

❑ **Previous team members (PhD/MEng students)**

- ***Dr Khee Yong Lim***
- ***Yuwen Wang***
- ***Dr Siau Ben Chiah***
- ***Dr Karthik Chandrasekaran***
- ***Dr Guan Huei See***
- ***Guan Hui Lim***

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- ***Institute for Sustainable Nanoelectronics (ISNE)***
- ***Atomistix Asia Pacific Pte Ltd***
- ***Institute of Microelectronics***

Our relevant publications: **http://www.ntu.edu.sg/home/exzhou/Research/DOUST/pub.htm**