CMOS ANALOG DESIGN USING ALL-REGION MOSFET MODELING

Márcio Cherem Schneider and Carlos Galup-Montoro

Federal University of Santa Catarina, Brazil

- Compact MOSFET model
- Circuit examples:
  - MOSFET sizing in amplifiers
  - Self-biased current reference

COMPACT MOSFET MODEL

Definitions:

C'_{ox}	oxide capacitance per unit area	ϕ_s	surface potential
Q'_I	inversion charge per unit area	V_{FB}	flat-band potential
Q'_B	bulk charge per unit area	V_G	gate-to-bulk voltage

Charge sheet approximation of the inversion charge

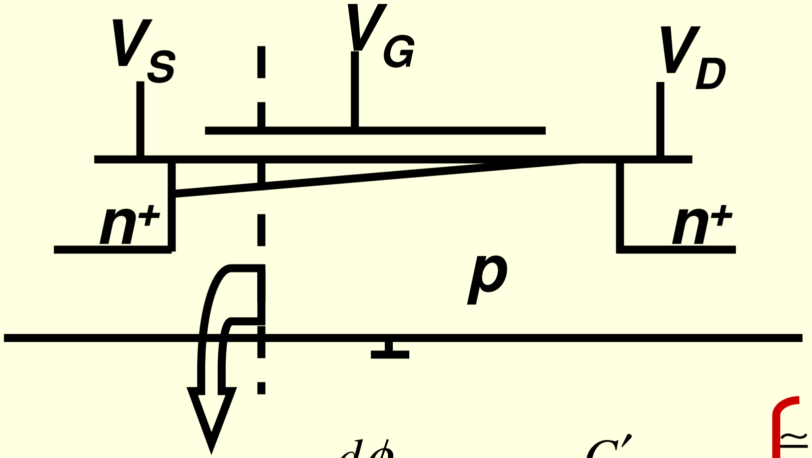
$$Q'_I = -C'_{ox}\left(V_G - V_{FB} - \phi_s\right) - Q'_B$$

- For constant V_G, it follows that

$$dQ'_I = C'_{ox}d\phi_s - dQ'_B = (C'_{ox} + C'_b)d\phi_s = nC'_{ox}d\phi_s$$

$$n = 1 + \frac{C'_b(V_G)}{C'_{ox}} = n(V_G)$$

UNIFIED CHARGE CONTROL MODEL (UCCM)-1



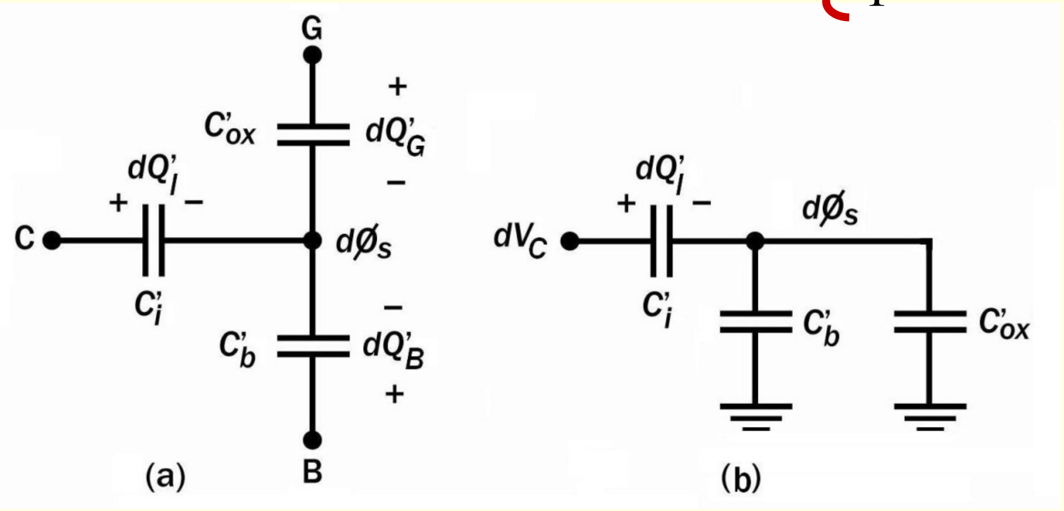
$$C'_{ox}+C'_b=nC'_{ox}$$

$$n=n(V_G)$$

$$dQ'_I=nC'_{ox}d\phi_s$$

$$C'_i=-\frac{Q'_I}{\phi_t} \qquad \phi_t=\frac{kT}{q}$$

$$\frac{d\phi_s}{dV_C}=\frac{C'_i}{C'_i+C'_{ox}+C'_b}\begin{cases}\simeq -\dfrac{Q'_I}{nC'_{ox}\phi_t}<1 & \text{WI}\\ \simeq 1 & \text{SI}\end{cases}$$



$$\Downarrow$$

$$\boxed{dV_C=dQ'_I\left(\frac{1}{nC'_{ox}}-\frac{\phi_t}{Q'_I}\right)}$$

$$V_S\le V_C\le V_D$$

UNIFIED CHARGE CONTROL MODEL (UCCM)-2

Integrating $dV_C = dQ'_I\left(\frac{1}{nC'_{ox}} - \frac{\phi_t}{Q'_I}\right)$ between V_C and V_P yields UCCM

$$\boxed{V_P - V_C = \frac{Q'_{IP} - Q'_I}{nC'_{ox}} + \phi_t \ln\left(\frac{Q'_I}{Q'_{IP}}\right)}$$

$Q'_{IP} = -nC'_{ox}\phi_t$ Thermal charge

$q'_I = \frac{Q'_I}{-nC'_{ox}\phi_t}$ Normalized inversion charge density

Normalized UCCM $\boxed{V_P - V_C = \phi_t(q'_I - 1 + \ln q'_I)}$

CHARGE-SHEET MODEL (CSM)

drift diffusion

$$\left.\begin{array}{c} I_D = -\mu W Q_I' \dfrac{d\phi_s}{dy} + \mu W \phi_t \dfrac{dQ_I'}{dy} \\[2em] dQ_I' = nC_{ox}' d\phi_s \end{array}\right\}$$

drift diffusion

$$I_D = \frac{\mu W}{L}\left[\frac{Q_{IS}'^{\,2} - Q_{ID}'^{\,2}}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right]$$

$$S = \frac{W}{L}$$

Normalization (specific) current $I_S = \mu C_{ox}' n \dfrac{\phi_t^2}{2} S$

Sheet (or square) normalization current $I_{SH} = \mu C_{ox}' n \dfrac{\phi_t^2}{2}$

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right] = S I_{SH}\left[i_f - i_r\right]$$

WEAK, MODERATE, STRONG INVERSION

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

$$\boxed{i_{f(r)} = {q'_{IS(D)}}^2 + 2q'_{IS(D)} \Rightarrow q'_{IS(D)} = \sqrt{1+i_{f(r)}} - 1}$$

WI	MI	SI
$i_f < 1$	$1 < i_f < 100$	$100 < i_f$
$q'_I < 0.4$	$0.4 < q'_I < 9$	$9 < q'_I$

FORWARD AND REVERSE CURRENTS

Long-channel MOSFET $I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D)$

I_F: forward current I_R: reverse current

(Forward) Saturation

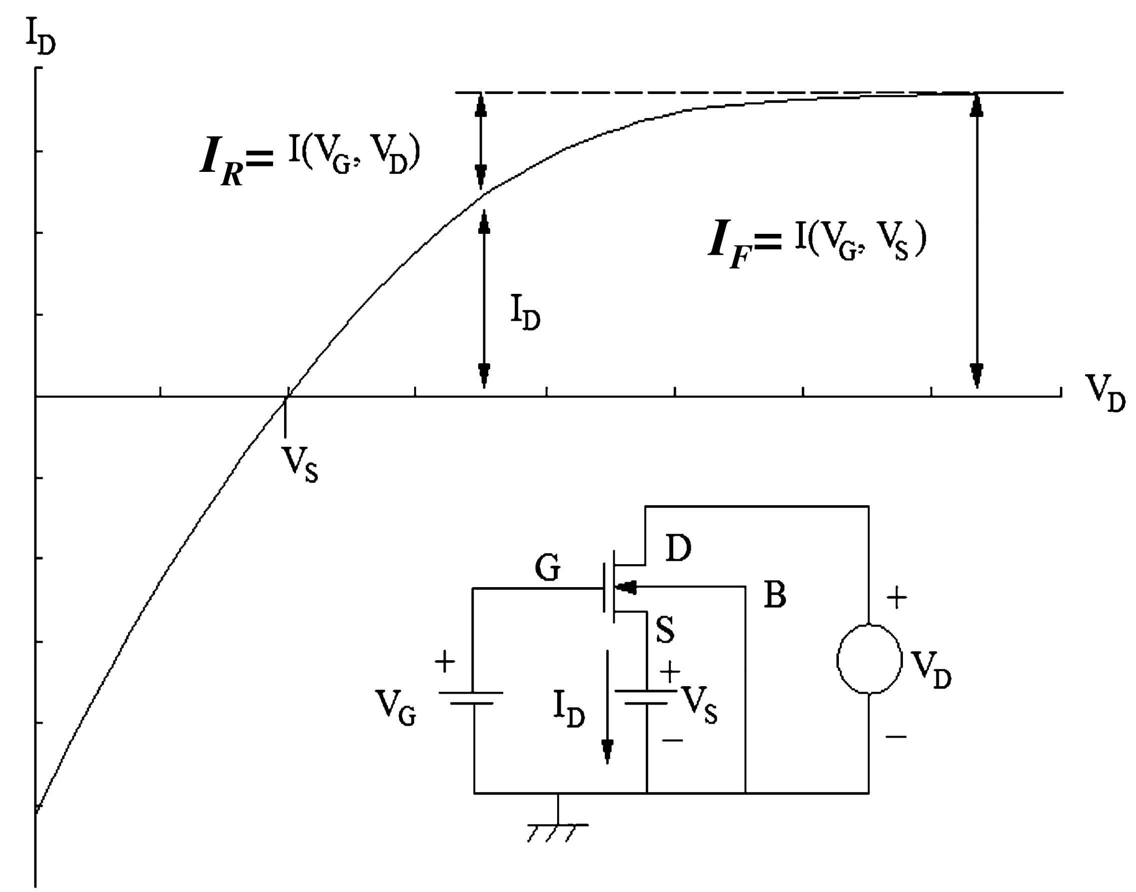
$$I_D = I_F - I_R \cong I_F$$

Triode

$$I_D = I_F - I_R$$

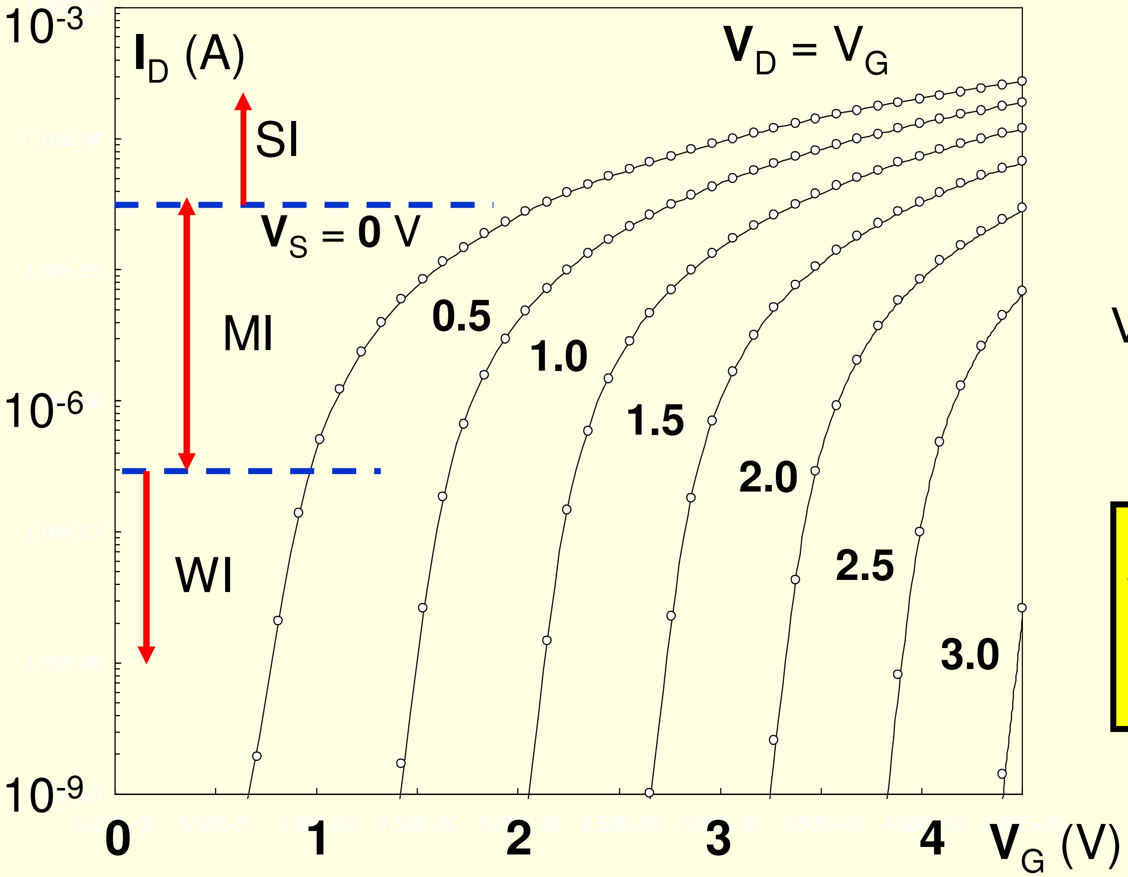
Triode for $V_{DS} \rightarrow 0$

$$I_F \cong I_R; \quad I_D = I_F - I_R << I_F$$

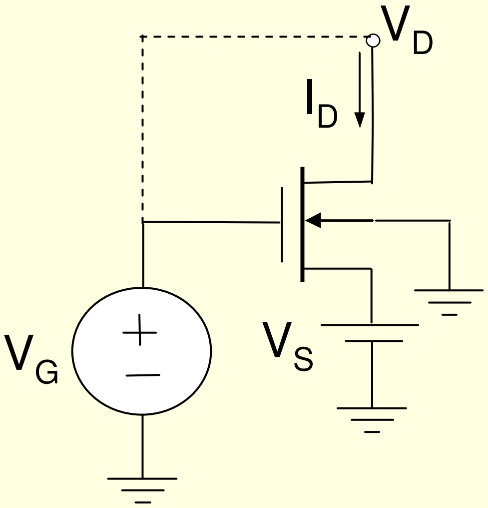


UNIFIED I-V RELATIONSHIP (UICM)

$$\boxed{V_P - V_S = \phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right]}$$



Common-source characteristics

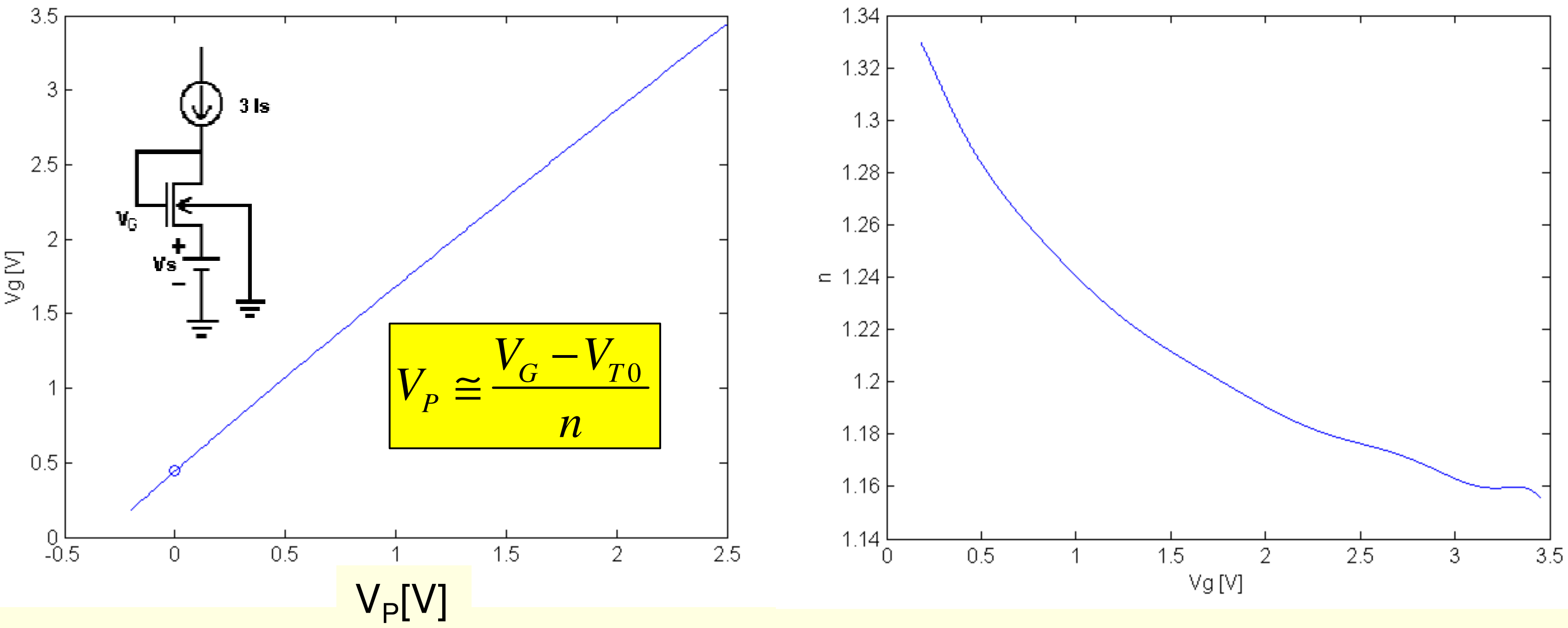


$$\boxed{\begin{array}{c} I_D = I_S\left[i_f - i_r\right] \cong I_S i_f \\ \text{since} \quad i_f >> i_r \end{array}}$$

PINCH-OFF VOLTAGE AND SLOPE FACTOR

$i_f=3$ at pinch-off ⇒

$$\boxed{V_P - V_S = 0 = \left[\sqrt{1+3} - 2 + \ln\left(\sqrt{1+3} - 1\right)\right]}$$



$$\boxed{V_P \cong \frac{V_G - V_{T0}}{n}}$$

Pinch-off voltage and slope factor as functions of V_G [0.18 μm CMOS technology].

TRANSCONDUCTANCES

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B$$

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0$$

Calculation of g_{ms}

$$\left.\begin{aligned} I_D &= I_F - I_R = I_S\left[i_f - i_r\right] \\ i_{f(r)} &= q'^{\,2}_{IS(D)} + 2q'_{IS(D)} \\ V_P - V_C &= \phi_t\left(q'_I - 1 + \ln q'_I\right) \end{aligned}\right\}$$

$$\boxed{g_{ms} = -I_S\frac{di_f}{dV_S} = -\mu\frac{W}{L}Q'_{IS} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f} - 1\right)}$$

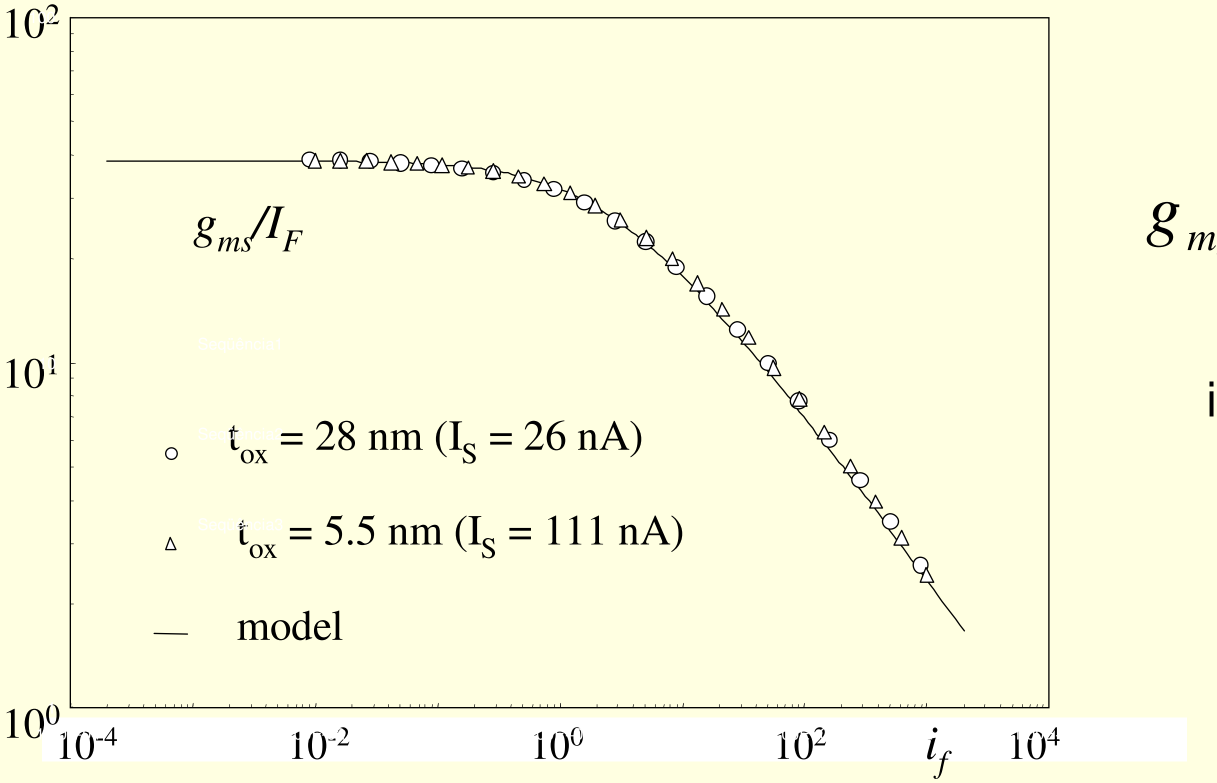
TRANSCONDUCTANCE-TO-CURRENT RATIO

Transconductance
-to-current ratio

$$\boxed{\frac{g_{ms(d)}\phi_t}{I_{F(R)}} = \frac{2}{\sqrt{1+i_{f(r)}}+1}}$$

$$\rightarrow \cong 1 \longrightarrow \text{WI } (i_f<1)$$

$$\rightarrow \cong \frac{2}{\sqrt{i_{f(r)}}} \longrightarrow \text{SI } (i_f>>1)$$

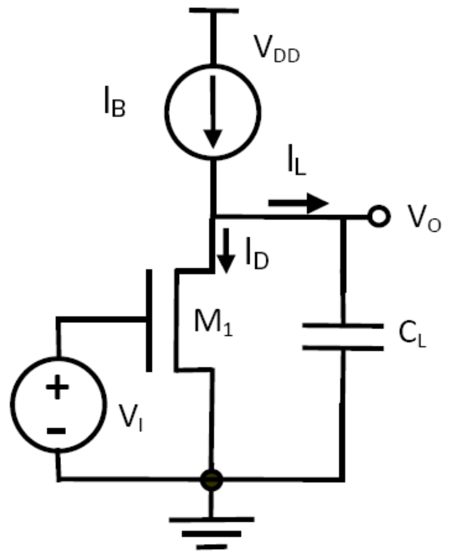


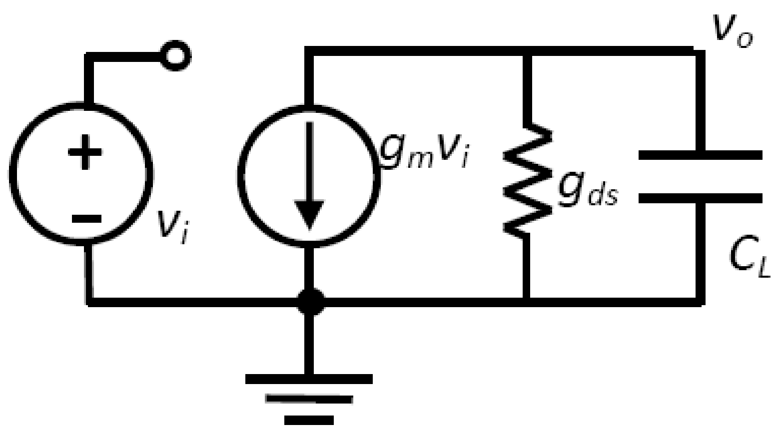
$$g_{mg} = \frac{g_{ms} - g_{md}}{n}$$

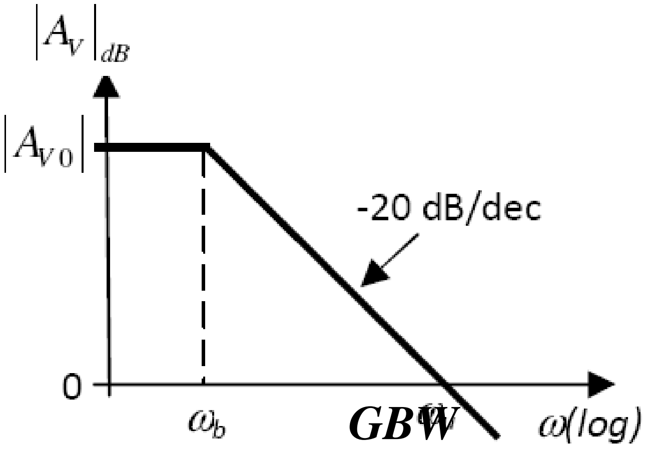
in saturation:

$$g_{mg} = \frac{g_{ms}}{n}$$

COMMON-SOURCE STAGE







$$v_o \cong -\frac{g_m}{j\omega C_L} v_i$$

for $\omega >> \omega_b$

EXAMPLE: GBW = 10 MHz, C_L = 10 pF

$\mu C'_{ox}$ = 80·10^{-6} A/V^2, n = 1.35

$$g_m = 2\pi \cdot GBW \cdot C_L = 628\ \mu\text{A/V}$$

W/L	I_{Dsi} (μA)[1]	I_D (μA)[2]
∞	0	22
500	6.6	28.6
100	33.2	55.2
50	66.4	88.4
10	332	354

[1] Strong inversion model

[2] Accurate all-region MOSFET model

ALL-REGION MOSFET MODEL

$$I_D = I_{WI} + I_{Dsi}$$

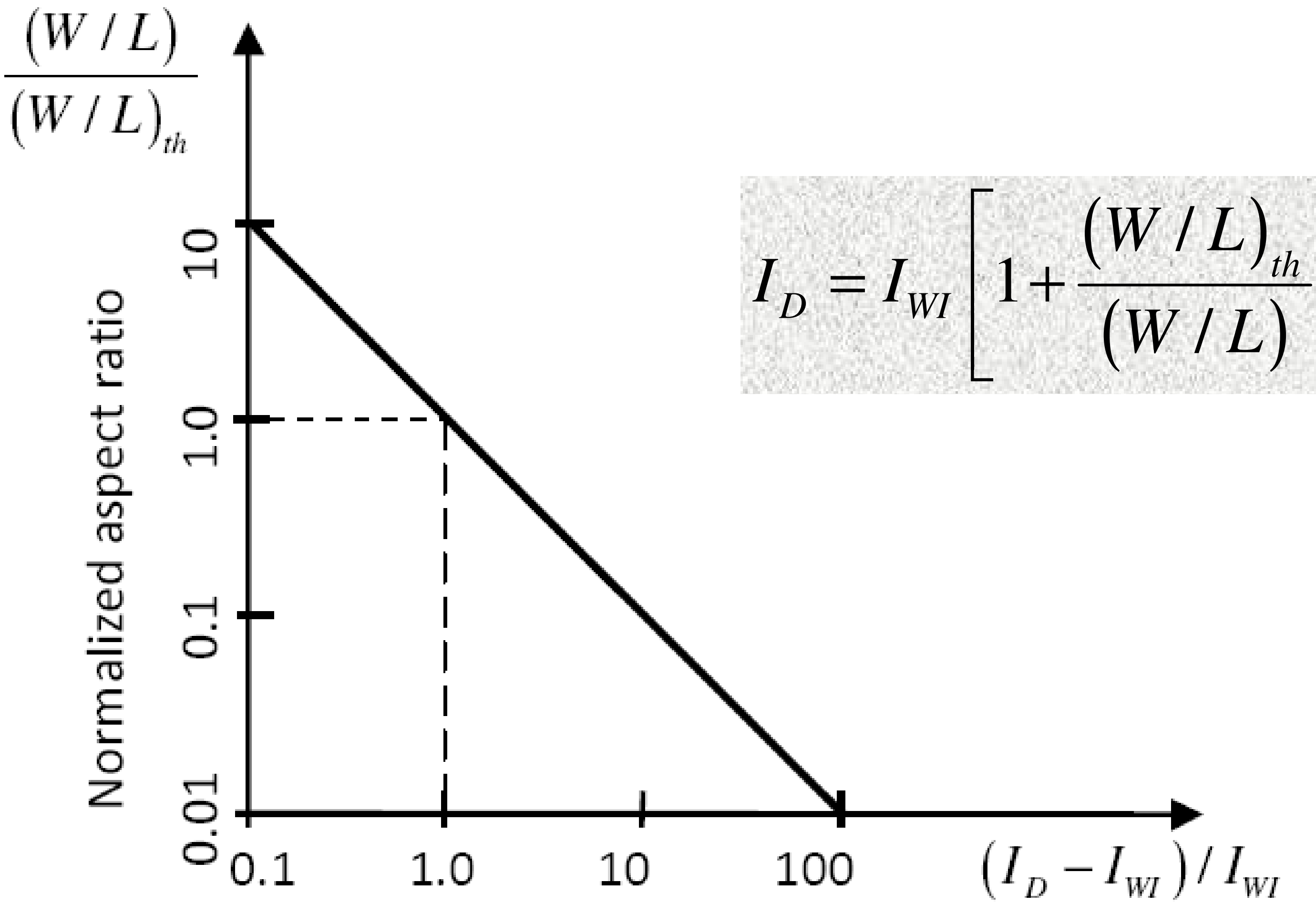
$$I_{WI} = n g_m \phi_t = 1.35 \cdot 628 \cdot 10^{-6} . 26 \cdot 10^{-3} = 22\ \mu A$$

$$I_D = I_{WI} + I_{Dsi} = n g_m \phi_t \left[1 + \frac{g_m}{2 \mu C'_{ox} \phi_t \left(W / L \right)} \right]$$

$$I_D = I_{WI} \left[1 + \frac{\left(W / L \right)_{th}}{\left(W / L \right)} \right]$$

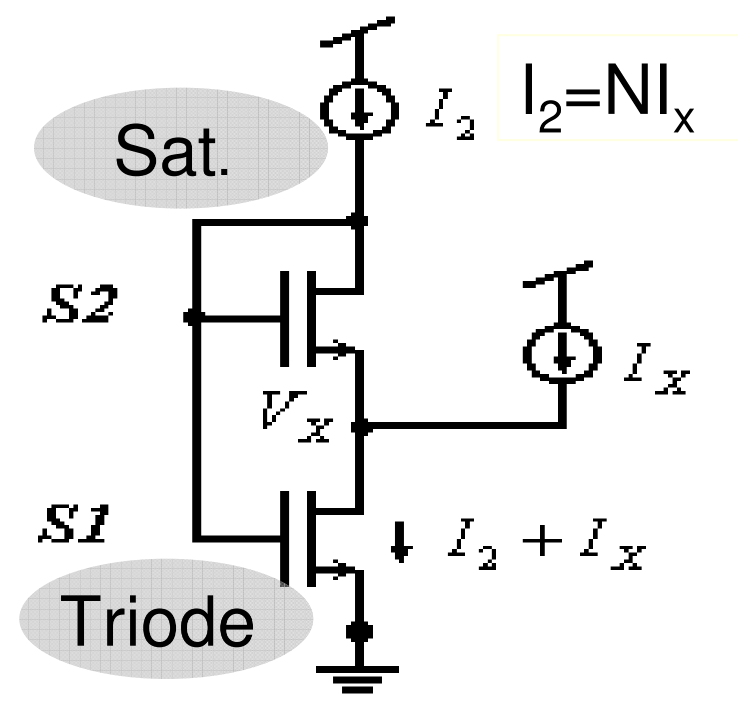
$$g_m = \left(W / L \right)_{th} \mu \left(2 C'_{ox} \phi_t \right)$$

ASPECT RATIO VS. CURRENT EXCESS



$$I_D = I_{WI}\left[1 + \frac{(W/L)_{th}}{(W/L)}\right]$$

SELF-CASCODE MOSFET (SCM)



$$I_{S2}i_{f2} = NI_x$$

$$I_{S1}(i_{f1}-i_{f2}) = (N+1)I_x$$

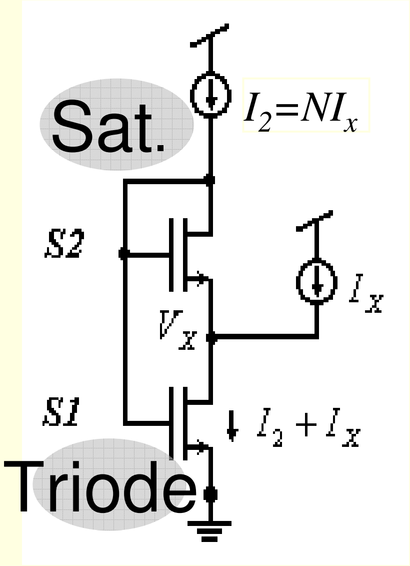
$$\Downarrow$$

$$i_{f1} = \left[1+\frac{S_2}{S_1}\left(1+\frac{1}{N}\right)\right]i_{f2} = \alpha i_{f2}$$

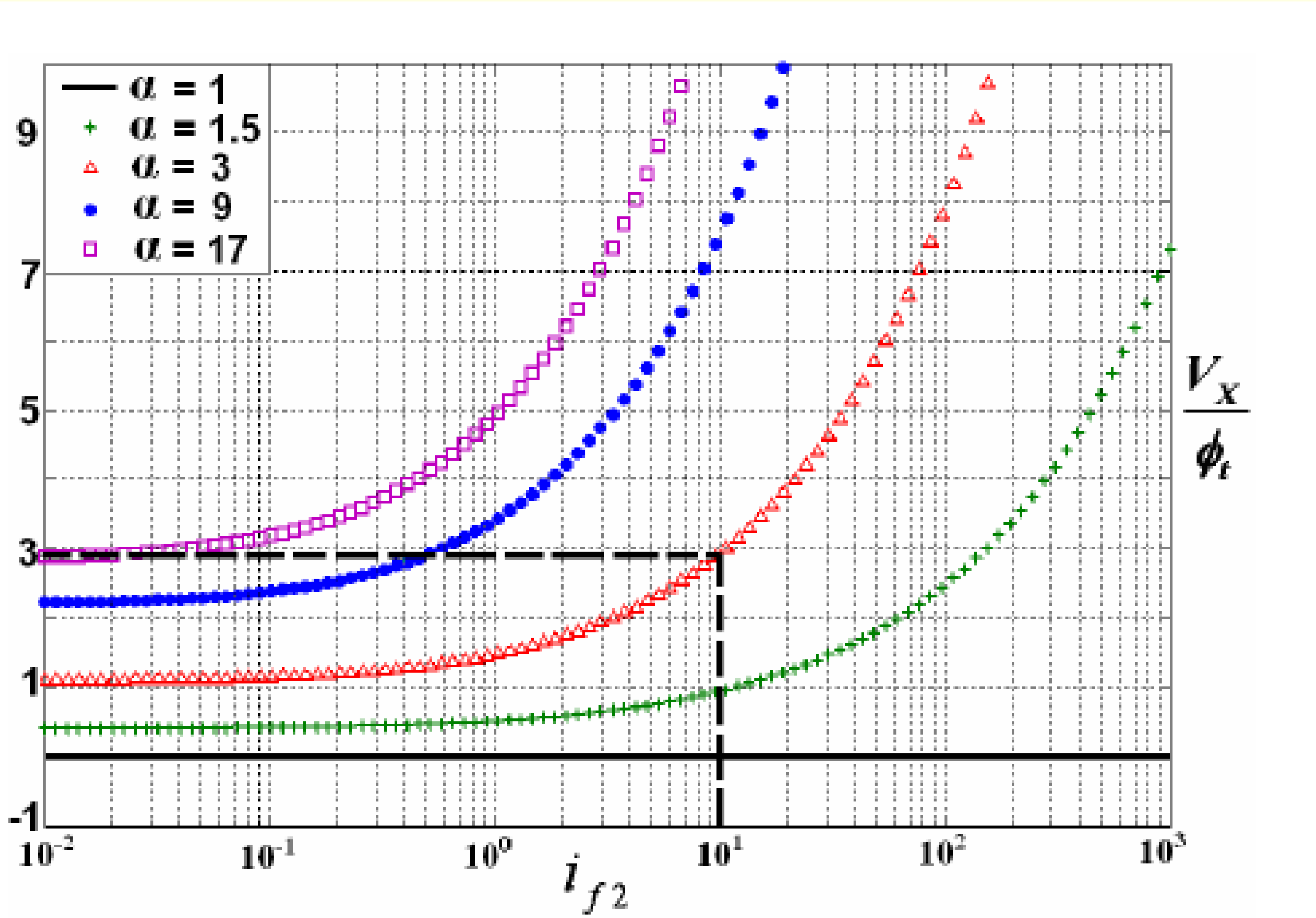
Applying UICM to both M1 & M2

$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right)$$

V-I CHARACTERISTICS OF SCM



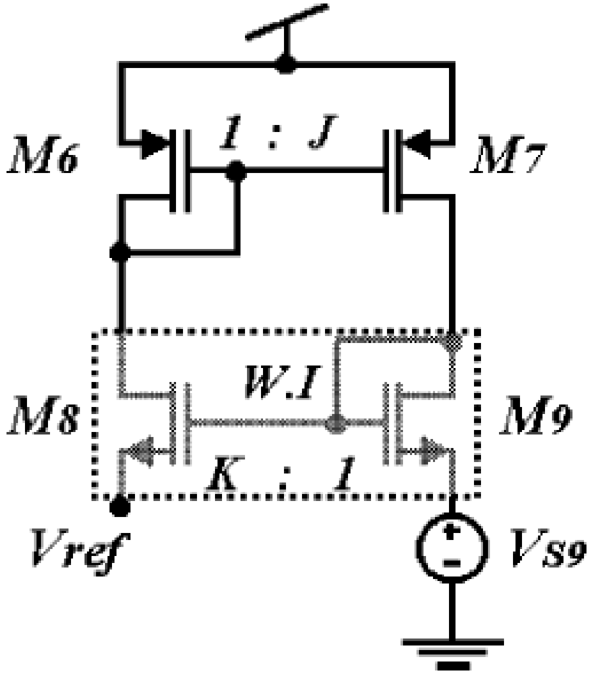
$$\alpha = 1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)$$



$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right)$$

In WI: $V_X = \phi_t \ln \alpha$

VOLTAGE FOLLOWING (NMOS) CURRENT MIRROR (PMOS)[1]

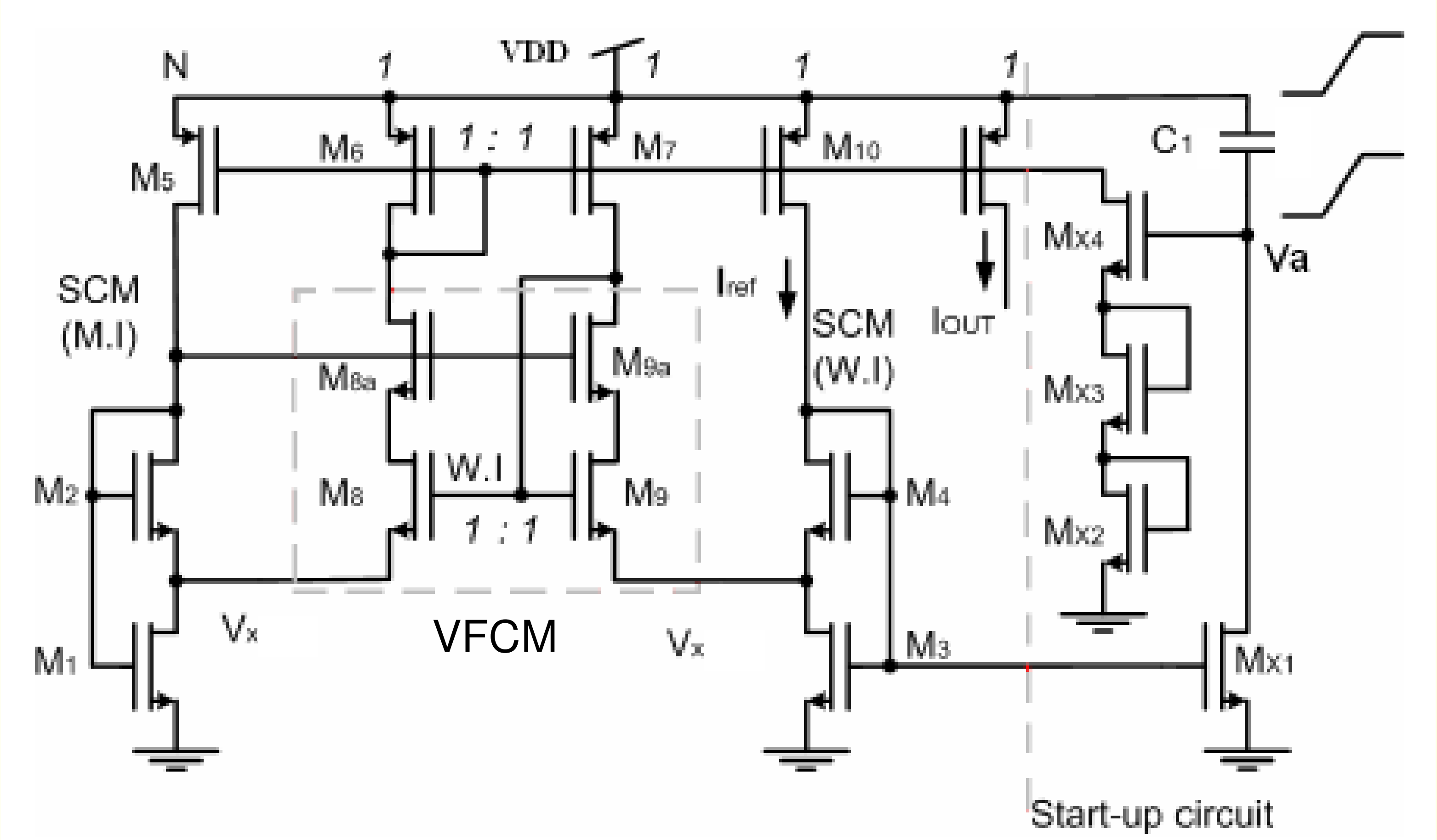


In WI: $V_{ref} = V_{S9} + \phi_t \ln(JK)$

---

[1] B. Gilbert, AICSP vol. 38, pp. 83-101, Feb. 2004

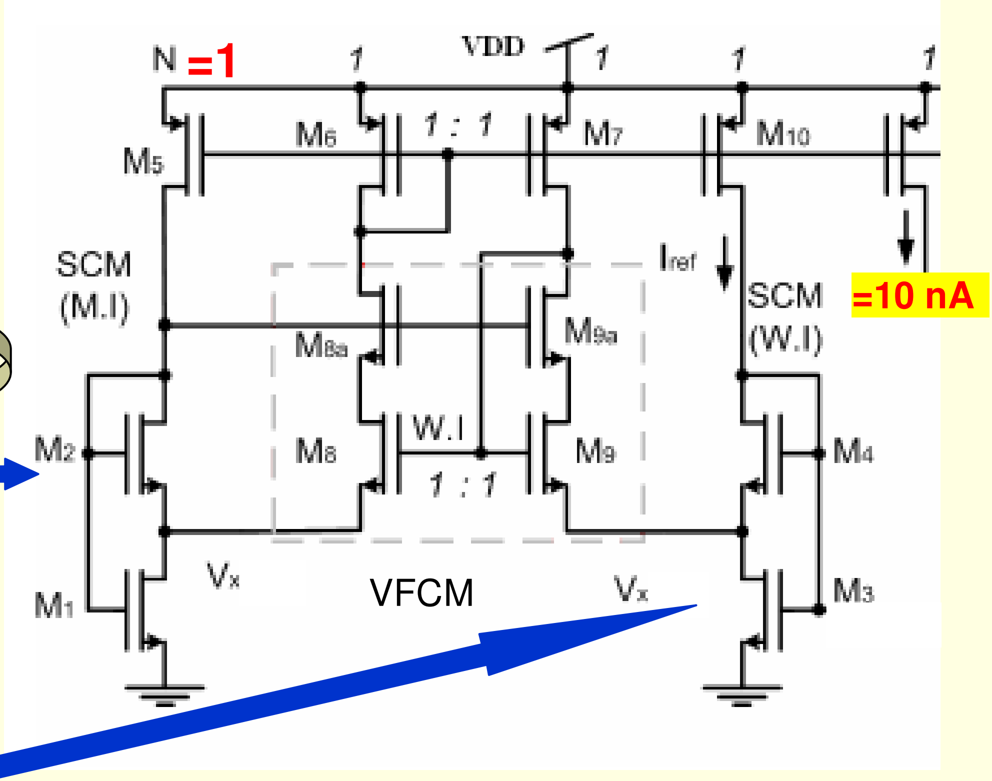
SELF-BIASED CURRENT SOURCE (SBCS)



DESIGN OF A SBCS

Output current: I_{ref}=10 nA

$I_{SH\text{n-channel}} \cong 100$ nA, $I_{SH\text{p-channel}} \cong 40$ nA



$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1}\right)$$

Let us choose

M_1 &M_2 in MI: i_{f2} = 10 S_2= S_1, N = 1

$$\alpha = 1+\frac{S_2}{S_1}\left(1+\frac{1}{N}\right) = 1+1+1 = 3$$

$$\frac{V_X}{\phi_t} = \sqrt{1+30}-\sqrt{1+10}+\ln\left(\frac{\sqrt{1+30}-1}{\sqrt{1+10}-1}\right) = 2.93$$

M_3 &M_4 in WI: $i_{f3(4)}$ <<1

$$\frac{V_X}{\phi_t} \cong \ln\alpha \Rightarrow \quad \alpha = e^{2.93} \cong 18.7$$

$$18.7 = 1+\frac{S_4}{S_3}\left(1+\frac{1}{1}\right) \Rightarrow \frac{S_4}{S_3} = 8.85$$

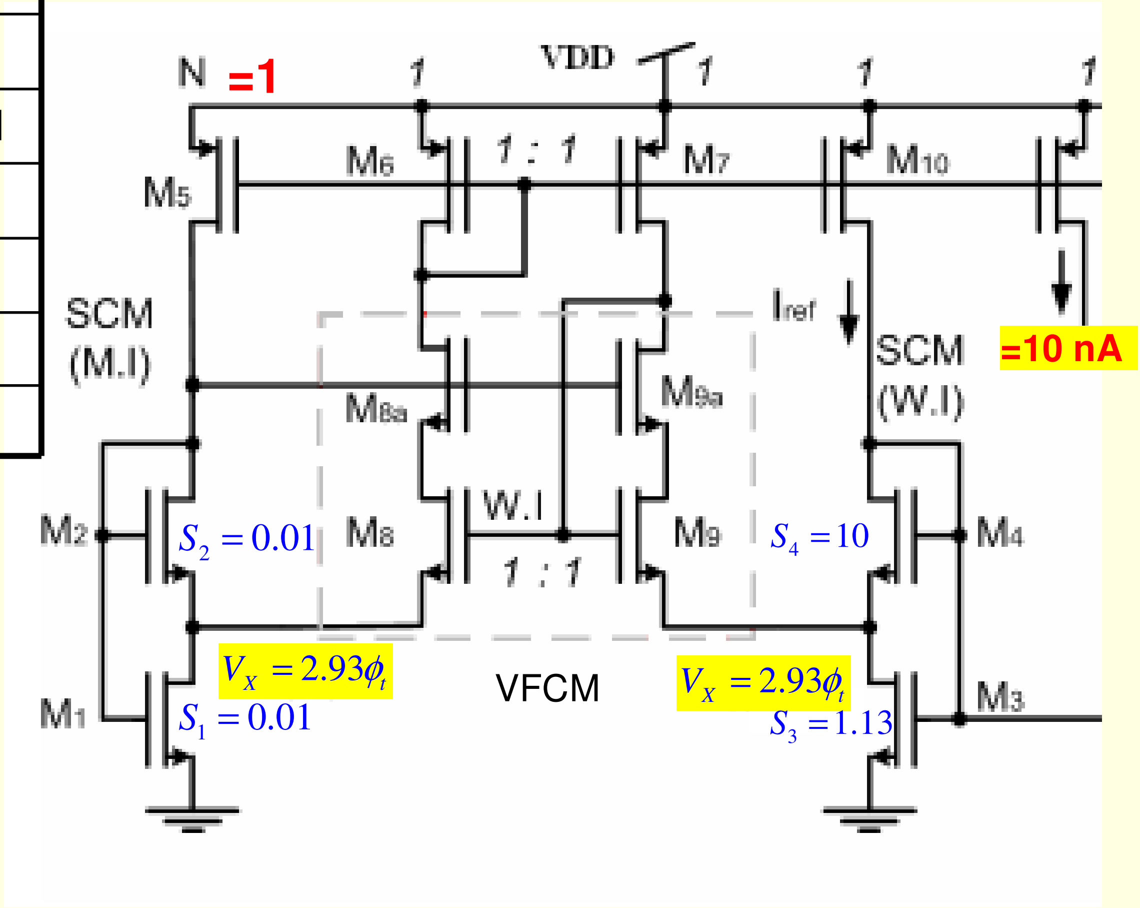
$$I_{S2}i_{f2} = 10 \text{ nA} \rightarrow I_{S2} = 1 \text{ nA} \rightarrow S_2 = S_1 = 0.01$$

Let us choose i_{f3}=0.187 → $i_{f4} = i_{f3}/\left[1+2S_4/S_3\right] = 0.01$ ⇒ $I_{S4}i_{f4} = 10 \text{ nA} \rightarrow I_{S4} = 1\ \mu\text{A} \rightarrow S_4 = 10$

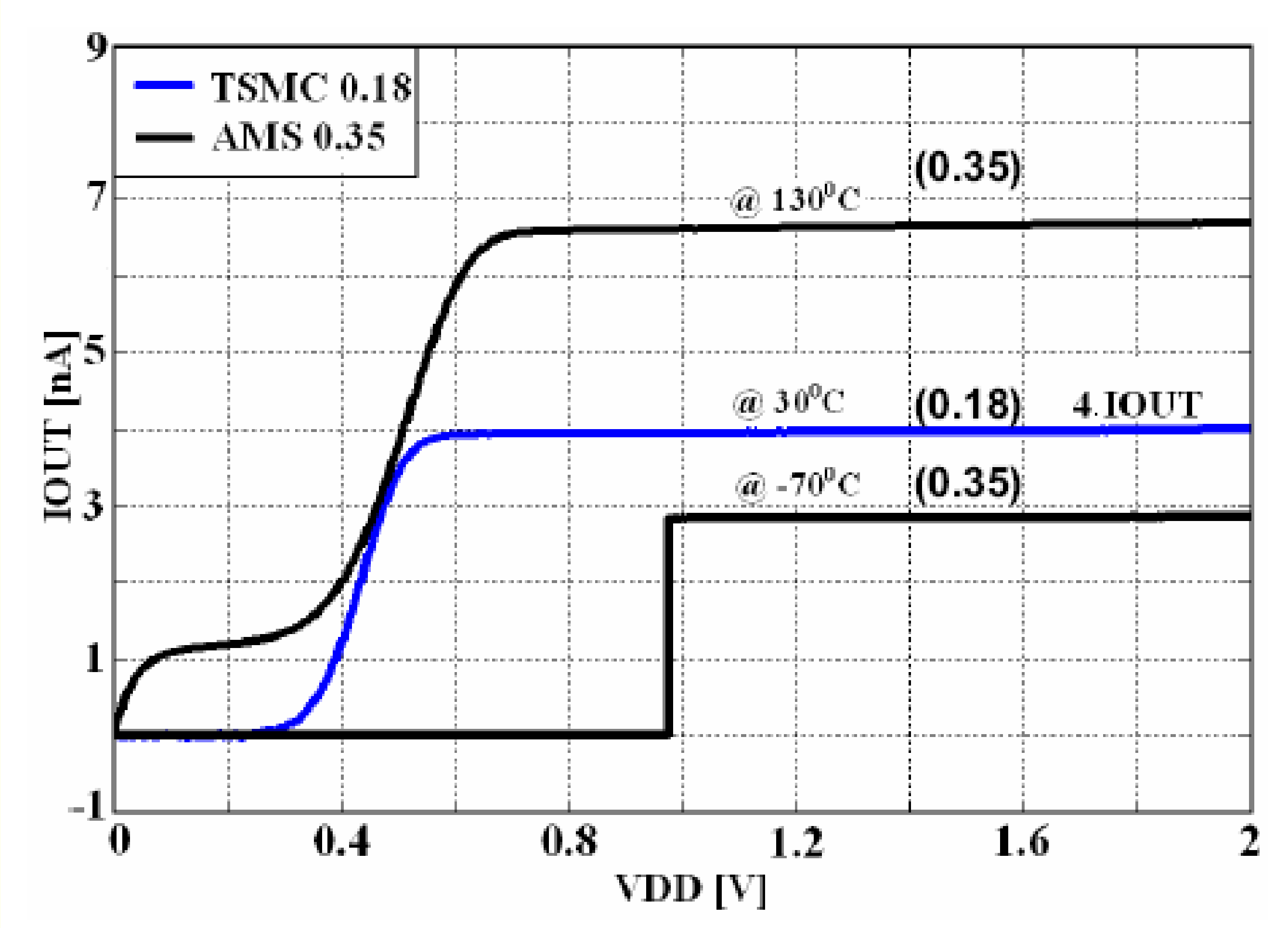
$$S_3 = \frac{S_4}{8.85} = 1.13$$

DESIGN OF A SBCS - Summary

	S	i_f	i_r
M_1	0.01	30	10
M_2	0.01	10	0
M_3	1.13	0.187	0.01
M_4	10	0.01	0
M_8, $M_{8(a)}$	1	0. 1	0
M_9, $M_{9(a)}$	1	0. 1	0
M_P (all)	2.5	0.1	0

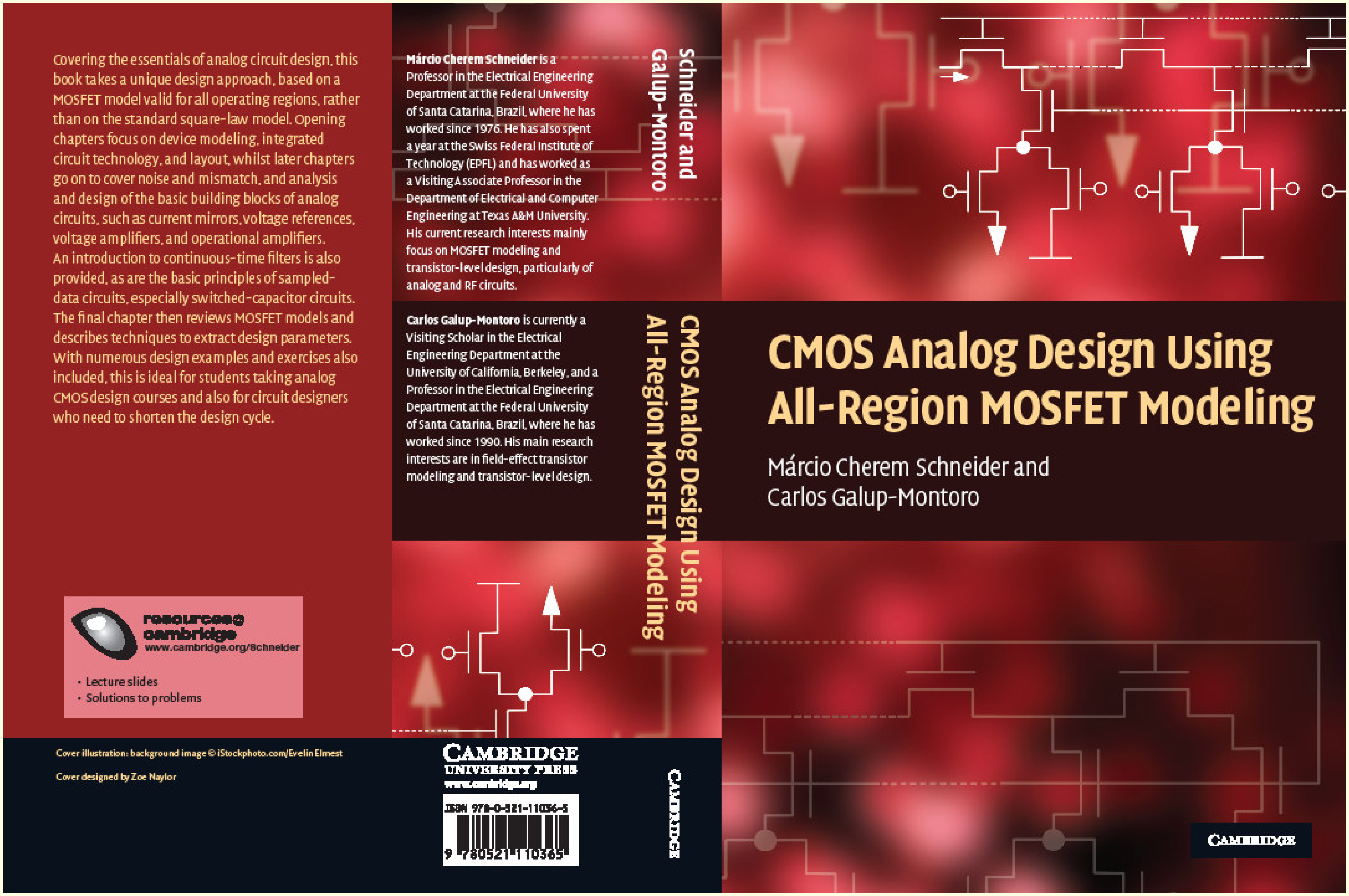


SBCS: I_{OUT} vs. V_{DD} AT CONSTANT TEMPERATURE[1]



[1] E. M. Camacho-Galeano *et al*. pp 2230-2233, ISCAS 2008

REFERENCE



Covering the essentials of analog circuit design, this book takes a unique design approach, based on a MOSFET model valid for all operating regions, rather than on the standard square-law model. Opening chapters focus on device modeling, integrated circuit technology, and layout, whilst later chapters go on to cover noise and mismatch, and analysis and design of the basic building blocks of analog circuits, such as current mirrors, voltage references, voltage amplifiers, and operational amplifiers. An introduction to continuous-time filters is also provided, as are the basic principles of sampled-data circuits, especially switched-capacitor circuits. The final chapter then reviews MOSFET models and describes techniques to extract design parameters. With numerous design examples and exercises also included, this is ideal for students taking analog CMOS design courses and also for circuit designers who need to shorten the design cycle.

resources@
cambridge
www.cambridge.org/Schneider

- Lecture slides
- Solutions to problems

Cover illustration: background image © iStockphoto.com/Evelin Elmest

Cover designed by Zoe Naylor

Márcio Cherem Schneider is a Professor in the Electrical Engineering Department at the Federal University of Santa Catarina, Brazil, where he has worked since 1976. He has also spent a year at the Swiss Federal Institute of Technology (EPFL) and has worked as a Visiting Associate Professor in the Department of Electrical and Computer Engineering at Texas A&M University. His current research interests mainly focus on MOSFET modeling and transistor-level design, particularly of analog and RF circuits.

Carlos Galup-Montoro is currently a Visiting Scholar in the Electrical Engineering Department at the University of California, Berkeley, and a Professor in the Electrical Engineering Department at the Federal University of Santa Catarina, Brazil, where he has worked since 1990. His main research interests are in field-effect transistor modeling and transistor-level design.

CAMBRIDGE
UNIVERSITY PRESS
www.cambridge.org

ISBN 978-0-521-11036-5

Schneider and
Galup-Montoro

CMOS Analog Design Using
All-Region MOSFET Modeling

CAMBRIDGE

CMOS Analog Design Using All-Region MOSFET Modeling

Márcio Cherem Schneider and
Carlos Galup-Montoro

CAMBRIDGE