Empirical Nonlinear IV and Capacitance LS Models and Model Implementation:

Nonlinear IV Models,
Capacitance Models, Charge Conservation,
LS Model Implementation,
FET examples: High Power, Linear,
GaN,SiC,GaAs,CMOS
Summary.

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1Physical Models- important in the device design stage.

2Table Based Models- very accurate in the measurement range!

Typ. 1000 measurement points! We have X-parameters- now!

Problems: 1Outside Measurement Range? Data set is large>20 mB->slow.
2Change of working conditions? Temp, Rtherm,Ctherm etc. ?
3Manufacturing tolerances? Vpof, Gm, etc.
4Scaling High Power Devices-> it is easier to measure smaller device and scale.
5Feedback for the device quality, EC. parameters etc.- important for foundries!

3Empirical Equivalent Circuit Models. 100-200 measurements points

1Accurate enough for many applications-1-5%.
Comparably easy to understand and extract, compact form- parameter list.
2Extendable out of the Measurement Range> from 65GHz measurements designs for 220GHz [Ref:46-48].
3Possibility to tune& change,scale the model, production tolerances, Rtherm...
4Provide feedback for device parameters change, quality of processing ..

All model types have their place and we should use the right type for the specific application. We can mix& integrate different type models- ETB.

Transistor modelling sequence:

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1Measurements

1.1 Transistor functionality.

1.2 Select Representative Device!!! Statistical data!

1.3.1 Measurements, Multi-bias:

a)DC-Ids vs. Vds , Vgs parameter

b)DC-Ids vs. Vgs, Vds parameter

1.3.2- Multi-bias S-parameters- the same bias points used in DC measurements

1.3.3-Power Spectrum (PS)- i.e. fixed RF, Vds, Pin, sweeping Vgs

2. SS model extraction

4.Model function selection

5.Model implementation

6.Model evaluation- a)Multi-bias DC and S-parameters.

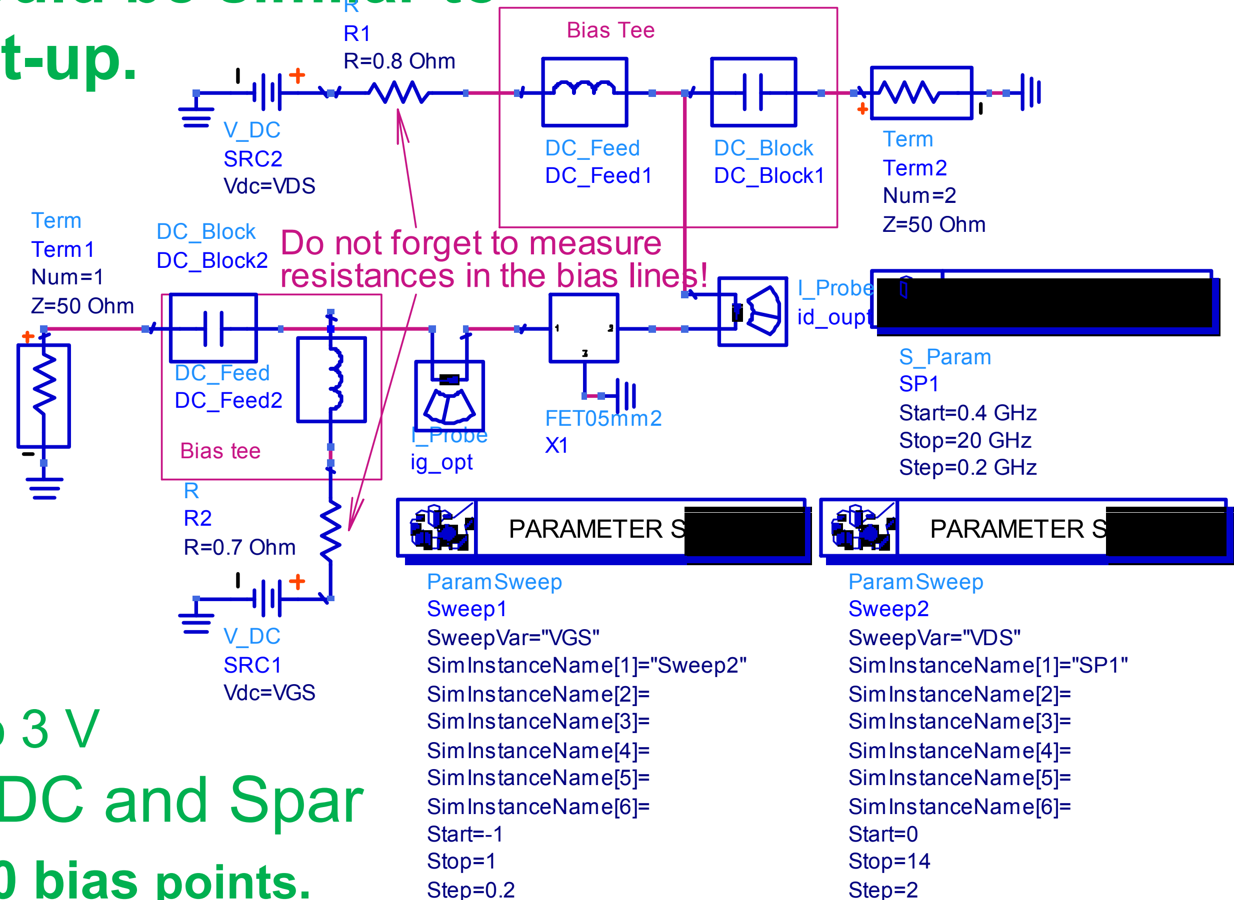
b).Large Signal evaluation- Power Spectrum (PS), Load-pull

c)Waveform, Combined Load-pull &Waveform.

Measurement setup DC and S-par.

Simulation setup should be similar to the measurement set-up.

Common mistake- people forget to measure resistances in bias lines.



1SS&Noise model>

3-4 practical bias points:

Ids=5,10,15 mA , Vds =1 to 3 V

2LS model :Multibias DC and Spar

$10V_{gs}$&$10V_{ds,}$ **Typ. 100-200 bias points.**

1 Transistor functionality evaluation: Rds(Ron)=Rd+Rs+Rch.

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Meas. 1 Ids vs. Vgs for low Vds;

Nonlinear Models are controlled by intrinsic voltages,

so we need Rs,Rd to account for the voltage drop.

Measurement Ids in the linear part of the IV sweeping Vgs, at fixed low Vds.

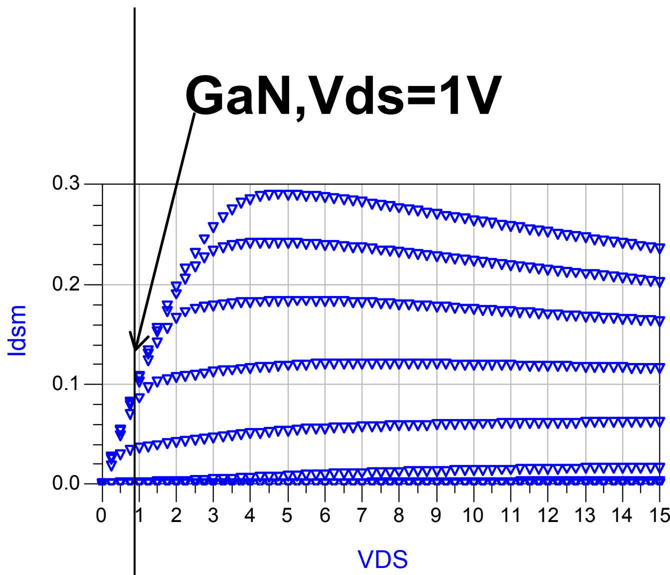
->safe measurement, GaAs Vds=0.1v, GaN Vds=1v.

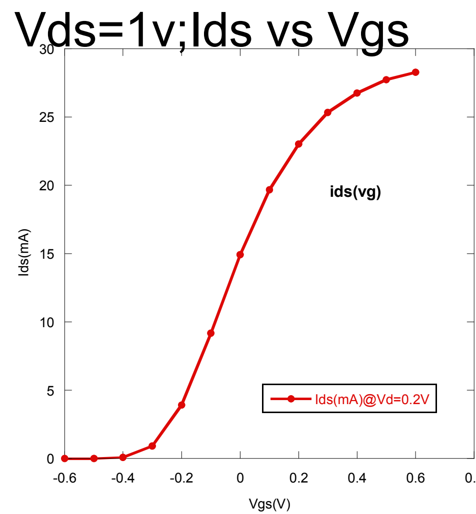
Rds=Vds/Ids: For gate in the middle S-D we can consider:

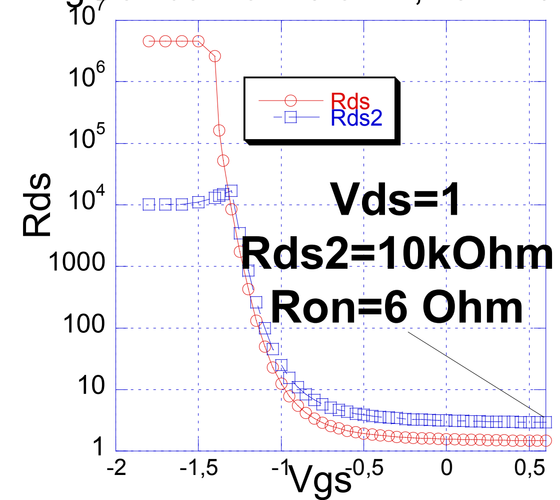
Rs=Rd=Rch=Rds/3 For MSEFET:More accurately-Rs,Rd,by fly-back method

Good device:Ron=3 oHm,Roff>3MOhm

Working device:Ron=6 oHm;Roff=10 kOhm







2Measurements Ids vs. Vds, Vgs param.

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Low Power device
Pdc<100 mW:
Pdc>100mW- self-heating
should be accounted

- α_r: slope at Small currents, Low Vds
- α_s: slope High currents ,Low Vds   λ: slope at high Vds & small currents.
- **I.e. we need 3 parameters to model the slope Ids vs. Vds(min.)**

2b Measurements Ids vs. Vds, Vgs param

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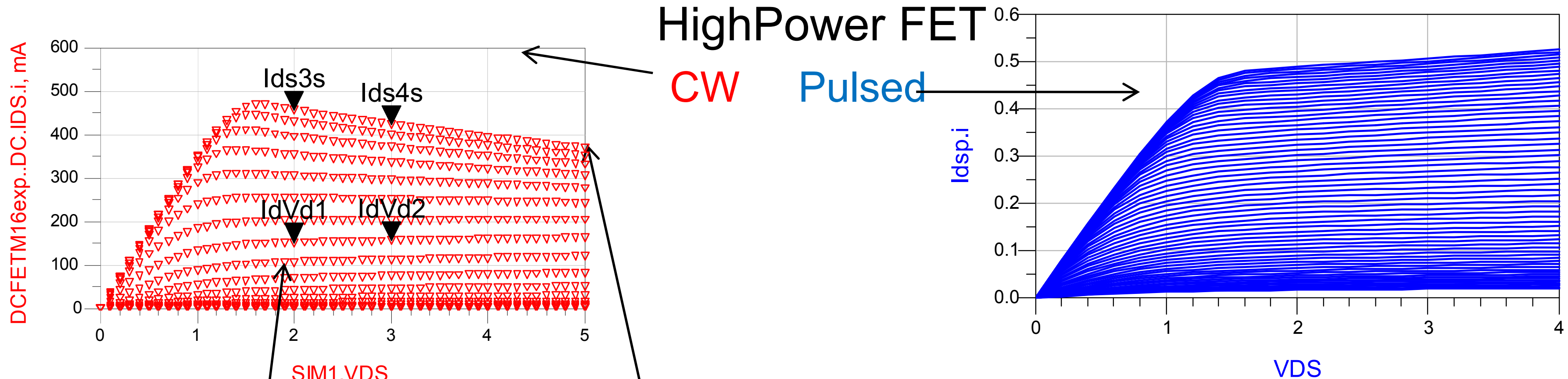

IdVd1
SIM1.VDS=2.000
DCFETM16exp..DC.IDS.i=0.151
SIM1.VGS=-1.250000

Ids3s
SIM1.VDS=2.000
DCFETM16exp..DC.IDS.i=0.456
SIM1.VGS=0.500000

IdVd2
SIM1.VDS=3.000
DCFETM16exp..DC.IDS.i=0.155
SIM1.VGS=-1.250000

Ids4s
SIM1.VDS=3.000
DCFETM16exp..DC.IDS.i=0.423
SIM1.VGS=0.500000

IdsVd2=IdsVd1(1+lambda1) lambda1=0.027; lambdaSelfHeat=-0.083;
Ids4=Ids3s(1+lambda1)*(1+lambdaSelfHeat)

Slope=DI/(I*DV)

Slope at low power is positive =+0.027

Slope at high power is negative=-0.083

The **negative** slope at high dissipated power is due **to selfheating!**
This effect should be modeled with a thermal network!
Pulsed IV measurements, when available. Pulse <100-200 nS, to avoid selfheating.Then, you might face, ringing, dispersion manifestation etc.

Self-Heating: Models without Self-Heating> not suitable for Pdc>0.3W

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Self-heating effects :

1 Change of mobility: Reduced mobility at higher temperature ->smaller Gm :
P1T =*gm/Ipk;* P1T=P1(1+TcP1*ΔTj) Linear function + -100C (TcP1**=-0.003)-negative**

2 Change of carrier concentration: Ipk0T=Ipk0(1+TcIpk0*ΔTj) (TcIpk0**=-0.003) negative**

3 Device speed: mobility change will influence capacitances :
Cgs0T=Cgs0(1+TcCgs0*ΔTj); Cgd0T=Cgd0(1+TcCgd0*DTj) (TcCgs0**=+0.003)**

4 RF and dispersion characteristics: influenced by traps (at higher temperature things worsen)
Rc=f(T) (TcRc=-0.002); Crf =f(T) (TcCrf=+0.002) ~

For all FET, important temperature coefficients are similar:

TcIpk0**=-0.0025 to -0.0035;& negative:**

TcP1 **=-0.0020 to -0.0035;& negative:**

TcCgs0**=0.002 to 0.0035;&positive**

$$TcIpk0 \simeq -0.003$$

$$TcP1 \simeq -0.003$$

The Self-heating effect is a proportional to TcIpk0*Rtherm.

Error in TcIpk0,TcP1 can be compensated with Rtherm.

Self-Heating: Models without Self-Heating not suitable for Pdc>0.3W.

Be careful if Rtherm is not listed in model parameters

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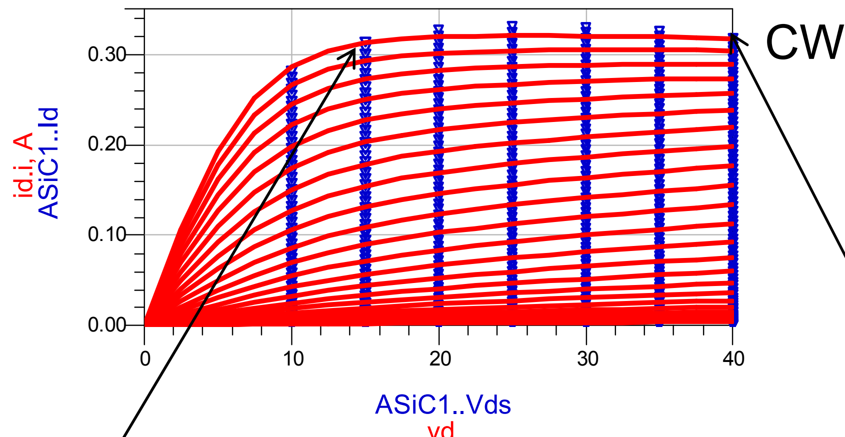
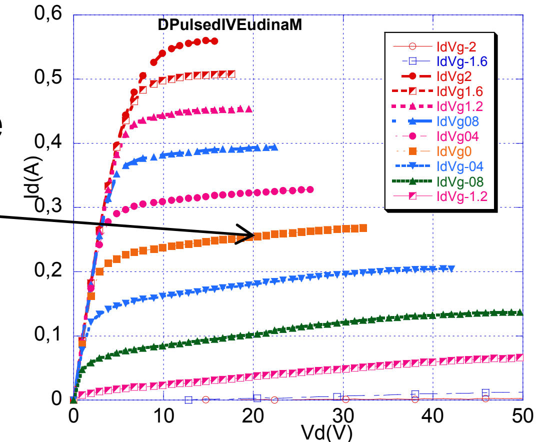


CW

Pulsed:
The slope is positive even at high Pdc!



Self-heating is usually modelled with a **single thermo-electrical circuit Rtherm*Ctherm.** With temperature coefficients TcIpk,TcP1 known, there is **only one thermal** parameter to find > **Rtherm. This is done in the CAD,** at high Pdc:

1Fit accurately Ids at the knee(current parameters), 2Adjust Rtherm to fit the slope Ids vs. Vds.

Accurately, thermal resistance can be found **measuring junction temperature Tj** with infrared microscope. Tj=**Rtherm.**Pd+Tamb

The thermal capacitance Ctherm model the thermal storage capacity of the structure. We can have different Rtherm and Ctherm for the chip Rthermchip, Cthermchip and for package Rthermpackage ,Cthermpackage for high power devices.

Rtherm is not constant with temperature. For **high** dissipated power>10W should be considered: **Rtherm(T)=Rtherm(1+TcRtherm*DTj).**

3Measurements Ids vs. Vgs

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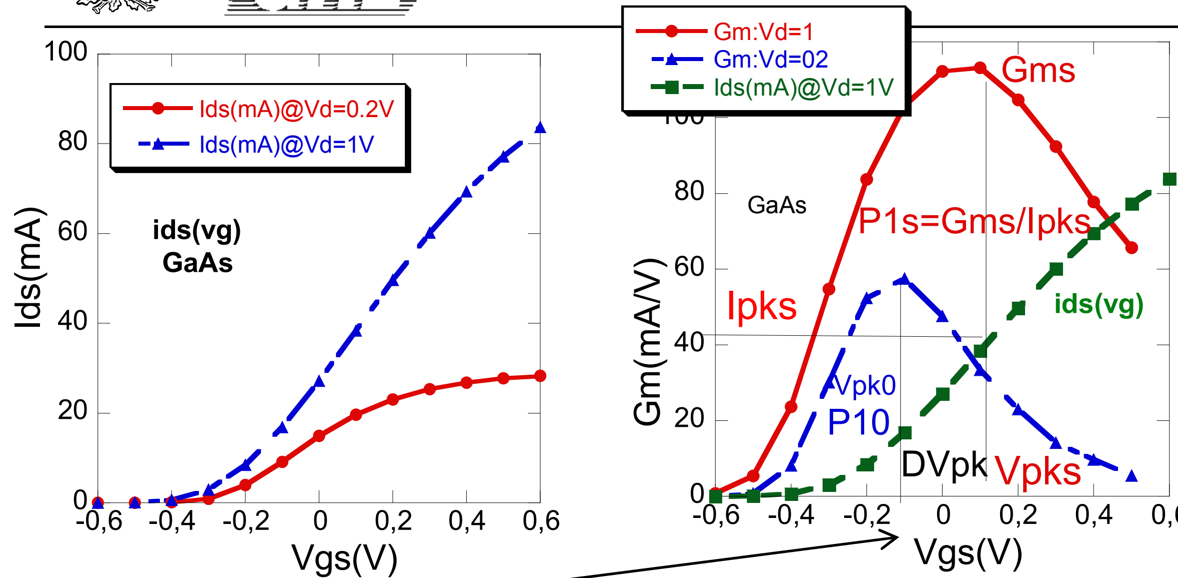


Meas 3. IV - Ids=f(Vgs, Vds)

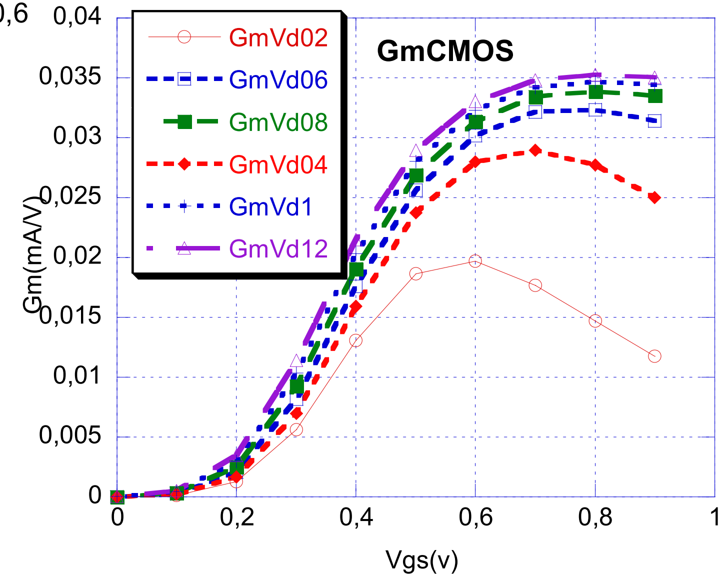
1Vds>Vknee at Vpks &and corresponding Ipks, Gmmax ;**P1s= Gms/Ipks**

2P10=Gm/Ipk0 at low Vds is larger P1s=Gms/Ipks

Part of ΔVpk is due to voltage drop on Rs * Ids

ΔVpki~0.2V (GaAs,CMOS) ΔVpk~0.2-0.6V (GaN)

Gm shape for MESFET&CMOS are similar



Variety of cases: Gm shape and P1s= Gms/Ipks
Models should be able to handle this.

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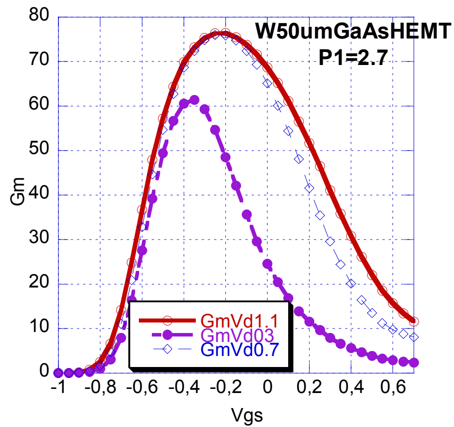
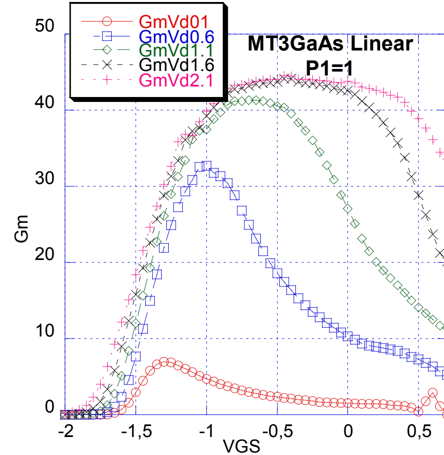
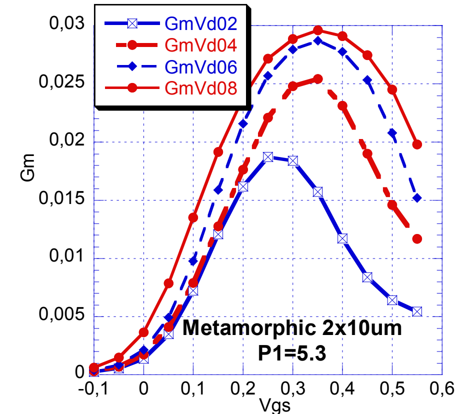
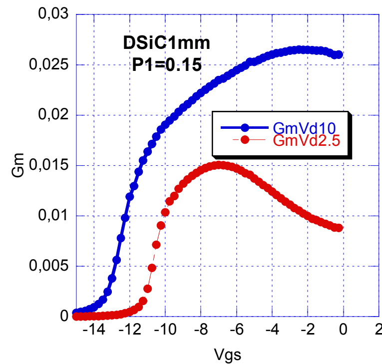
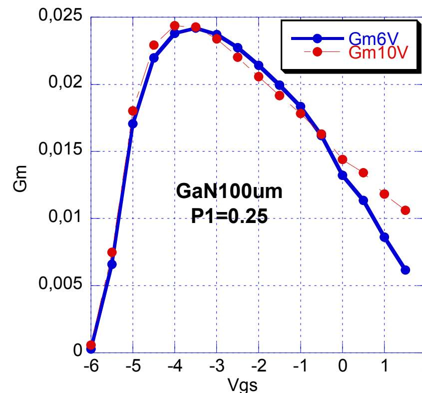


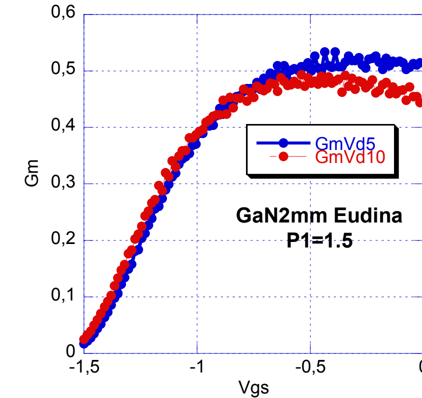




P1s=2.7 (HEMT) **P1s=1.1 (Linear HEMT)** **P1s=5.3 (High Gain HEMT)**







P1s=0.15;SiC **P1s=0.25;GaN** **P1s=1.4;GaN Eudina**

Variety of cases: **Gm shape and P1s= Gms/Ipks**

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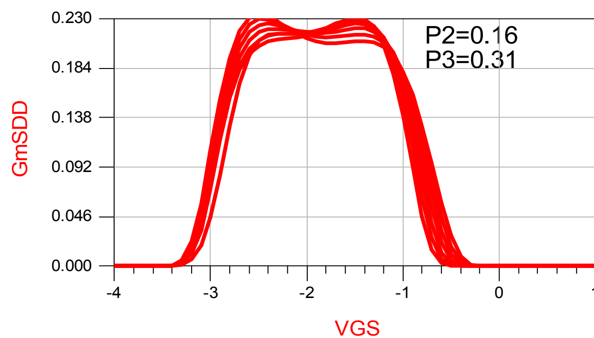
It is important to find the reason for the specific effect, dependence etc. to model and implement this properly.

Example 1;Gm shape- doping profile (Ids dependence vs. Vgs)-Ids=f(Ψ(Vgs)),P2,P3

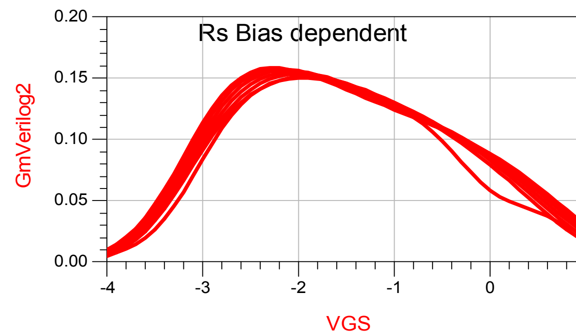
Example 2; GaN FET -Rs is bias dependent, velocity saturation.Rs=f(Ids)

Example 3 ;Rs,Rd temperature dependent-self-heating. Rs=f(T)

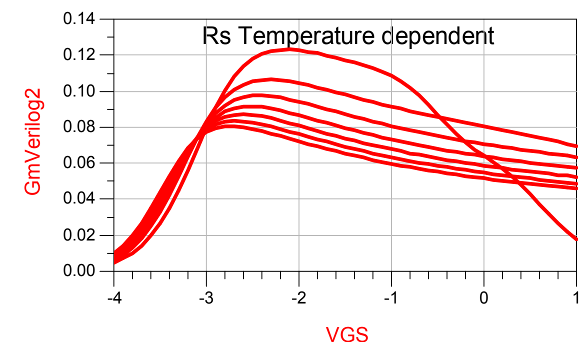
Usually we have several effects on the top of each other. I.e. we need to do several, properly designed measurements to distinguish between effects, like specific Ids measurements, Measurements at 3 equally spaced temperatures, pulsed IV, LSVNA etc...



Example 1:Parameters of the F=f(Ψ(Vgs)) function changed



Example 2: Rs Bias dependent



Example 3:Rs,Rd temperature dependent

High Power devices

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Important for Large&High Power devices:

1.**The Gate Control is delayed and reduced at high frequency**:
Large&High Power Devices do not respond immediately at RF!
Cdel =2-3fF- is the capacitance of the gate footprint, Rdel=2kOhm(chan. resistance)

2 Current slump -In some cases at RF we do not reach the DC Ids values.

3. (Back-gate) voltage will change the effective Vgs at RF ->dispersion

4. **Higher Rs and Rd/ mm** for SiC and GaN FET in comparison with GaAs FET

5. Rd, Rs bias and temperature dependent! (A.Inoe *et al.,* IMS2006 WE2F2, M. Thorsel)

6. **Self-heating model-must!** Mounting quality is critical.

7. Breakdown important for high power devices!

8 Keep device safe<Pmax!

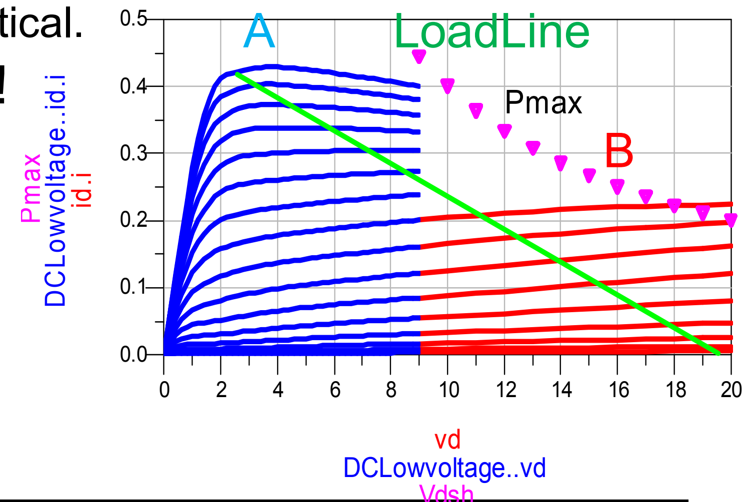
Organize measurements properly.

Dual region measurements& simulations:

A)High Ids, Low Vds;

B)Low Ids, High Vds

Cover the load line!



High Power FET EC

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Lg Rg Rgd Cgd Rd Ld

Gate Drain

Igd

Ri Cdel

Ids Crf

Rtherm

Igs Vgsc

Vbgate

Ctherm Rdel R1 R2

Cds Rc

Thermal subciruit.

Cgs Cdel

External

Rs2

Source

Ls Rs Crs

Simplified Dispersion Model:Crf,Rc

SiC FET

Parasitic elements :Rg,Rgd,Rd,Rs,Ri, Cds,Lg,Ld,Ls, layout elements etc.

New: Cdel, Rdel shunting the gate control node Vgsc> Frequency dependent gate control and delay.

b) Frequency dependent Rs for SiC

Nonlinear: Ids, Igs, Igd,Cgs,Cgd-> we need models.

Models are controlled by intrinsic voltages!

GS,GD Breakdown Measurements

We can use resistors to limit& define safe currents levels.

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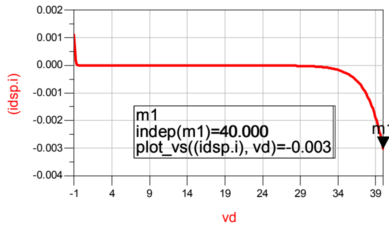
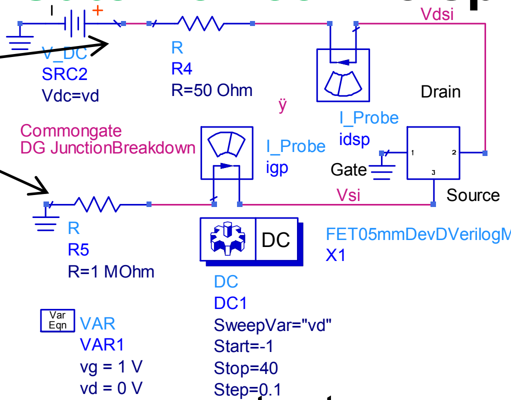
Common Gate Device: we split the GS, GD Junctions:

GD

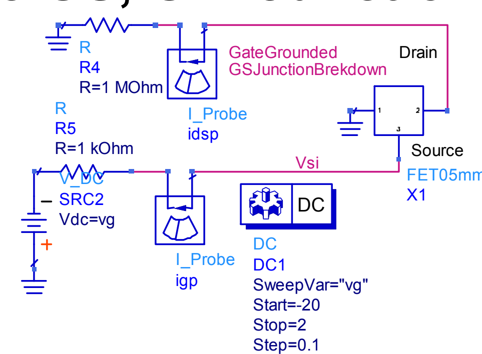
Rmeas=50 ohm

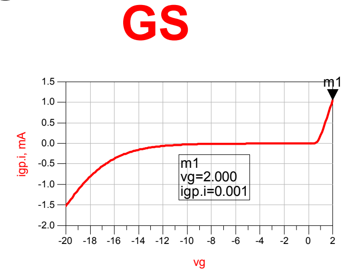
Rcoupl= 1 MOhm





GS

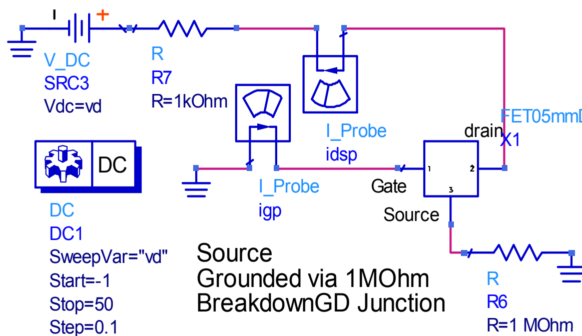


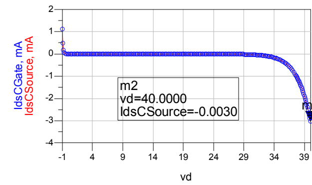


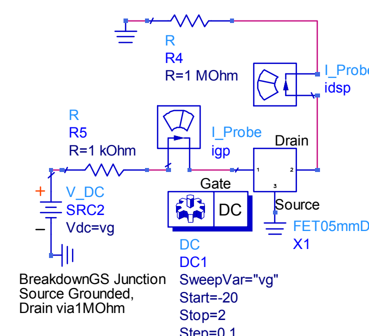
Gate -Drain breakdown measurement setup ; **Gate -Source** breakdown measurement setup.

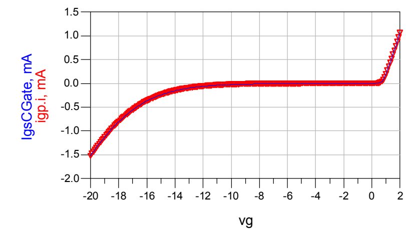
We can use resistors to limit& define safe currents levels. Compliance is not fast enough and difficult to model.

Common Source Device, Source without via, using needles:









Gate -Drain breakdown measurement setup. **Gate-Source** breakdown measurement setup.

Ids, Igs &Cap. Model Function Selection

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1**Physical !!!**

2.Single definition -∞+ ∞; Infinite & correct derivatives.

3.The model parameters should be responsible for specific things: Current, Voltage, Cap, Slope, etc.

4. Flags, conditions should be avoided!

5. Directly extractable! Available in CAD tools!

6. If possible, use inflection points to construct the model. This simplifies the extraction, improves accuracy and reduce model parameters.

7.The best solution is to split (if possible) the model Function on independent parts: F= f1[Ψ1(Vgs)]*f2[Ψ2.Vds]

8.If the guess for modeling function F is good, extracted argument will be linear function: Ψ =P1*Vgs; P1=derivative of F=f(Ψ(Vgs))

2 Ids Model Function Selection

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FET Ids- solution of Schrodinger equation:

Error type functions → $$\frac{d}{dx}\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} e^{-x^2}.$$

Typical for FET: f1(Vgs)=1+erf(Vgs)

The error function is not always available in CAD tools **and**

simple& direct reverse extraction is not possible.

Replacement for error functions:

a) GaAs: f1a(Vgs)=1+**Tanh**[P1.Vgs]

extraction :Ψ1a(Vgs)=**ArcTanh**[(Ids/Ipk0)-1]

b) GaN and SiC: f1b(Vgs)=1+**Tanh**[**Sinh**(P1.Vgs)]

extraction: Ψ1b(Vgs)=**ArcSinh** [**ArcTanh**[(Ids/Ipk0)-1]]

c)We need to fit different profiles i.e. Adjustment possibilities!

d) try to use inflection points- this will make model compact and accurate at critical points.

3 Ids Model Function Selection FET
Ψ Examples:extracted GaN, SiC FET

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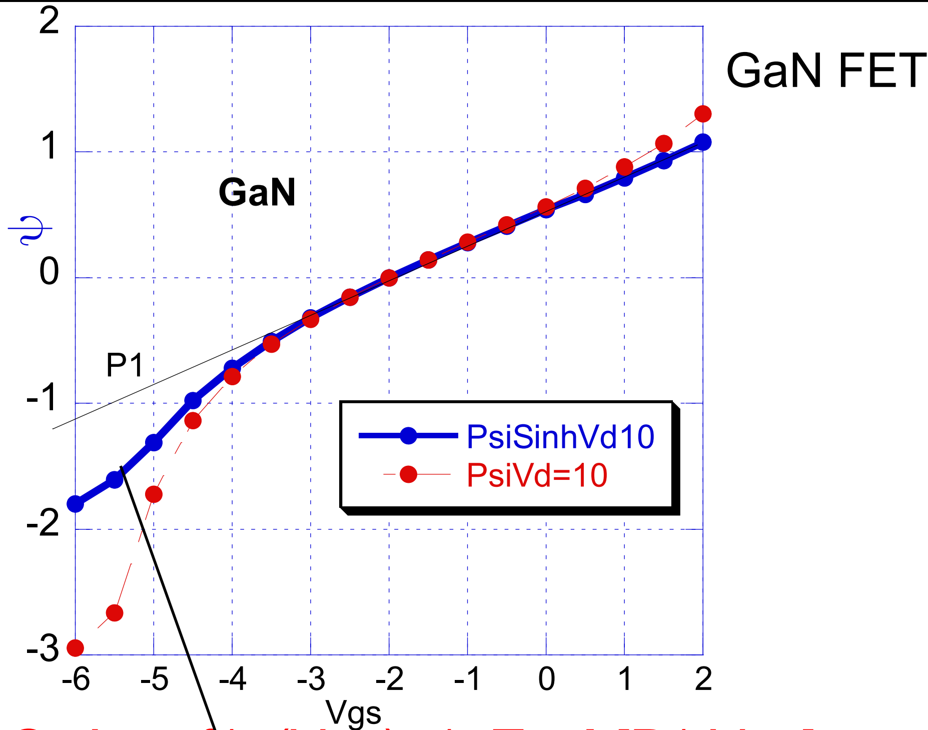

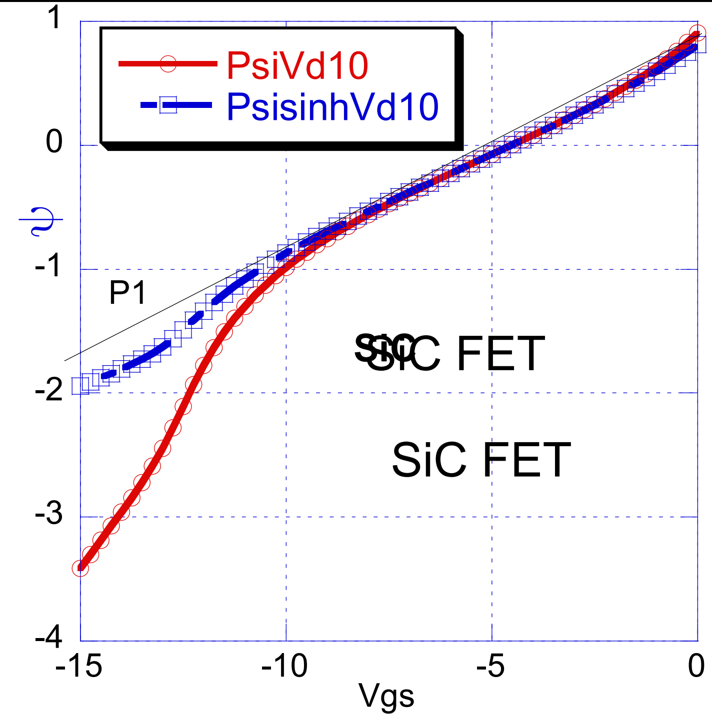

a) GaAs: f1a(Vgs)=1+**Tanh**[P1.Vgs]

Ψ1a(Vgs)=ArcTanh[(Ids/Ipk0)-1]

b) GaN and SiC: f1b(Vgs)=1+T**anh**[**Sinh**(P1.Vgs)]

Ψ1b(Vgs)=ArcSinh[ArcTanh[(Ids/Ipk0)-1]]

c)Directly extractable.

H.Rohdin ED-33,N5,May1986 pp. 664

$n_s(V_g)=n_{s0}(\alpha+(1-\alpha)\mathbf{tanh}[(V'_g-V_{gm})/V_1]]$

4 Model Function Selection
Spectral content(derivatives)

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$$\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \sum_{n=0}^{\infty} \frac{(-1)^n x^{2n+1}}{n!(2n+1)} = \frac{2}{\sqrt{\pi}} \left(x - \frac{x^3}{3} + \frac{x^5}{10} - \frac{x^7}{42} + \frac{x^9}{216} - \cdots \right)$$

$I_{ds}ef = 1 + Erf[(\Psi)]/(2/Sqrt[\pi]);\ \Psi = P_1(V_{gs} - V_{pks})$

DC ,1-st equal

1. $I_{ds}ef = I_{pk} + I_{pk} * P_1 * V_{gs} - \frac{1}{3}(I_{pk} * P_1^3)V_{gs}^3 + \frac{1}{10}(I_{pk} * P_1^5)V_{gs}^5$

$I_{ds} = I_{pk}(1 + \tanh(\Psi));\ \Psi = P_1(V_{gs} - V_{pks});\ GaAs$

2. $I_{ds} = I_{pk} + I_{pk} * P_1 * V_{gs} - \frac{1}{3}(I_{pk} * P_1^3)V_{gs}^3 + \frac{2}{15}(I_{pk} * P_1^5)V_{gs}^5$

5-th different

$I_{ds1} = I_{pk}(1 + \tanh(\Psi 1));\ \Psi 1 = P_1(\sinh(V_{gs} - V_{pks}));\ GaN, SiC$

3. $I_{ds1} = I_{pk} + I_{pk} * P_1 * V_{gs} - \frac{1}{6}(I_{pk} * P_1^3)V_{gs}^3 + \frac{1}{40}(I_{pk} * P_1^5)V_{gs}^5$

3-rd different

5 Model Function Selection – Ids Derivatives

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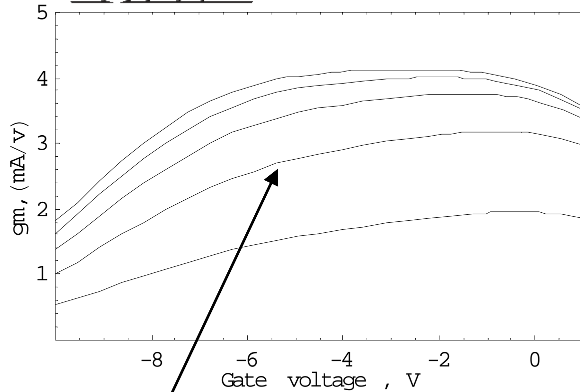
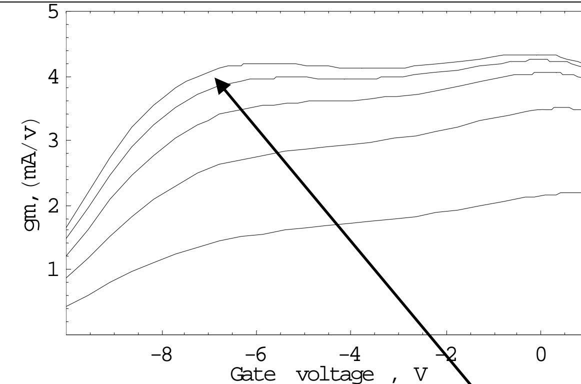




GaAs Gm bell shaped.

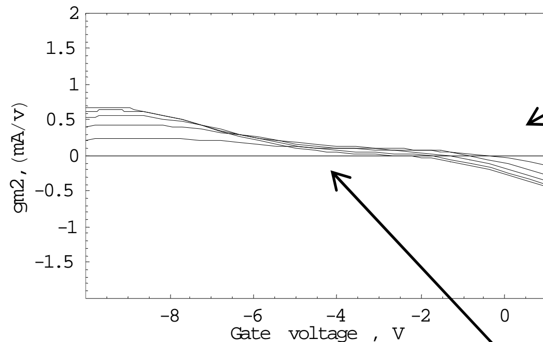
f1a(Vgs)=1+Tanh(P1.Vgs)

Due to the term:(1/6)(Ipk0*P1)Vgs ^{3}>

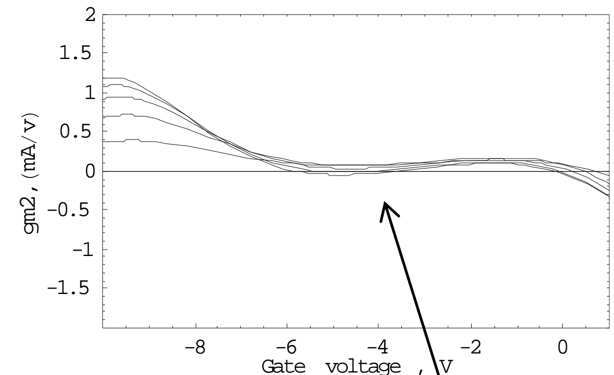
GaN ; SiC Gm:

b) f1b(Vgs)=1+Tanh(**Sinh**(P1.Vgs))

Rectangular shape of Gm



3-rd order of Ids



GaAs Gm2:f1a(Vgs)=1+Tanh(P1.Vgs)

GaN SiC Gm2: f1b(Vgs)=1+Tanh(**Sinh**(P1.Vgs))

Simple Ids model:

5 Parameters: Ipks,Vpks,P1, αs, λ

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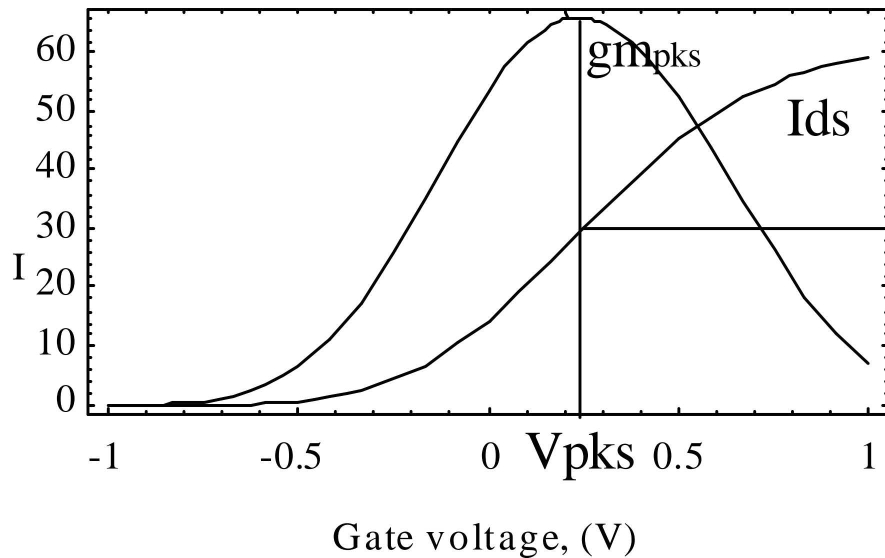

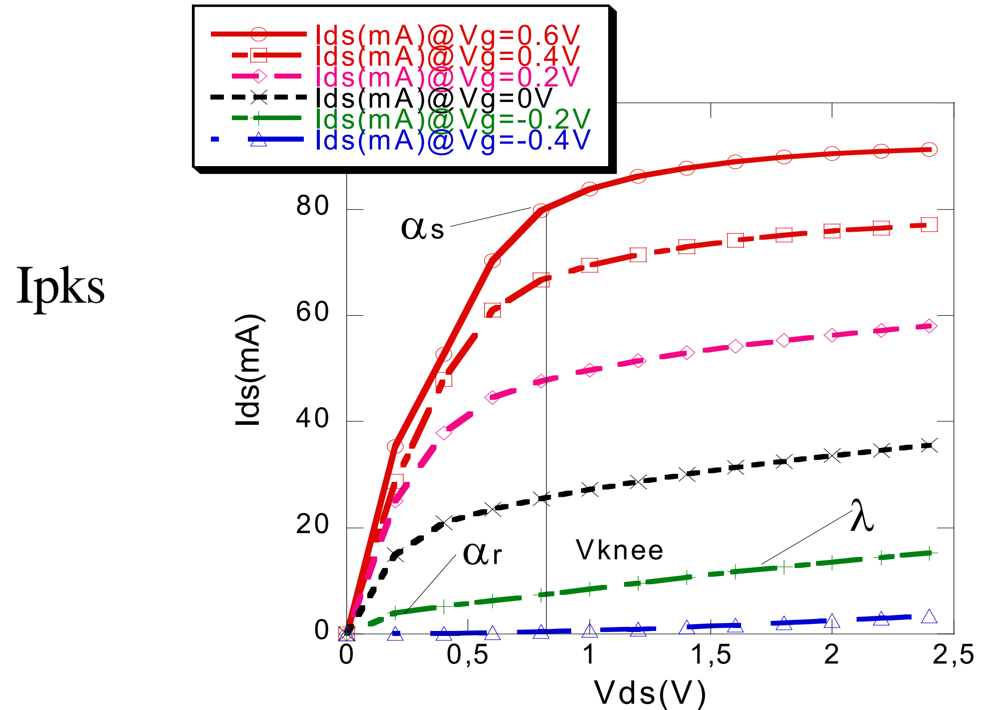

5 Parameters: Ipks,Vpks,P1, αs, λ

Ids, gm are exact at Vpk, typical, global error <10%.

$$I_{ds} = I_{pks}(1+\tanh(\Psi_p)).\tanh(\alpha_s V_{ds})(1+\lambda V_{ds})$$

$$\psi_p = P_{1m}((V_{gs} - V_{pks})); P_{1m} = g_{mpk} / I_{pk}$$

Typical:

$\lambda = 0.001-0.02 GaN; 0.04-0.25\ GaAs;$

$P1 = 0.15-0.3 SiC; 0.35-1 GaN; 1-5 GaAs;$

$\alpha_s = 0.3-0.7 GaN; 0.5-3 GaAs$

Ids: 10 Parameters Model: Ipks, Vpks, P1, αs, λ +ΔVpk, P2,P3, DP, αr

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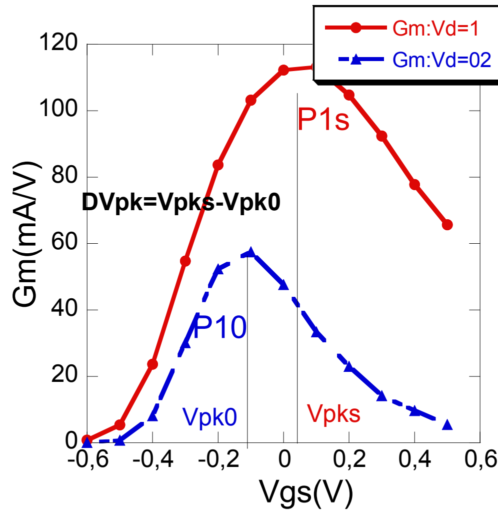
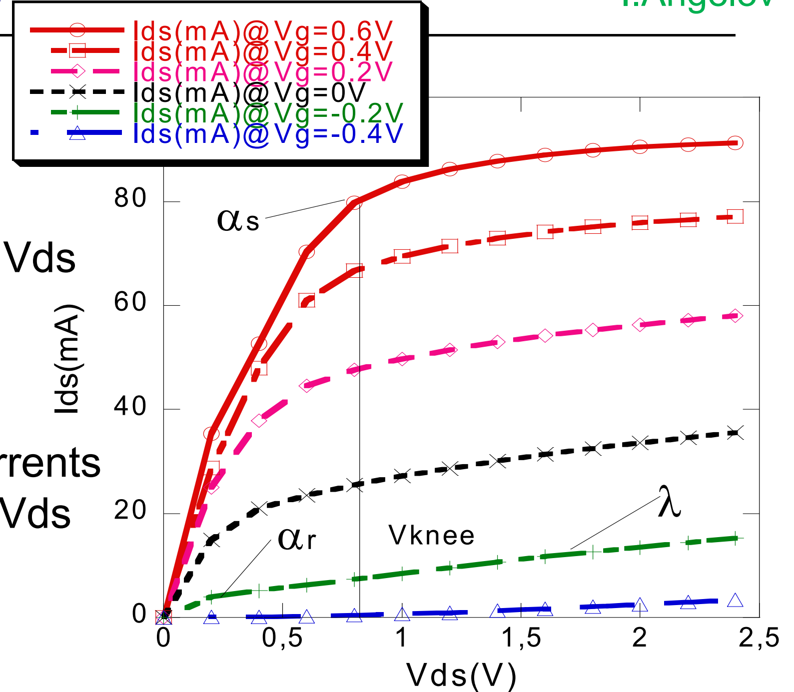


Ipk0,Vpk0,P1=gm/Ipk0
DVpk- change for the Vpk vs. Vds
P2,P3-adjust GM shape
αs- slope at high currents
αr-slope at small currents
λ-slope at high Vds, small currents
DP1-reduction of P1 for high Vds



10 parameters model : 5par. + DVpks,P2,P3,$a_{r,}$DP1

$$I_{ds} = I_{pks}(1+\tanh(\Psi_p)).\tanh(\alpha.V_{ds})(1+\lambda V_{ds})$$

$$\psi_p = P_{1m}((V_{gs}-V_{pk0}) + P_2(V_{gs}-V_{pks})^2 + P_3(V_{gs}-V_{pkm})^3)$$

$$V_{pk}(V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks}\tanh(\alpha_s V_{ds})$$

$$P_{1m} = P_1(f(T))[(1+\Delta P_1)(1+\tanh(\alpha_s V_{ds}))]$$

$$\alpha = \alpha_R + \alpha_S * (1 + \tanh(\psi_p))$$

Typical, global error <3%.

Connection with physical models

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Ipks=0.5*Imax;Vpks=Vpoff+Vbi;
P1=abs(Imax/Vpks); For example:
Imax=0.8;Vpoff=-1.2;Vbi=0.8;

GaN FET

Gm max at Imax/2 (for respective Vgs)

$$I_{ds} = \frac{I_{\max}}{2}(1+\tanh(\Psi_p)).\tanh(2.\frac{V_{ds}}{Vknee})(1+\lambda V_{ds})$$

$$I_{\max} = \frac{q\sigma vs}{10}; \text{Knee voltage } Vknee = R.\mathrm{I}\max;$$

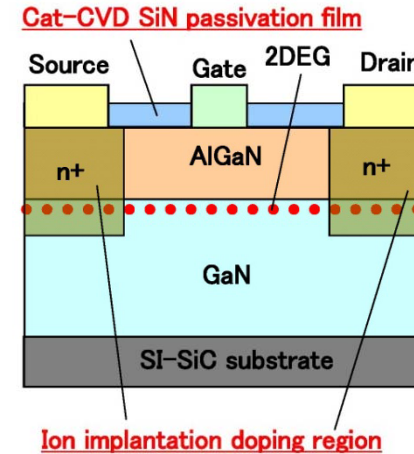
$$R = \frac{(Lsg+Lgd+Lg).10^4}{q\sigma\mu} + 2Rc; Rs = \frac{(Lsg+0.5.Lg).10^4}{q\sigma\mu} + 2Rc;$$

Pinch-off voltage:

$$V_{poff} = \phi_b - \triangle E_c - \frac{q\sigma}{\varepsilon_o.\varepsilon_{AG}} d.10^7; \phi_b = V_{bi} - \triangle E_c$$

$$\triangle E_c = \chi_G - \chi_{AG}; \varepsilon_{AG} = \varepsilon_G + (\varepsilon_A - \varepsilon_G)$$

$$\chi_{AG} = x.\chi_A + (1-x)\chi_G - B_\chi(1-x)x$$



Schematic structure

No.	Physical parameter	Unit	Value
1	Al content of AlGaN (x)	-	0.2
2	Thickness of AlGaN (d)	nm	27
3	Built-in voltage of Schottky gate (Vbi)	V	1.3
4	Polarization charge (σ)	cm-2	7.0e12
5	Electron saturation velocity (vs)	cm/s	9.0e6
6	Distance between source and gate (Lsg)	μ m	1
7	Distance between gate and drain (Lgd)	μ m	2
8	Gate length (Lg)	μ m	1
9	Contact resistance (Rc)	Ω mm	2.4
10	Electron mobility (μ)	cm2/V/s	1300

[49}T. Oishi, H. Otsuka, K. Yamanaka, Y. Hirano, I. Angelov “Semi-physical nonlinear model for GaN HEMTs with simple equations “ INMMIC 2010 Göteborg

Ids Equations – Extended: Breakdown& Dispersion

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$$I_{ds} = I_{pk}(T)(1+\tanh(\Psi_p))\tanh(\alpha V_{ds})(1+\lambda V_{ds} + \lambda_{sb}.e^{kb(V_{dg}-V_{tr})})$$

Breakdown parameters

Important for High Power designs

$$\Psi_p = P_{1m}((V_{gs}-V_{pk0}) + P_2(V_{gs}-V_{pks})^2 + P_3(V_{gs}-V_{pkm})^3)$$

$$P_{1m} = g_{mpk} / I_{pk}$$

Back-gate-Dispersion parameter

$$V_{pk}(V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks}\tanh(\alpha_s V_{ds} + K_{BGate}.V_{BGate} - V_{sb2}.(V_{dg} - V_{tr})^2)$$

$$P_{1m} = P_1(T)[(1+\Delta P_1)(1+\tanh(\alpha_s V_{ds}))]$$

$$P_{2m} = P_2[(1+\Delta P_2)(1+\tanh(\alpha_S V_{ds}))]$$

$$P_{3m} = P_3[(1+\Delta P_3)(1+\tanh(\alpha_S V_{ds}))]$$

$$\alpha_p = \alpha_R + \alpha_S * (1+\tanh(\psi_p)); \alpha_n = \alpha_R + \alpha_S * (1+\tanh(\psi_n))$$

Ipk=f (T); P1=f(T)self-heating

2-nd harmonic

3-rd harmonic vs. Vds

Ids parameters=14 (Ids-10, Breakdown param.=4)

7 important Ids parameters: $I_{pk}, P_1, V_{pk}, \Delta V_{pk}, \alpha_r, \alpha_s, \lambda$ are found directly from measurements and provide accuracy <5%

CAD tool is used for the extraction and optimization.

MEFET Igs Equations -These devices have Gates!!!

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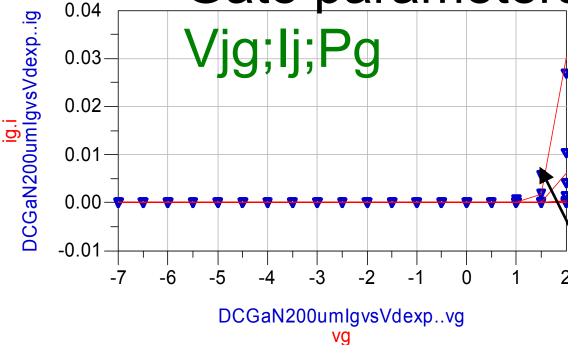
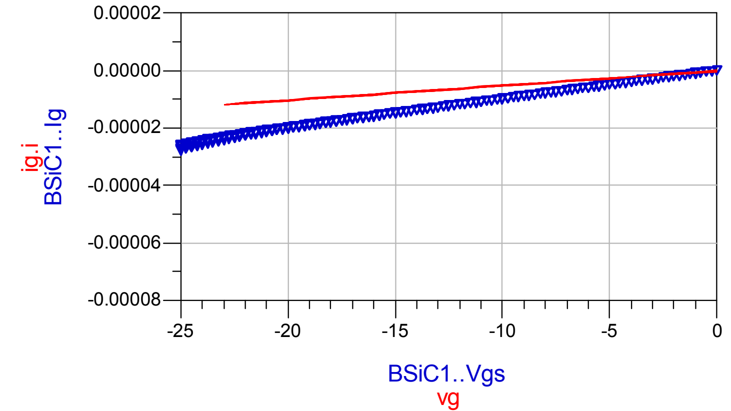
Gate parameters:

Vjg;Ij;Pg



Igs-Vgs AlGaN/GaN HEMT

The diode equation shifted to Vjg at which we operate the device



Igs-Vgs SiC MESFET

Simple: 3 parameters Igs model -Vjg, Ij; slope Pg=1/(Vt*η):

$$I_{gs} = I_j(\exp(P_g.\tanh((V_{gs} - V_{jg}))) - \exp(-P_g * V_{jg})); GaAs, Vjg = 0.8$$

$$I_{gd} = I_j(\exp(P_g.\tanh((V_{gd} - V_{jg}))) - \exp(-P_g * V_{jg})); GaN, Vjg = 1.2$$

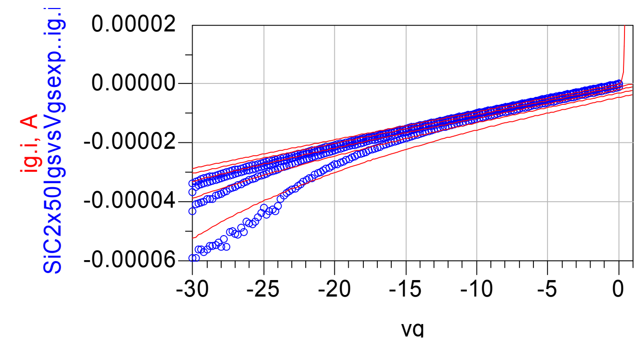
Vds=10,20,40V;Vgd 70V

Breakdown model:3+4parameters

3-simple Igs model + 4(Kbdgate,Ebdgate,Vbdgs, Vbdgd)

$$I_{gsbd} = I_{gs}(1 + K_{bdgate}.\exp(E_{bdgate}((V_{gs} - V_{bdgs})))$$

$$I_{gdbd} = I_{gd}(1 + K_{bdgate}.\exp(E_{bdgate}((V_{gd} - V_{bdgd})))$$



5 b Model Function Selection

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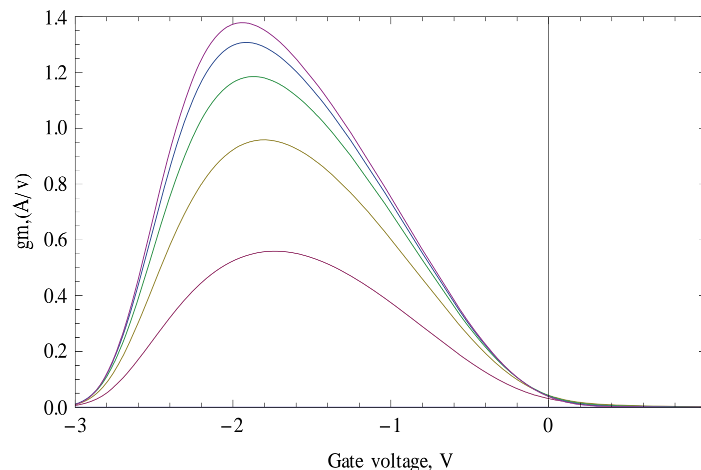
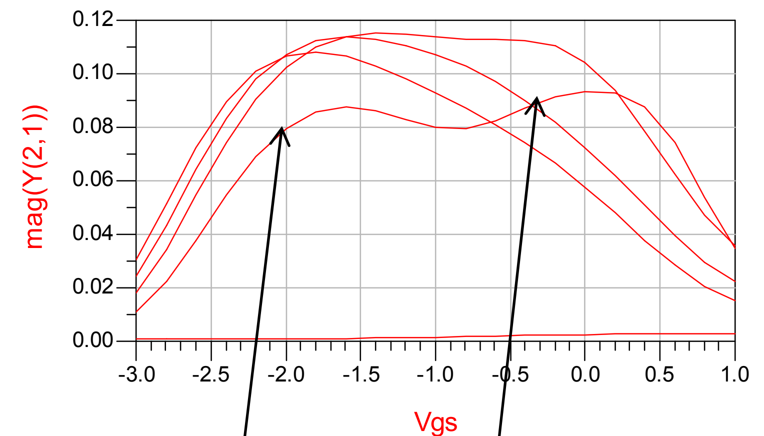
We can add part of Ψ2 working at other voltage **Vpk2,** and **combine.**

We create large variety of Gm shapes with 2 extra parameters **Vpk2, AA.**

Example: Vpk=-0.3; Vpk2=-2; AA=0 to 1

Ψ = P1p ((AA (Vgs - Vpk) + (1 - **AA**) (Vgs - **Vpk2**)
+ P2p (Vgs - Vpk)^2 + P3p (Vgs - Vpk)^3))





Vpk2=-2.0v; Vpk=-0.3V, AA=0.1;

We can, but even for devices with complicated IV, we should Stop to increase parameters-> We can switch to Table Based(TB) or Empirical Table Based (ETB) !!!

Cap FET

1 From S-parameter measurements
Small Signal extraction: Cappy; Berroth....

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Measured&Extracted SS capacitances should be verified for Charge Conservation!

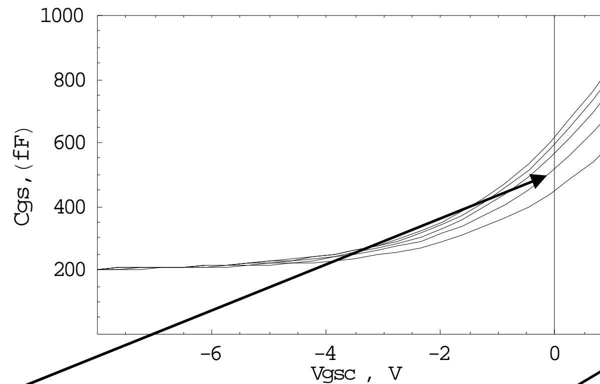
$$\frac{\partial C_{gs}}{\partial V_{gd}} = \frac{\partial C_{gd}}{\partial V_{gs}}$$

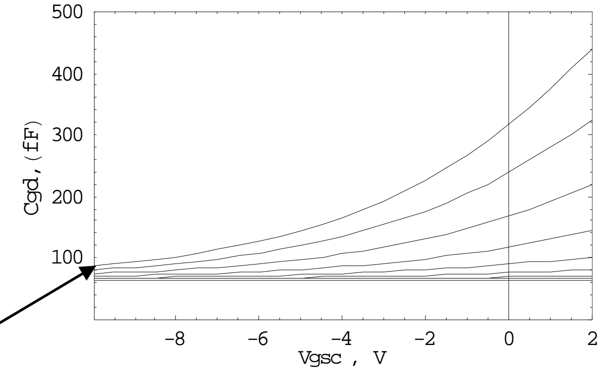
$C_{gs} = C_{gsp} + C_{gs0} *$

$(1+\tanh[\psi_1]).(1+\tanh[\psi_2])$

$\psi_1 = P10 + P11.V_{gs}$

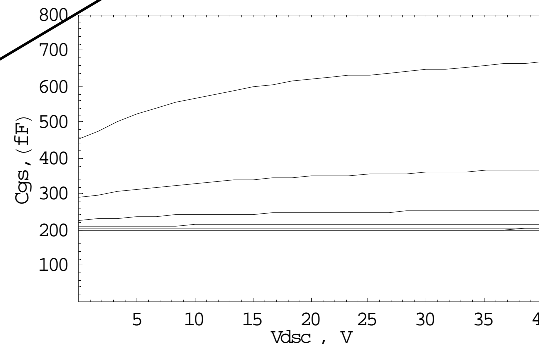
$\psi_2 = P20 + P21.V_{ds}$

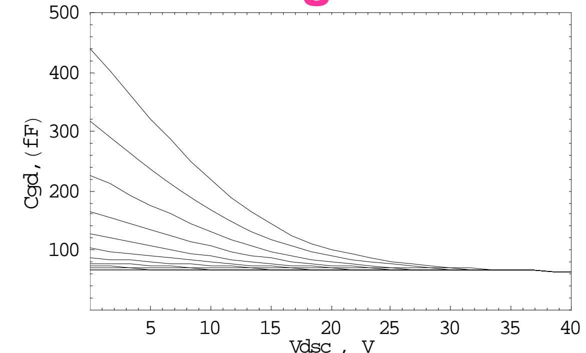




Cgs,Cgd vs. Vgs

Usually, Capacitances are extracted from S-par **measurements in 4-10 GHz range:**





Cgs,Cgd vs. Vds

- Cgdpi-minimum cap;

Cgs0,Cgd0: capacitances at the inflection point;
P11,P21:slope vs.Vgs,Vds

Gate Charge: Capacitance or Charge Implementation?

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1 Capacitance implementation >we don't need transcapacitances! Cap directly from SS extraction!

2 The Cap. Functions should be well defined -∞+ ∞.

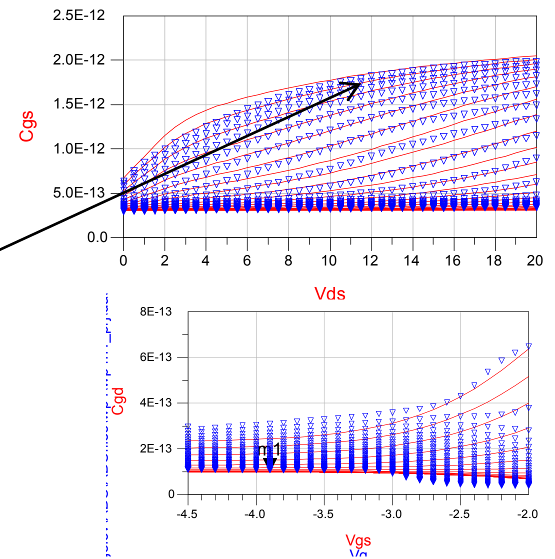
$$\rightarrow SS: C_{gs} = C_{gsp} + C_{gs0}.(1+\tanh[\psi_1]).(1+\tanh[\psi_2])$$

$$\psi_1 = P_{10} + P_{11}.V_{gs} + P_{111}.V_{ds}; \quad \psi_2 = P_{20} + P_{21}.V_{ds}$$

$$C_{gd} = C_{gdp} + C_{gd0}.(1+\tanh[\psi_3]).(1+\tanh[\psi_4] + 2P_{111})$$

$$\psi_3 = P_{30} - P_{31}.V_{ds}; \quad \psi_4 = P_{40} + P_{41}.V_{gd} - P_{111}.V_{ds}$$

High voltage effects for C_{gs}&C_{gd} cross-coupling from Vds -P_{111}



$$HB: \frac{\partial Vgs}{\partial t}; \frac{\partial Vgd}{\partial t}; 2Igsc = \frac{\partial Vgs}{\partial t}Cgs; Igdc = \frac{\partial Vgd}{\partial t}Cgd$$

2 Charge Implementation :

$$Q_{gs} = \int C_{gs}(V_{gs}, V_{ds})dV_{gs} = C_{gsp}.V_{gs} + C_{gs0}.(V_{gs} + Lc1)Th2$$

$$Q_{gd} = \int C_{gd}(V_{gs}, V_{gd})dV_{gd} = C_{gdp}.V_{gd} + C_{gd0}.(V_{gd} + Lc4)Th3$$

$$Lc1 = \frac{\log[\cosh[\psi_1]]}{P_{11}}; Th2 = \tanh[\psi_2]; Lc4 = \frac{\log[\cosh[\psi_4]]}{P_{41}}; Th3 = \tanh[\psi_3];$$

Total Charge Implementation $Qg = Qgs + Qgd$

Integration vs. terminal voltage!

Remote voltage parameter!

We will always have difference in the simulated S-parameters using capacitance or charge implementation using the same coefficients!

> S.Maas Nonlinear Microwave Circuits

Cap Implementation 1-
DC current phenomenon in HB.

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1Cap implementation: **DC current can be observed in HB for Cap.depending on *Vt, Vr***. If the voltage *V* across the capacitors terminal consists of a small and a large amplitude V_0 and V_1, the current ***I*** through that capacitor can be defined as:

$$I = C\frac{dV}{dt} = I_o + I_1;(Eq.1) \quad C \approx C_0 + \frac{dCo}{dV}V_1;(Eq.2) \quad C_0\frac{dV_1}{dt} + \frac{dC_0}{dV}\frac{dV_0}{dt}V_1 = I_1;(Eq.3) \quad \frac{dC_0}{dV}\frac{dV_0}{dt} = G_0;(Eq.4)$$

whereas I_0 and I_1 are small and large amplitude current parts. Linearizing *C* yields Eq.2
Inserting this *C* in Eq.1) and eliminating the second order terms yields Eq.3.
The part Go from Eq.4 is a DC conductance (current) via capacitor which is unphysical.

$$Q_g = aV_{gs}^2 + bV_{gs} * V_{gd} + cV_{gd}^2 (Eq.5) \qquad ig = \frac{dQ_g}{dV_{gs}}\frac{dV_{gs}}{dt} + \frac{dQ_g}{dV_{gd}}\frac{dV_{gd}}{dt};(Eq.6)$$

2 Charge implementation, will not produce DC Current via Cap.- we multiply with j ω, and for ω=0 ,Icap=0

For example, if the total charge Qg is Eq.5(linear combination), the total gate current will be Eq.6.
Assuming *V*gs = *e* sin(w*t*) and *V*gd = *f* cos(w*t*) (*e* and *f* are constants) yields Eq.7
whereas ω is the radian frequency and $A = a.e^2 - c.f^2$ and $B = b.e.f$.
The current is **purely capacitive** and does not have any DC component,**at ω=0 ,Ig=0.**

$$i_g = \omega(A\sin(2\omega t) + B\sin(2\omega t));(Eq.7) \qquad C_{gs}(V_{gs},V_{ds}) = \frac{dQ_g}{dV_{gs}}(V_{ds} = const)\Big|;(Eq.8)$$

Comparison in ADS: Cap, Cgs,Cgd calculated from Charge and Cap implementations:

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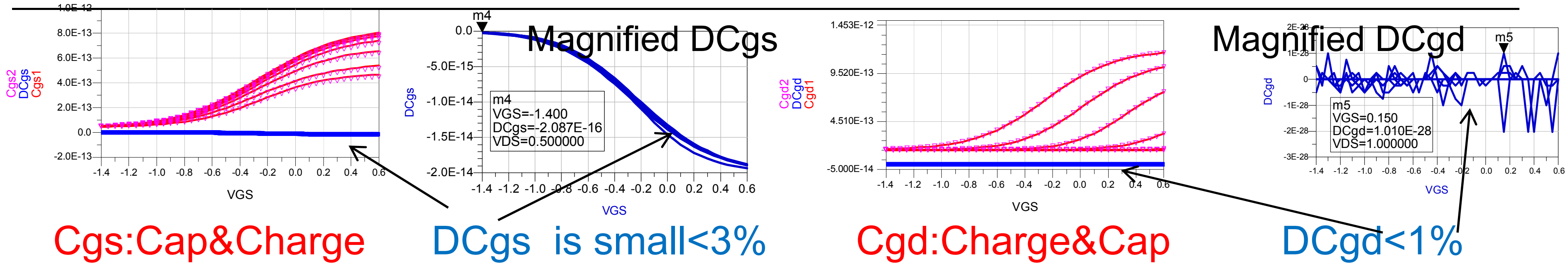
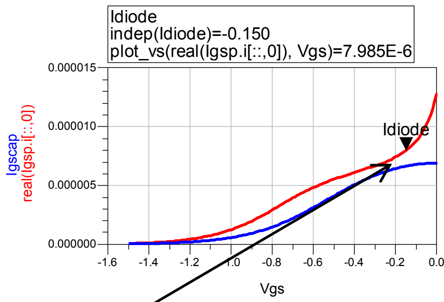
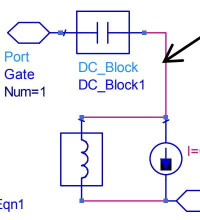
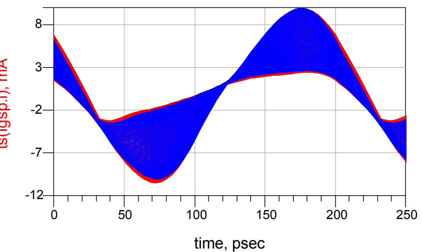


Cgs:Cap&Charge DCgs is small<3% Cgd:Charge&Cap DCgd<1%



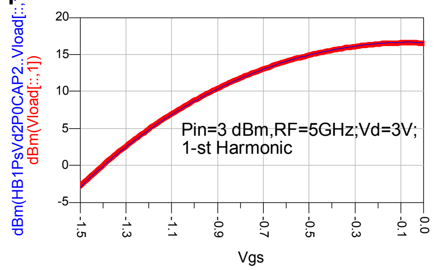


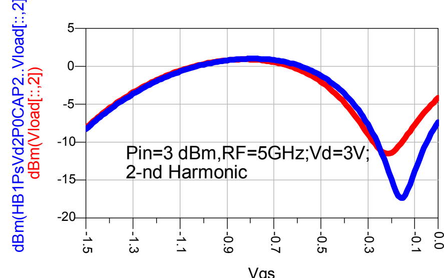
FORCED CHARGE CONSERVATION for Cap. Impl.
DC current component arising from the violation of the charge conservation is blocked with DC block. But, DC current is generated, so HB calculation will be influenced. The inductor allows DC current to flow **without disturbing the input circuit**. Though, the DC current we hide, will influence the PAD, waveforms etc.

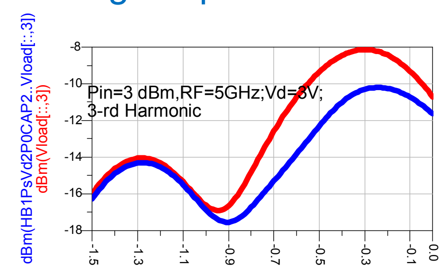


Igs with Cap Implementation Waveforms for Charge&Cap similar, but not equal.

Cap current is the same order as diode current. Harmonics are correct from the charge implmentation!







1-st harmonic, Charge&cap, 2-nd harmonic Charge&Cap, 3-rd Charge&Cap

Mixed Charge-Current (MCC) Implmentation

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MCC- 1Charges are derived the usual way :Integrating the capacitance with terminal voltage, remote voltage parameter.

$$Qgs = f2r(Vds).\int Cgs(Vgs)*dVgs; \quad Qgs= f2r*f11; \quad Qgd = f3r(Vds).\int Cgd(Vgd)*dVgd; Qgd=f3r*f44$$

The constants of the integration are Q_{gs0} and Q_{gd0} .When terminal voltage is 0(short circuit), charge is 0.

2-Calculate time derivative for Terminal charges: f11;f44; Eq.5a, 7a(multiplying **with j**ω)

f11=Cgs0(Vgs+ Log[Cosh[P10+P11 Vgs]]/P11)(Eq5a)

f2r=(1+Tanh[P20+P21 Vds]) (Eq5b)+Cgspi .Vgs;

Qgs0=Cgs0(Log[Cosh[P10]]/P11)(1+Tanh[P20+P21 .Vds]);

Qgst=Qgs-Qgs0; Cgs=D[Qgst,Vgs] (*Eq*6)

f 44 = Cgd0(Vgd+ Log[Cosh[P40+P41 Vgd]]/P41)* (Eq7a)

f3r=(1+Tanh[P30-P31 Vds]) (Eq7b)+Cgdpi Vgd;

Qgd0=Cgd0(Log[Cosh[P40]]/P41)(1+Tanh[P30-P31 Vds]);

Qgdt=Qgd-Qgd0;Cgd=D[Qgdt,Vgd] (*Eq*8)

3 Resulting terminal, cap. current is multiplied with remote voltage dependences f2,f3 f2-Eq.5b, f3-7b to get the node currents Eq.9, 10.

I(gdi,di) <+ ddt(Qgd)*(f3r)-Qgd0*f3r;(*Eq*9)

I(gsi,si) <+ ddt(Qgs)*(f2r)-Qgs0*f2r ;(*Eq*10)

This procedure can be used to implement capacitances dependent on several remote voltages.

The ideal case:

1 **Small Signal analysis- results coincide with Capacitance type Implementation.** We should compare imaginary parts Y11,Y12,Y22.

2 **Large Signal Analysis -results coincide with the Charge type Implementation.** We should look at the Output Power, Harmonics,PAD etc.

3 The DC current via capacitances is 0 or very small.

The radical solution is to use charges, but to make the CAD tool calculate analytically partial derivative of the charge for SS.

I.e. calculate capacitances and use Cap. in the SS analysis.

For HB charges are used directly to get currents. This is easy to arrange for default models- you provide equations for the charges and capacitances (ADS)

Cap Implementation6-Mixed Charge-Current: **Results**

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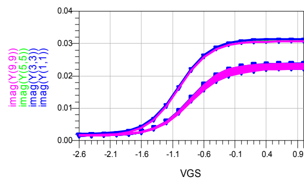
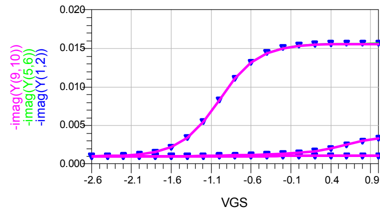
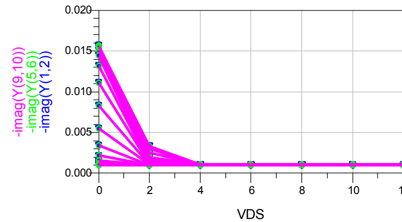
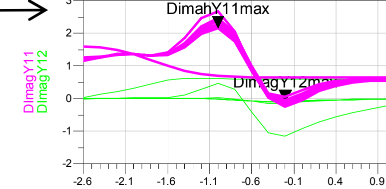


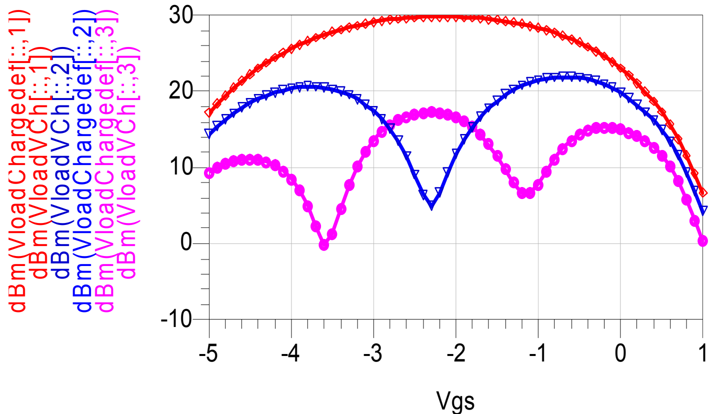




Difference is very small<2%



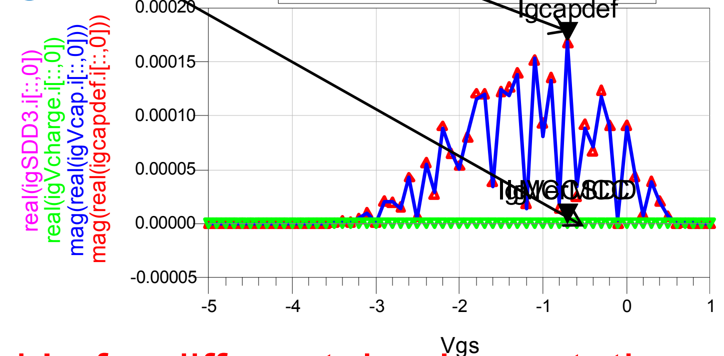
ImaginaryY11,Y12 vs. Vgs and Y12 vs. Vds for different implementation, Cap,**MCC**-Verilog,**MCC** SDD



Igcap=10 ^-4A

IgMCC=10-14A

IgCharge=10-28A



PS:Charge model,MCCVerilog,MCCSDD; Generated Ig for different implementatioons

Dispersion Modelling Implementation

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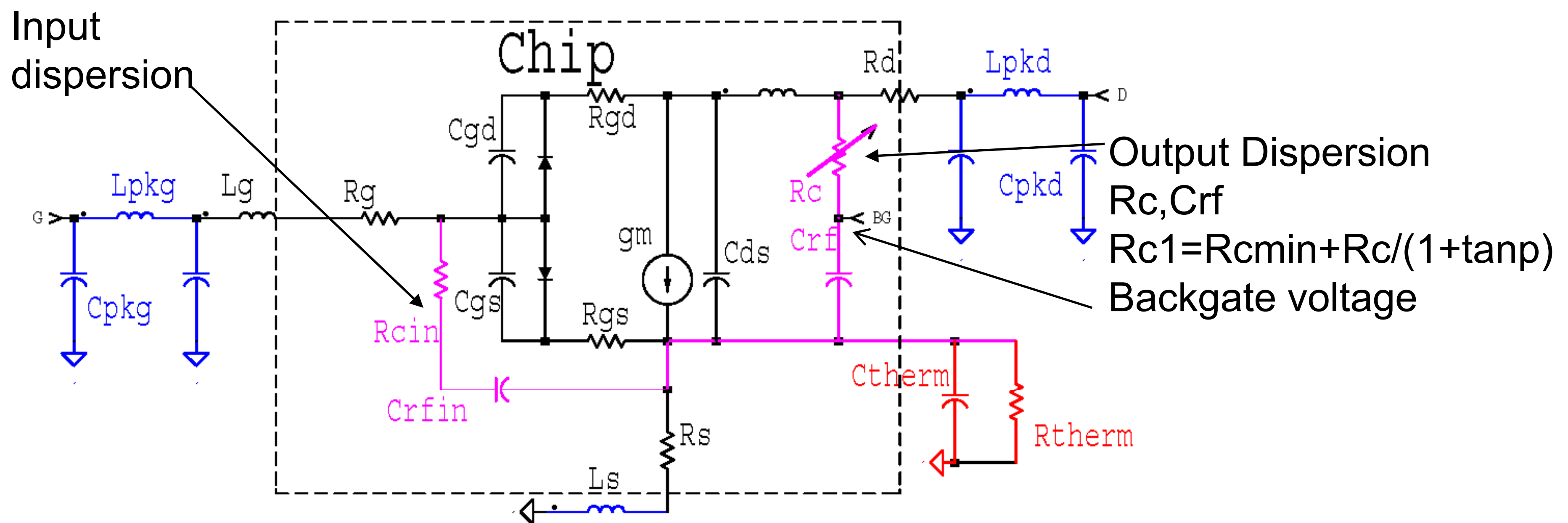
1 Simple> Rc,Crf at the ouput, usually implemented in CAD tools
Rc is bias dependent! Rc1=Rcmin+Rc/(1+tanp)
2 Back-gate Approach: (J. Conger, A. Peczalski, M. Shur, SC,Vol. 29, No.1),ADS2009
3 Physical Approach: (K. Kunihiro, Y.Ohno, ED, Vol. 43, No. 9)
4 Device is symmetric>input (Rcin,Crfin)-output dispersion, Rc,Crf

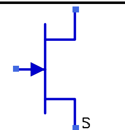


Extended EC for dispersion Modelling–combined Rc and back-gate:5 par.

Model Parameters tot. 69

GaN
Ids parameters-12
Cap parameters-15
Thermal parameters-8
Breakdown-7
Igs-3

Parasitics&package



New in the GaN model implemented in VerilogA , ADS 2009:

1 f1(Ψ)=1+**Tanh**[**Sinh**(P1.Vgs)]

2Rd and Rs are Bias(Rd2) and Temperature Dependent (TcRs),

Rsbdep=Rs*(1+Rd2*(1+tanh(Ψ))); Rdbdep=Rd*(1+Rd2*(1+tanh(Ψ)));

RsbdepT=Rsbdep*(1+TcRs*DTj); RdbdepT=Rdbdep*(1+TcRs*DTj);

3**Delay:Rdel,Cdel**,4 **Backgate dispersion-Kbgate**

5Breakdown for GS,GD Junctions: Kbdgate,Vbdgs,Vbdgd, Pbdg

Spar. Measurements & FIT.

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S(3,3) S(1,1)
freq (1.000GHz to 30.00GHz)

S(4,3) S(2,1)
freq (1.000GHz to 30.00GHz)

S(1,1) S(3,3)
freq (50.00MHz to 14.05GHz)

S(2,1) S(4,3)
freq (50.00MHz to 14.05GHz)

S(3,4) S(1,2)
freq (1.000GHz to 30.00GHz)

S(4,4) S(2,2)
freq (1.000GHz to 30.00GHz)

S(1,2) S(3,4)
freq (50.00MHz to 14.05GHz)

S(2,2) S(4,4)
freq (50.00MHz to 14.05GHz)

AlGaN/GaN HEMT SiC FET. Measured and modelled Spar.

For LS model, it is important to look for the global fit.

For harmonics, DC and Spar fit is not enough!!!

Importance of Correct Derivatives

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For LS & Harmonics modelling we need correct derivatives

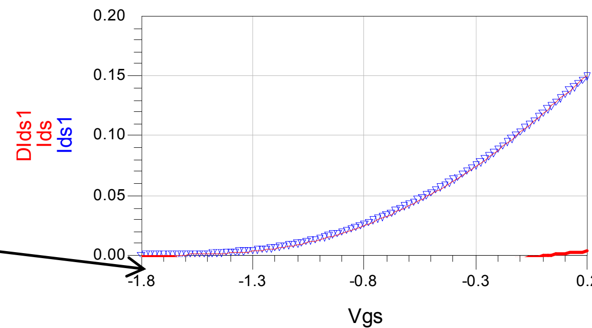
Self-Heating, Dispersion, Memory effects, complicate the picture.

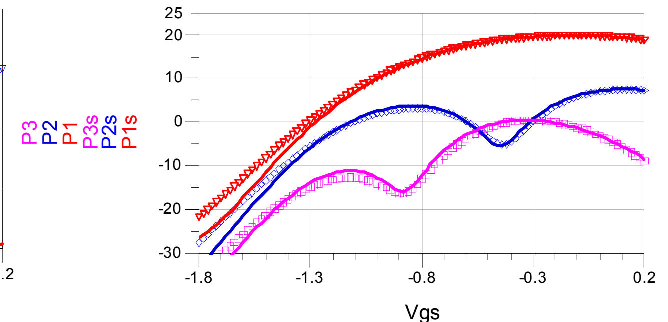
DC data for Ids harmonics are often noisy! Solution:

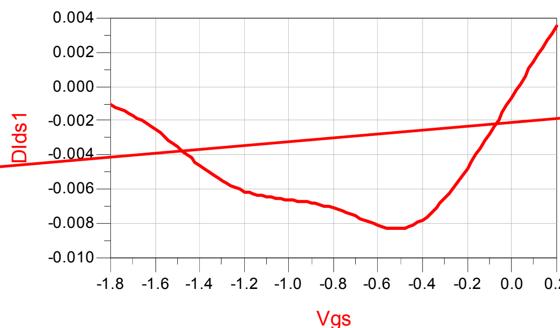
1Power Spectrum evaluation (PS);

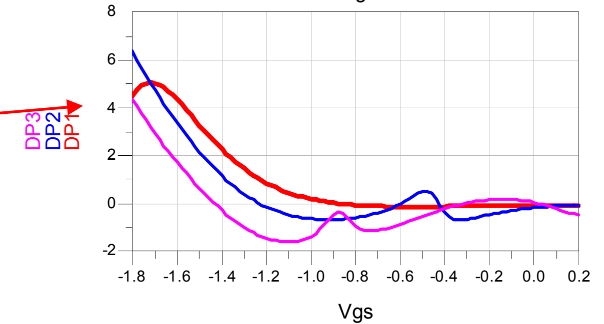
2Load Pull or LSNA or Combined Load Pull & LSNA Evaluation!!

Example:
we change the shape of Ids at pinch-off, i.e.
P3=0.2 to
P3=0.5 in Ids parameters.
Change <2% for Ids,
4-7 dB in harmonics!









PS Measurements-Harmonics vs. Vgs

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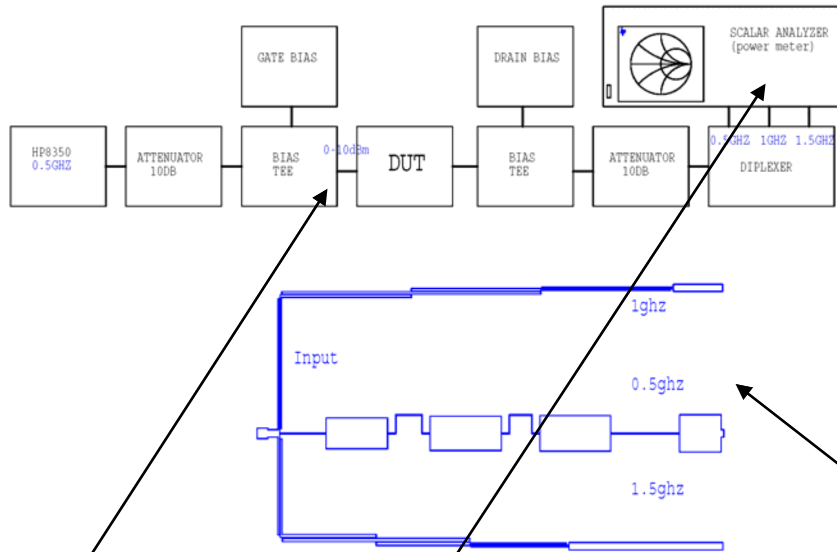
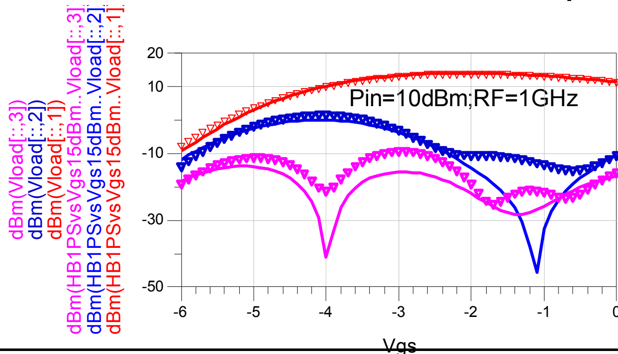


Pin,RF freq, Vds Constant.
1) RF- Low Freq.> current source
2) RF-High Freq.> capacitances
Spectrum analyzer(SA) or ScalarNA(SNA) or Power meter with diplexer filter.

1 Calibrate the input power (Pin=10 dBm for SiC and GaN) at the device terminal for fund. and harmonics.
2 Calibrate losses of output cables,diplexer, SA(orSNA);Keep attenuators directly at the bias tee, close to DUT!!!
3 Measure 1,2,3 harmonics sweeping Vgs(10pts), for several Vds (Vds=0.2; 8V, 16V, 24V for GaN, SiC)



Measured and modeled PS GaN 200 um
f1b(Vgs)=1+Tanh(**Sinh**(P1.Vgs))

Combined LSNA & Load-Pull Measurements- best approach for Device and LS evaluation!

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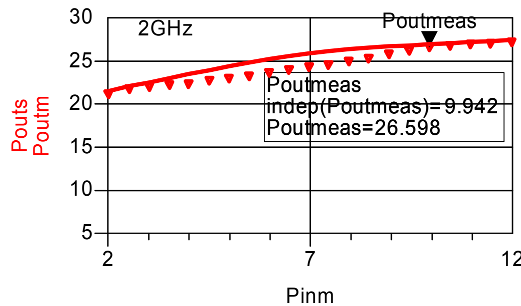
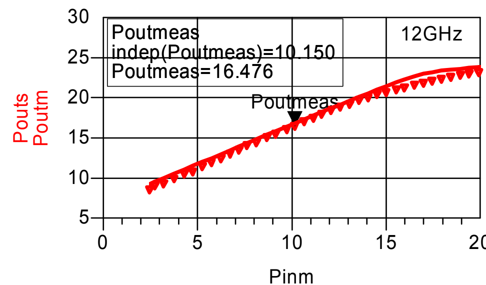
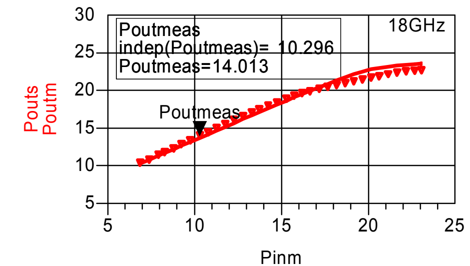
Voltages & Harmonics extracted from the waveforms at the device terminal!

LSNA & Load Pull > better understanding of device behavior at high frequency!

(Ref: On the modeling of High Frequency& High Power Limitations of FET, INMMIC, Rome)





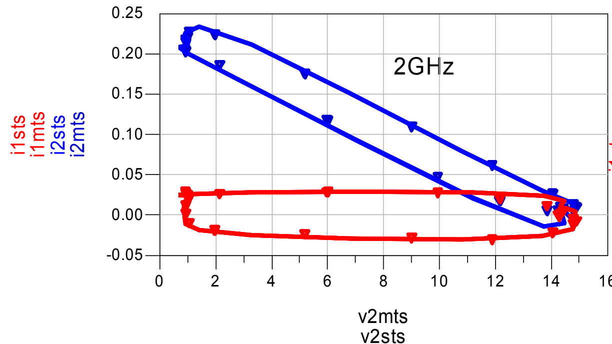


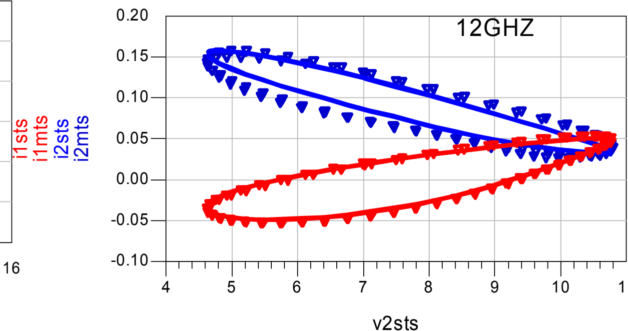
For the same input power 10 dBm:

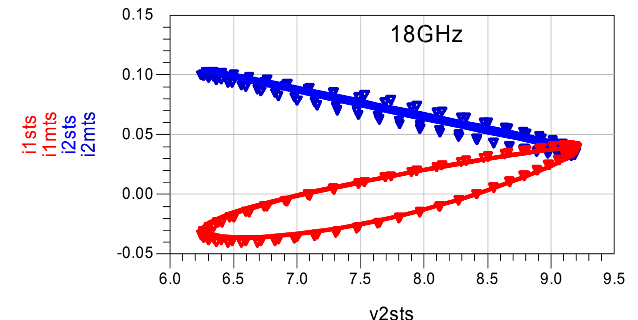
2GHz >Pout=27 dBm

12GHz>Pout=16.4 dBm

18GHz>Pout=14 dBm







The reason for the power decrease: we do not reach at high frequency the DC (Low Frequency)

Knee: **2GHz Vmin=0.8V(DCKnee GaAs)** **12GHz Vmin=4.5V** **18GHz Vmin=6.3V**

The high freqency IV slump is modeled with the gate control network Rdel,Cdel

Empirical &Table Based **(ETB)** LS Model

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ETB: Modeling Complicated IV & Cap shapes. **Empirical model serves as spline function.** Combine the best of Empirical and Table Based Models

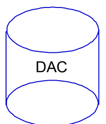
Complicated data (parts of the model) loaded using data set.

High accuracy and good description of harmonics and good convergence. Significant reduction of required measured points(100-200 OK). **Easy to extrapolate out of the measured range.**

ETB LSM **FET**

$I = I_{pk0} \cdot \tanh(\alpha_{table})\,(1+\tanh(P1 * \psi_{table}))\,(1+\lambda_{table})$

1 Difficult to model parameters replaced with table data.
2. Good convergence and infinite number of derivatives.
3. User access to technologically & mounting dependent parameters: Ipk0, Vpk, P1, Ron, Rtherm, Ctherm etc.



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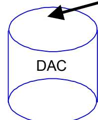
InterpMode=Linear
InterpDom=Rectangular
ExtrapMode=Interpolation Mode
iVar1="VCE"
iVal1=_v8
iVar2="VBE"
iVal2=_v7



DataAccessComponent
DAC_lambda
File="lambda1.citi"
Type=CITIfile
InterpMode=Linear
InterpDom=Rectangular
ExtrapMode=Interpolation Mode
iVar1="VCE"
iVal1=_v8
iVar2="VBE"
iVal2=_v7

Complicated Ids(Vgs) Complicated Ids(Vds)

1 ETB **FET** (MTTS 1999 pp. 2350)
2 ETB **HBT** (EUMC 2004 pp. 229)
3 ETB **FET** (Wiley Int. J. of RF and Microwave Computer-Aided Engineering Vol.14, No. 2, 2004, pp. 122, Johnson *et al.*)

It is Time to Integrate Circuit,Physical Models!

Now, we can trust Physical, Circuit models and we can try to integrate them:

1Circuit designers can create the ideal transistor for their application.

2Using Physical models**, we can design the device** for the specific application.

3 Measurements&Circuit models provide feedback to improve device.

4. Everything made on Si ->GaN,GaAs?

CMOS Large Signal Model

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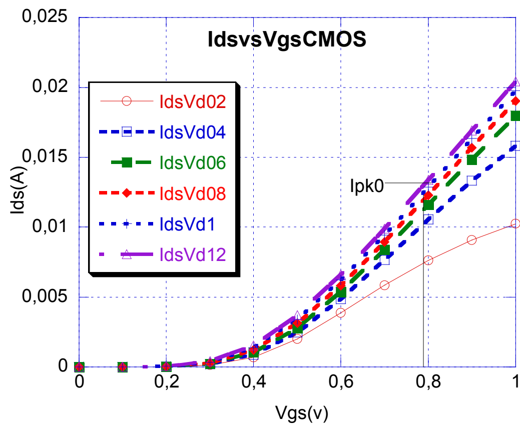
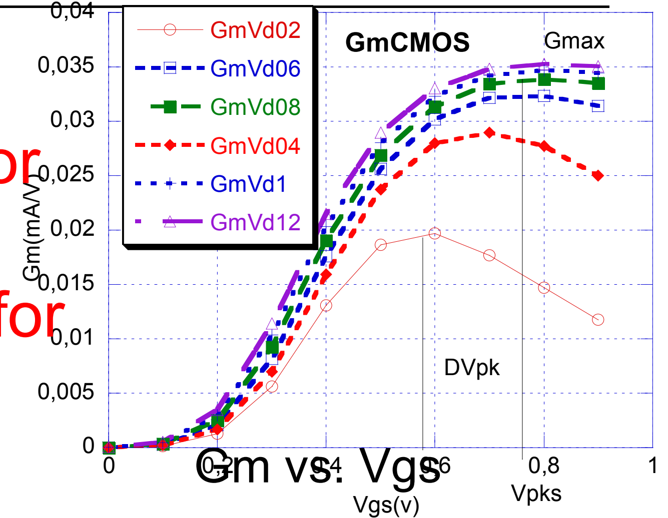
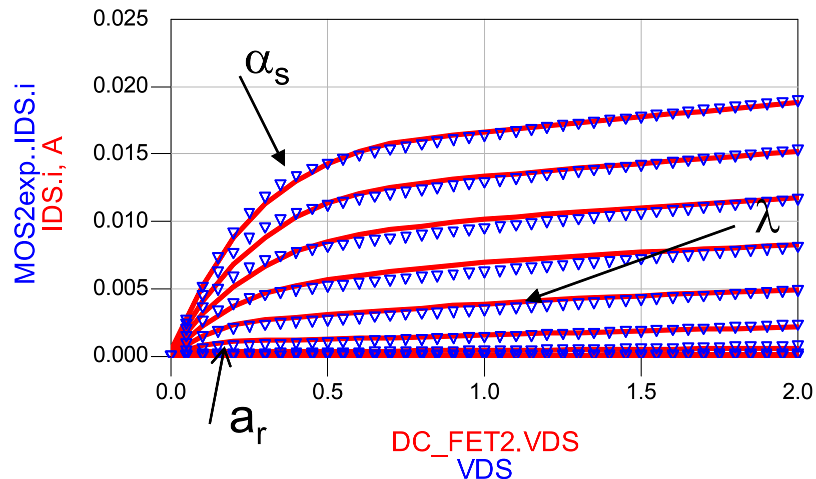


Ids vs. Vgs

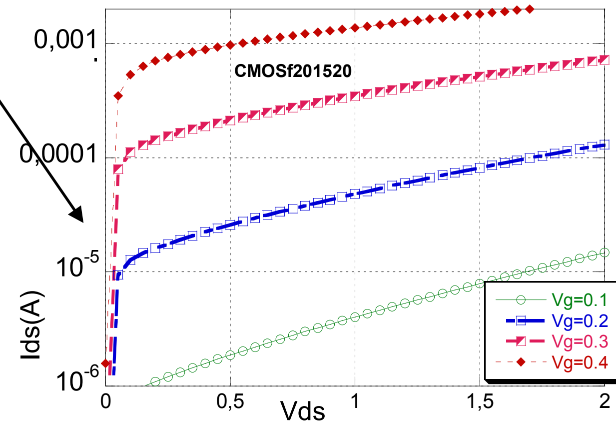
Ids, Gm shape similar for CMOS, GaAs MESFET. **CMOS-Ids exponential** for small currents



Gm vs. Vgs



Measured and modeled IV



EC CMOS-**Bulk influence:**

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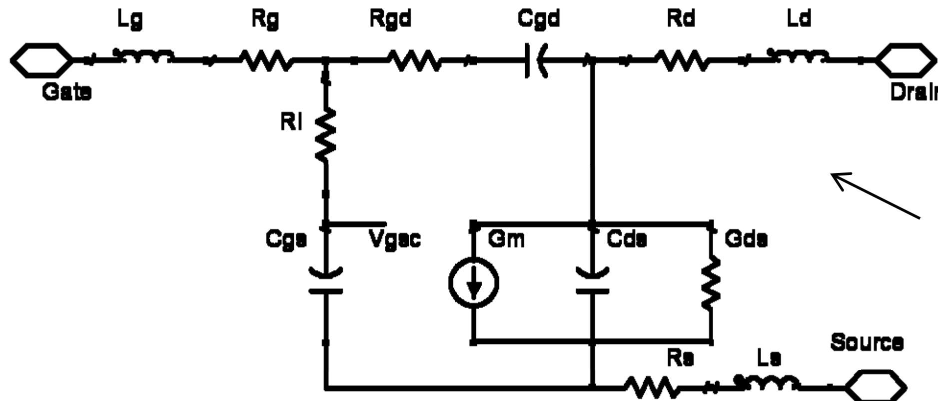
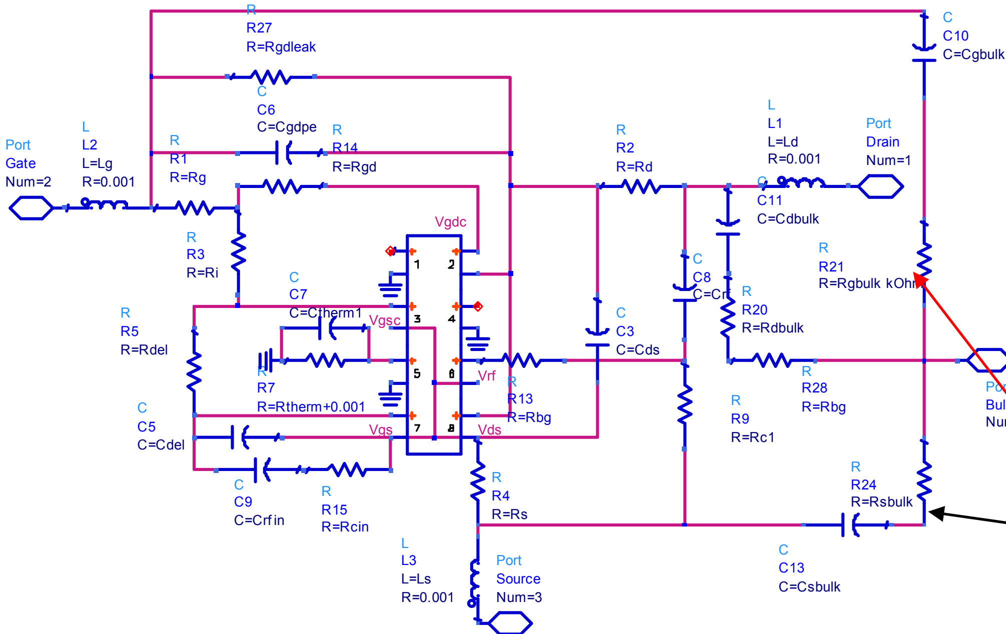


Simplified EC CMOS

GaAs and CMOS EC similar



Equivalent Circuit including Self-heating, Bulk & Bias dependent Dispersion

Rc1= Rcmin+Rc/(1+tanp)

Different is:Bulk influence:

RC Branches: Gate-Bulk, Drain-Bulk, Source-Bulk.

Compact, Equivalent Circuit Models for GaN, SiC, GaAs and CMOS FET

Ids Equations CMOS- symmetric

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A symmetric equation for Ids for accurate modeling for positive and negative *Vds*.
To obtain this: Ids =Idsp-Idsn; Vgs and Vgd control Ids :

$$I_{ds} = I_{dsp} - I_{dsn}$$

$$I_{dsp} = I_{pk}(1+\tanh(\psi_p))(1+\tanh(\alpha_p V_{ds}))$$
$$(1+\lambda_p V_{ds} + \lambda_{1p}\exp(((V_{ds}/V_{kn})-1)))$$

$$I_{dsn} = I_{pk}(1+\tanh(\psi_n))(1+\tanh(\alpha_n V_{ds}))$$
$$(1-\lambda_n V_{ds} - \lambda_{1n}\exp(((V_{ds}/V_{kn})-1)))$$

This term provides exponential dependence

$$\psi_p = P_{1m}(V_{gs}-V_{pk}) + P_{2m}(V_{gs}-V_{pk})^2 + P_{3m}(V_{gs}-V_{pk})^3$$

$$\psi_n = P_{1m}(V_{gd}-V_{pk}) + P_2(V_{gd}-V_{pk})^2 + P_3(V_{gd}-V_{pk})^3$$

$$V_{pk}(V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks}\tanh(\alpha_s V_{ds})$$

$$P_{im} = P_i * \Delta P_i \tanh(\alpha_s V_{ds})$$

$$\lambda_i = \lambda - \Delta\lambda\tanh(\psi)$$

$$\alpha_p = \alpha_r + \alpha_s[1+\tanh(\psi_p)];\ \alpha_n = \alpha_r + \alpha_s[1+\tanh(\psi_n)]$$

Cap Equations CMOS

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CMOS Cap shape & equations different from GaAs FET!

Defined -∞+ ∞ ; Infinite numbers of derivatives!!!!

$$C_{gs} = C_{gsp} + \frac{C_{gs0}\left(1+V_{gs}+P_{10}\right)}{\sqrt{P_{11}+\left(V_{gs}-P_{10}\right)^2}}\left(1+\tanh\left(P_{20}+P_{21}V_{ds}\right)\right)$$

$$C_{gd} = C_{gdp} + \frac{C_{gd0}\left(1+V_{gs}+P_{40}\right)}{\sqrt{P_{41}+\left(V_{gd}-P_{40}\right)^2}}\left(1+\tanh\left(P_{30}-P_{31}V_{ds}\right)\right)$$

$$I_{gsc} = C_{gs}\frac{\partial V_{gs}}{\partial t};\ I_{gdc} = C_{gd}\frac{\partial V_{gd}}{\partial t}$$

Cap parameters:

Cgsp,Cgs0;P10,P11,P20,P21

Cgdp,Cgd0;P40,P41,P30,P31

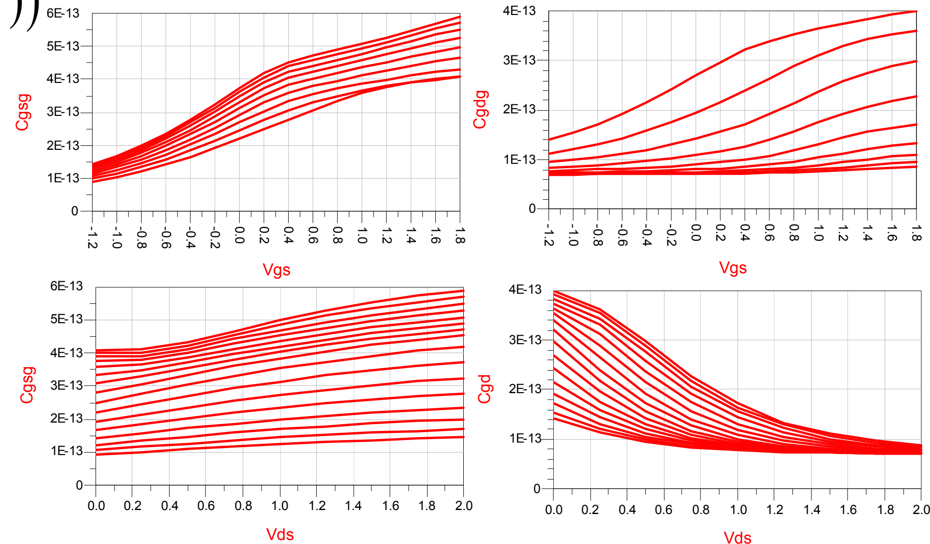
Implementation Cap:

1 Calculated the capacitances

2 Calculate DVgs/dt, DVgd/dt

3 Calculate current via Cap.

Forced charge conservation for Idc=0 via cap (use DCblock, Dcfeed)!



CMOS Capacitances implemented in ADS

FET examples:FIN FET – LS model similar to CMOS

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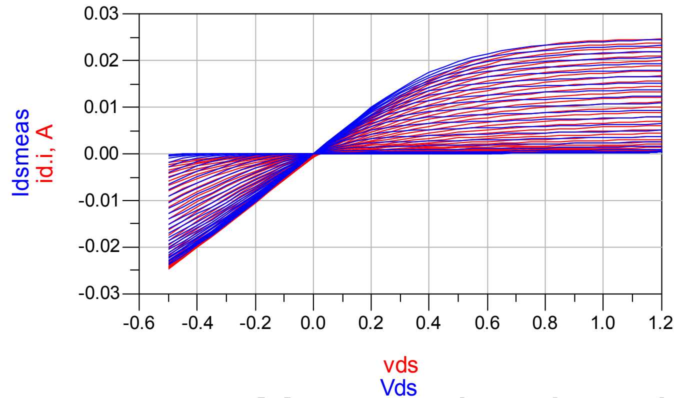
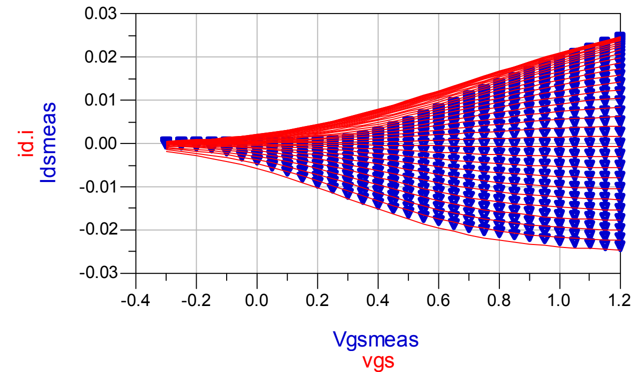
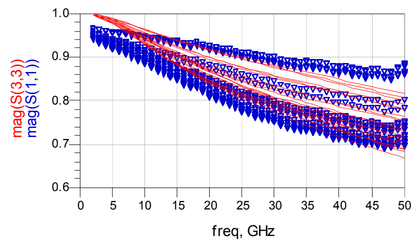
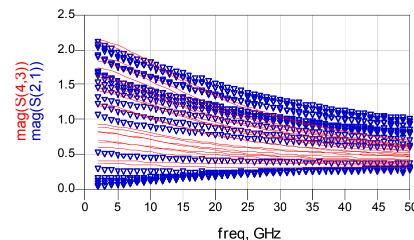
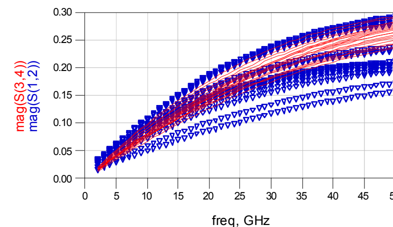


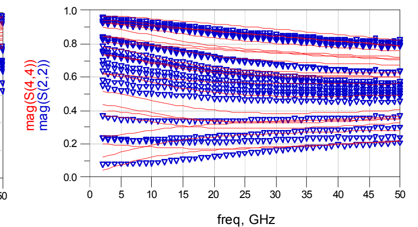


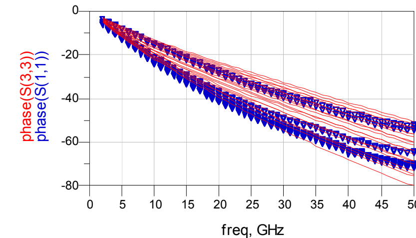
Measured and modelled IV (FINFET 36 um tot. gate size) ADS

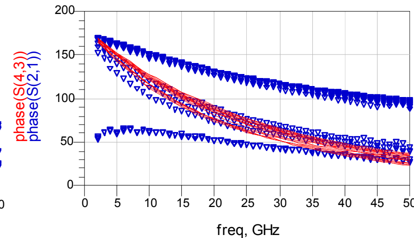


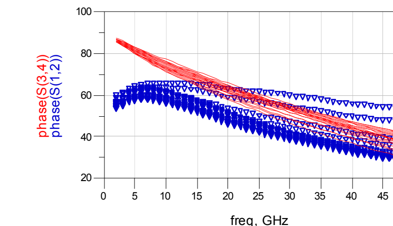


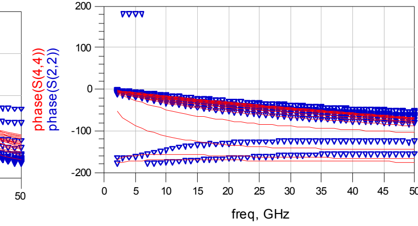












Measured and modeled S-parameters, ADS

RF & LF CMOS **Noise** Model

LS implementation of Pospiezalski Noise Model

Main Noise Contributor is high gate resistance!!!

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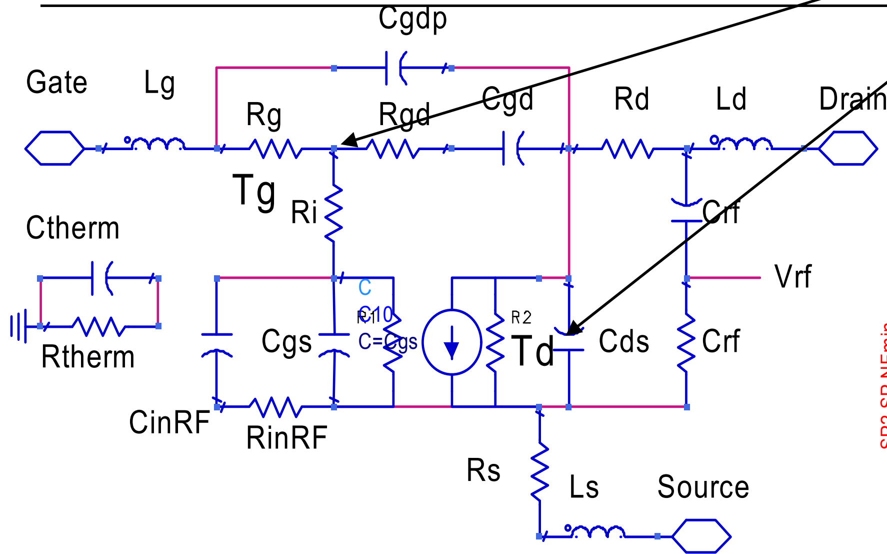
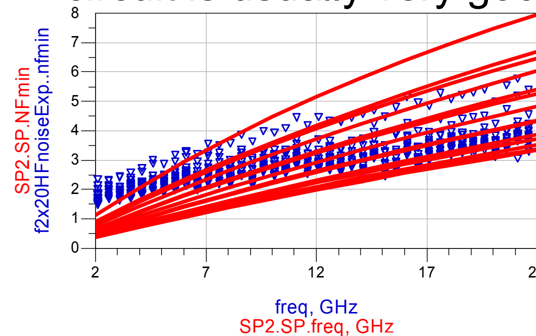
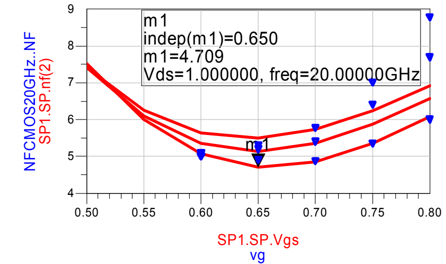


Original SS Pospiezalski Noise model is accurate, because it is using directly derivatives Gm,Gds in the noise calculations and fit for SS equivalent circuit is usually very good.



Measured & modelled minimum NF vs. Freq.



Measured and modelled NF at 20 GHz

Noise parameters: **4 RF+6 LFN**

Td, Tg, **Td1, Idmin**

LF noise: KLF1,KLF2,Ffe,fgr,Kf,Af

Work to be done to reduce Rg to improve the noise.

Idn1=abs(Ids)+abs(Igs);Tdi=**Td***(1+tanh(abs(Vds-Vkn)))
PPout=Lw*4*Kb*TambK*abs(sqrt((Tdi/Tamb)*Idn1+**Td1***(Idn1-**Idnmin**)^2)^2)*(1+KLFO)
KLFO=KLF1*(1/(1+freq^**Ffe**)+KLF2/(1+(freq/**fgr**)^2))
Igs_NoiseSqrd=2*qe*Igs*deltaF+**Kf***(Igs^**Af**)/(freq^**Ffe***deltaF)
Igd_NoiseSqrd=2*qe*Igd*deltaF+**Kf***(Igd^**Af**)/(freq^**Ffe***deltaF)
TgRi=**Tg***(1+tanp)*tanh(alphap*Vds)*(1+lambda*Vds)

Conclusions

I.Angelov

A general purpose large-signal modeling approach was proposed, implemented in CAD tools and experimentally evaluated. Models show good accuracy and stable behavior in HB simulations.

Acknowledgements

•SSF, Sweden

Colleagues : C. Fager, K. Andersson, M. Ferndahl,, H. Zirath, N. Rorsman, D. Schreurs, M. Mierzwinski, A. Inoue, K. Kanaya, S. Maas, W. Curtice for the help and valuable discussions. **S.D.GL.**

Thank you for your attention!

Meyer's Law, part of Murphy's LAW:

It is a simple task to make things complex, but a complex task to make them simple.

Questions?

References

I.Angelov

[1] S. Maas, Nonlinear Microwave and RF circuits, Artech House 2003.
[2] R. Anholt, "Electrical and Thermal Characterization of MESFETs, HEMTs, and HBTs," Artech House, 1995.
[3] L. D. Nguyen, L. Larson, U. Mishra “Ultra-High-Speed MODFET: A Tutorial Review”, Proceedings of the IEEE, Vol.80, N4, 1992, pp.494
[4] H. Rohdin, P. Roblin,”A MODFET DC Model with Improved Pinch off and Saturation Characteristics” IEEE Trans ED, Vol. ED-33, N5, 1986, pp.664-672.
[5] R. Johnoson, B. Johnsohn, A. Bjad,” A Unified Physical DC and AC MESFET Model for Circuit Simulation and Device Modeling” IEEE trans ED, Vol. ED-34,N9,1987, pp.1965-1971.
[6] M. Weiss, D. Pavlidis, “The Influence of Device Physical Parameters on HEMT Large-Signal Characteristics”, IEEE Trans. MTT, Vol-36, N2, 1988, pp.239-244.
[7] C. Rauscher, H. A. Willing, ”Simulation of Nonlinear Microwave FET Performance Using a Quasi-Static Model,” IEEE Trans. MTT., vol. MTT-27, no. 10, pp. 834-840, Oct. 1979.
[8] W. Curtice, “A MESFET Model for Use in the Design of GaAs Integrated Circuit,” MTT., vol. 28, no. 5, pp. 448-455, 1980.
[9] A. Materka and T. Kacprzak, “Computer Calculation of Large-Signal GaAs FET Amplifiers Characteristics," IEEE Trans. MTT.", vol. 33, no. 2, pp. 129-135, 1985.
[10] T. Brazil,"A universal Large-Signal Equivalent Circuit Model for the GaAs MESFET," Proc. 21st EuMC, pp. 921-926, 1991
[11] G. Dambrine and A. Cappy,”A new Method for Determining the FET Small-Signal Equivalent Circuit”, IEEE Trans. MTT, vol. 36, pp. 1151-1159, July 1988.
[12] Berroth, M.; Bosch, R.; High-frequency equivalent circuit of GaAs FETs for large-signal applications MTT Vol.39, Issue 2, Feb. 1991 pp: 224 - 229
[13] Berroth,M.; Bosch R.”Broad-band determination of the FET small-signal equivalent circuit” MTT, Vol.38, N7, July 1990 pp: 891 - 895
[14] M. Ferndahl at all, “A general statistical equivalent-circuit-based de-embedding procedure for high-frequency measurements,” *IEEE Trans. MTT.*, vol56, n 12, 2008, pp.2962-2700
[15]D. Root, B. Hughes, ”Principles of nonlinear active device modeling for circuit simulation”, #2 Automatic radio Frequency Technique Group Conf. ,Dec 1988
[16] D. Root, S. Fan, J. Meyer,” Technology-Independent Large-Signal FET Models: A Measurement-Based Approach to Active Device Modeling, 15 ARMMS Conf, Bath UK Sept. 1991.
[17]D. Root, “Measurement-based mathematical active device modeling for high frequency circuit simulation,” IEICE Trans. Electron., vol. E82-C, no. 6, pp. 924-936, June 1999
[18]D. Root ; Nonlinear charge modeling for FET large-signal simulation and its importance for IP3 and ACPR in communication Circuits and Systems, MWSCAS 2001. Proc.4th IEEE Midwest Symp.Vol. 2, 14-17 pp.768 - 772
[19] R. B. Hallgren "TOM3 Capacitance Model: Linking Large- and Small-signal MESFET Models in SPICE," MTT, vol.47, n5, pp. 556 (May, 1999).
[20] R. J. Trew, "MESFET Models for Microwave CAD Applications," Microwave and Millimeter-Wave CAE, vol. 1, no. 2, pp. 143-158, April 1991.
[21] J. P. Teyssier at all, ”A new Nonlinear I(V) Model for FET Devices Including Breakdown Effects,” IEEE Microwave and Guided Wave Letters, vol. 4, no.4, pp.104-107, April 1994.
[22] K. Kunihiro, Y. Ohno, ”A Large-Signal Equivalent Circuit Model for Substrate-Induced Drain-Lag Phenomena in HJFET’s” IEEE Trans. ED,Vol.43, N9,1996, pp.1336-1342.
[23] J. Conger, A. Peczalski, M. Shur,” Modeling Frequency Dependence of GaAs MESFET Characteristics” IEEE Journal of Solid State Circuits, Vol. 29, N1, 1994 pp. 71-76
[24]. Scheinberg, N.; Bayruns ” A low-frequency GaAs MESFET circuit model”, Solid-State Circuits, IEEE Journal of ,Volume: 23 , Issue: 2 , April 1988,pp. 605 - 608
[25]Canfield, P. Modelling of frequency and temperature effects in GaAs MESFETs”; Solid-State Circuits, IEEE Journal of, Volume: 25, Issue: 1, Feb. 1990, pp. 299 – 306
[26] M. Lee at all “A Self-back-gating GaAs MESFET model for Low-Frequency anomalies”, IEEE Trans. on ED, Vol.37, N.10 Oct., pp.2148-2157.
[27] C. Camacho-Penalosa and C. Aitchison, ”Modeling Frequency Dependence of Output Impedance of a Microwave MESFET at Low Frequencies,” Electronics Letters, Vol. 21, N 12, pp. 528-529, June 1985
[28] J. Reynoso-Hernandez and J. Graffeuil,”Output Conductance Frequency Dispersion and Low-Frequency Noise in HEMT's and MESFET's,” MTT-37, n. 9, pp. 1478-1481, Sept. 1989.
[29] P. Ladbrooke, S. Blight, ”Low-Field Low-Frequency Dispersion of Transconductance in GaAs MESFETs with Implication for Other Rate-Dependent Anomalies,” IEEE Trans. ED-35, no. 3, pp. 257, March 1988.
[30] G. Kompa, ”Modeling of Dispersive Microwave FET Devices Using a Quasi-Static Approach,” Int. Journal of Microwave and Millimeter-Wave Computer-Aided Engineering, vol. 5, No 3, pp.173-194, 1995
[31] M. Paggi at all”Nonlinear GaAs MESFET Modeling Using Pulsed Gate Measurements, ”IEEE Trans. MTT-36, no. 12, pp. 1593-1597, Dec.,1988.
[32] J. P. Teyssier at all "A Pulsed S-parameter Measurement set-up for the nonlinear characterization of FETs and Bipolar Transistors," Proc. 23rd EuMC, pp. 489, Madrid, 1993.
[33] J. M. Lopez at al., Design Optimization of AlInAs-GaInAs HEMTs for High Frequency Applications!”, IEEE Trans. ED, vol 51, n 4, April 2004, pp. 521-528
[34] J. Bandler at all ”Efficient Large-Signal FET Parameter Extraction Using Harmonics,” MTT-37, no. 12, pp. 2099-2108, Dec. 1989.
[35] Angelov at all.Extensions of the Chalmers Nonlinear HEMT and MESFET model, MTT, Vol. 46,N 11, Oct. 1996, pp.1664-1674.
[36] Angelov, H. Zirath, N. Rorsman, "Validation of a nonlinear HEMT model by Power Spectrum Characteristics," IEEE MTTS Digest, pp.1571-1574, 1994.
[37] Angelov A. Inoue, T. Hirayama, D. Schreurs, J. Verspecht “On the Modelling of High Frequency& High Power Limitations of FETs INMMIC Rome 2004
[38] Angelov at all “ On the large-signal modelling of AlGaN/GaN HEMTs and SiC MESFETs, EGAAS 2005 pp.309 - 312
[39] Angelov at all “Large-signal modelling and comparison of AlGaN/GaN HEMTs and SiC MESFETs”, 2006. APMC 2006 pp:279 - 282
[40] ADS,MO, Ansoft Designer user manuals
[41] Angelov at all “An empirical table-based FET model” MTT, Vol. 47, N12, Dec.1999 pp:2350 - 2357
[42] Angelov at all “An Empirical Table Based HBT large signal model”;EUMC, 2004. 34 Vol. 1, 11-15 Pp:229 – 232
[43] Angelov at all “CMOS large signal model for CAD,.; Microwave Symposium Digest, 2003 Vol. 2, 8-13 June 2003 pp:643 - 646
[44] Angelov at all “CMOS Large Signal and RF Noise Model for CAD, EUMC, 2006. Sept. 2006 Pp.217 - 220
[45] Johnson at all ”Generalized nonlinear FET/HEMT modeling (p 122-133) Wiley International Journal of RF and Microwave Computer-Aided EngineeringVol.14, No. 2, 2004, pp. 122
[46] S.Gunnarsson at all” 220 GHz (G-Band) Microstrip MMIC Single-Ended Resistive Mixer ; Microwave and Wireless Components Letters, IEEE Volume 18, Issue 3, March 2008 pp.215 - 217
[47] S.Gunnarsson at all A 220 GHz Single-Chip Receiver MMIC With Integrated Antenna ;Microwave and Wireless Components Letters, IEEE Volume 18, Issue 4, April 2008 pp:284 – 286
[48] S.Gunnarsson at all; A G-band (140 – 220 GHz) microstrip MMIC mixer operating in both resistive and drain-pumped mode , IEEE MTT-S 2008 pp 407 – 410
[49]T. Oishi, H. Otsuka, K. Yamanaka, Y. Hirano, I. Angelov Semi-physical nonlinear model for HEMTs with simple equations INMMIC 2010 Göteborg

Linear Scaling CMOS

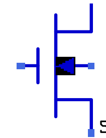
I.Angelov

Ipk0=Ipk0w*Wtot
Cds=Cdsw*(Wtot+0.05)
Cgspi=Cgspiw*(Wtot+0.01)
Cgs0=Cgs0w*(Wtot +0.01)
Cgdpi=Cgdpiw*(Wtot+0.01)
Cgd0=Cgd0w*(Wtot+0.01)
Cgdpe=Cgdpew*(Wtot+0.01)
Rg=0.01+Rgw/Wtot
Ri=0.01+Riw/Wtot
Rs=0.01+Rsw/Wtot
Rd=0.01+Rdw/Wtot
Rgd=0.01+Rgdw/Wtot
Rtherm=0.01+Rthermw/Wtot
Lg=2 pH+ Lgw
Ld=2 pH+Ldw

Ls=2 pH+Lsw
Ij=Ijw*Wtot
Rgbulk=Rgbulkw*Wtot
Rdbulk=Rdbulkw*Wtot
Rsbulk=Rsbulkw*Wtot
Rcmin=Rcminw*Wtot
Wtot=Nfing*Wfing*1000
Wtot1=Nfing*Wfing*Lfing

Scaling Parameters:
Nfing,Wfing,Lfing,Gcont.Lgate
Tot. number of model parameters, including self-heating, dispersion and scaling: 70

ADS Implmentation



MOSscaled2x20n1
CMOS1

Idsmod=1
Ipk0w=1.1 A
Vpks=0.955 V
DVpks=0.052 V
P1=2.14
P2=+0.07
P3=0.40
P5=0
alphar=0.40
alphas=2.68
alphaV=2.68
Vk=0.758
lambda=0.051
lambda2=0.0003
Lvg=0.0015

Lvg2=-0.00015
B1=0.1
B2=3.7
Lsb0=0
Vtr=3.0 V
Vsb2=0 V
Cdsw=100 fF
Cgspiw=50 fF
Cgs0w=500 fF
Cgdpiw=50 fF
Cgd0w=500 fF
Cgdpew=50 fF
P10=0.02
P11=1.45
P20=0

P21=0.32
P30=0
P31=0.32
P40=0.02
P41=1.45
P111=0.0001
Vjg=0.90 V
Ijw=0.5e-8 A
Pg=2
Rgw=0.5 Ohm
Riw=0.1 Ohm
Rsw=0.05 Ohm
Rdw=0.1 Ohm
Rgdw=0.1 Ohm
Lgw=16 pH

Lsw=15 pH
Ldw=28 pH
Rthermw=1.0 Ohm
Ctherm=0.01 F
TcIpk0=0.001
TcP1=-0.001
TcCgs0=0.001
TcCgd0=0.001
TcLsb0=0.001
Tamb=25
Cgbulk=5 fF
Cdbulk=5 fF
Csbulk=15 fF
Rgbulkw=2.3 kOhm
Rdbulkw=1.2 kOhm

Rsbulkw=1.7 kOhm
Rcminw=200 Ohm
Rc=5 kOhm
Nfing=2
Wfing=10 um
Lfing=0.12 um
Gcont=1
taum=0.39 psec
Crf=1 pF
Rcin=300 kOhm
Crfin=15 fF

Circuit <>FET model<>Physical models<>Device Design

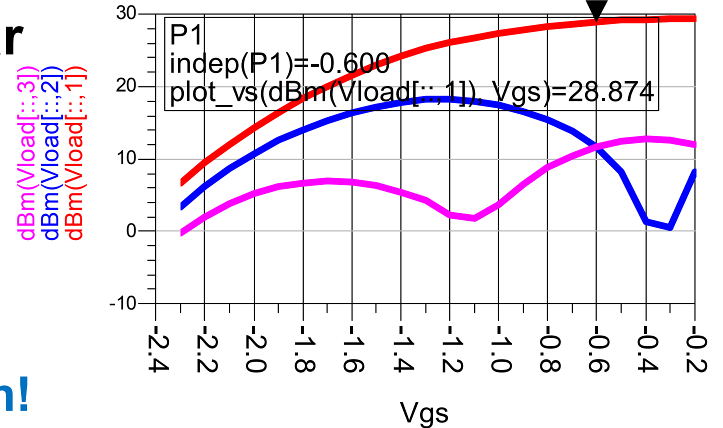
Example: 1mm FET: Pout & Harmonics

I.Angelov

Examples :Application oriented P1=Gm/Ipk:

a) High Gm/Ipk;P1>4 high gain, but non- linear

b) Low P1<1 Low gain, but Linear



a) High Gain HEMT P1=5

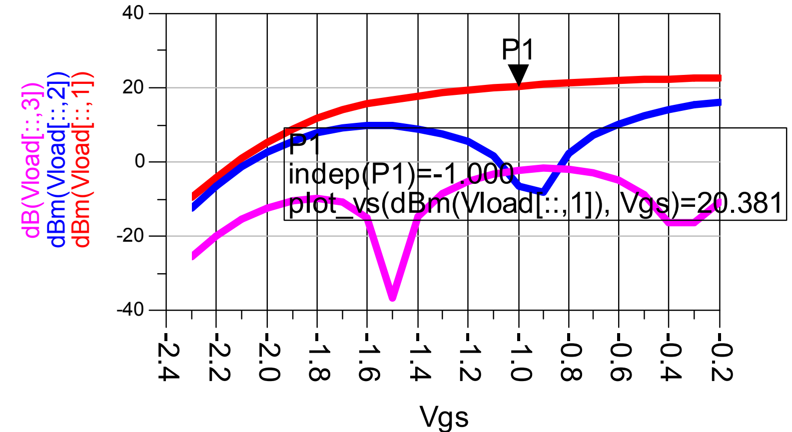
Vpk=0.21; Ipk0=0.3A; **Ichan=0.6A;**

for Ids=10mA, gm=50ms!!

Very good for Small Signal, Low Noise & High Gain!

P1out= 29 dBm; but strong harmonics-

P2h=10 dBm , Very Good for Multipliers!



b) Typical HEMT: P1=2.5

- Vpk=-0.5V; Ipk0=0.24A; Ichan=0.48A;

P1out= 30 dBm; P2h= -10 dBm

> Medium Power &Linear