Total Virtual Fabrication of Advanced CMOS Devices and Processing

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Abstract

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Recent advances in semiconductor 3-D device architecture (FinFET, TriGate, embedded memories) and increasingly elaborate process integration flows including High-K/Metal-Gate and multilevel patterning steps have dramatically increased the complexity of integrated circuit processes. The cost and turn-around-time of technology development using traditional trial-and-error experimental methodologies has concurrently increased to the point where it is unsustainable. A more systematic virtual-development approach is required for advanced technologies to tune 3-D device geometry and achieve time-to-market objectives. 3-D process modeling based on a voxel algorithm has already demonstrated its value for MEMS and more recently for semiconductor processing. This capability has been demonstrated in the semiconductor space for a wide range of technology development capabilities in a simple, robust, high-speed software platform. Several examples will be discussed including virtual fabrication, variation analysis and design-process interaction for advanced CMOS flows. Furthermore we demonstrate the interfacing of this virtual design platform to the traditional finite element platforms for the TCAD electrostatic device analysis.
Outline

- Technology Development Landscape
- Virtual fabrication model methodology
- Case studies
- Summary
Recent Technology Roadmap

- Strained Silicon, Copper Interconnects, 193 nm lithography
- 2nd generation strained Silicon, eSiGe, wafer orientation for low-cost apps
- High-K + metal gate, Computational Litho
- Second generation high-K
- Ultra-thin body, Fully depleted SOI?
- Tri-gate (FinFET), Double Patterning

Graphical timeline:
- 2002 to 2016
- MOS-AK 26 Sept 2014
Semiconductor industry trends:

- Entering an era of performance scaling, not geometric scaling
  - Performance enabled by new materials
  - Performance enabled by new device geometry
- Litho mask count is increasing (from 20 to 45 in last 12 years)
  - Prevalence of LE*\textsuperscript{n}, SAnP, all the EUV precursors
- Process complexity is increasing
  - 500+ steps for Front End of Line
- Unique process flows for Logic, DRAM, Flash
- Technology development costs are increasing
  - 200mm $\rightarrow$ 300mm $\rightarrow$ 450nm wafers
- ITRS: Front-End process modeling is a “grand challenge”

- TAT and wafer cost are becoming unsustainable
Virtual modeling objectives

• Predictability
• Robustness
• Efficient in time/storage
• One path to achieve these objectives –
  • Model the outputs rather than the inputs
  • Behavioral model rather than first principal (Reactor-scale)
  • Provide a basic set of process models for non-critical areas
    • Etch, Deposit/growth, Photolithography, planarization
  • Provide a more detailed process suite for critical areas
  • Provide ‘fab-like’ virtual metrology suite of tools for direct measure of output
  • Provide ability to perform batch-jobs
More complex processes

- Multi etch
  - Etch multiple layers with provision for
    - Sputtering, sidewall copolymer deposition, taper etc

- Silicon directional etch – along major crystal directions

- CMP planarization
  - Overpolish regimes and dishing

- Visibility deposition
  - Snowfall like depositions

- Epi growth with plane variability

- Pattern dependent etching
  - Isolated and nested feature distinctions
Automate in-line, local measurements of critical technology parameters.

Mimic real in-fab metrology, replace slow out-of-fab destructive characterization.
What is SEMulator3D?

A Powerful 3D Semiconductor Modeling Platform

• Applicable to ANY process & ANY layout
• Replaces build & test with **accurate** 3D modeling of large areas & complex process sequences
• Provides validation and visualization of relationships between design and process
• Provides a **predictive** view of design-technology interactions
SEMulator3D is primarily a **voxel** modeling tool.

Voxels are like 3D pixels:

A 2D shape

The same 2D object, represented with pixels. Note the partly filled pixels!

A similar 3D shape, represented with voxels. The color represents the **volume fraction**.

SEMulator3D voxels can be partly filled, just like pixels.
SEMulator3D uses patented voxel modeling algorithms:

- Data compression exploits self-similarity in the model to reduce memory use.
  - Compression ratios of 10,000:1 (vs. storing all voxels) are not uncommon
  - Particularly efficient for semiconductor processes
- Acceleration algorithms also exploit self-similarity in the model to greatly reduce the time required to build models.

BUT – voxel size has a large impact on performance.

- In SEMulator3D, voxel size is called “Model Resolution” and can be chosen by the user.
- Lower resolution to save compute time and memory.
- Higher resolution to resolve small details.

Guideline: At least 2 voxels across the smallest model feature.
Case Studies

1. Virtual Process window study
2. Electrostatic response analysis to FinFET profile variability

1) SISPAD 2013
2) DAC 2014
cap nitride remain thick enough to protect the gate silicon during the dual-epitaxial source/drain modules, but must also be thin enough to ensure complete top-removal for uniform silicide formation.

Gate transition over n-p boundary compounded by multiple generated mask edges during spacer and trench etches.
Case study 1 – model calibration

Model calibration to inline physical measurements

Cross gate section

Through gate section
Case study 1 – create test structure and determine response

Enhanced response structure

Integration of calibrated virtual nitride profiles vs Edge placement variation
Case study 1 – characterize test structure

Sensitivity to Edge placement variation

Sensitivity to Edge placement variation
Case study 1 – optimize profiles

Resist profile initial vs model optimized

Test Structure Yield
\( \frac{N_{\text{THRESHOLD}}}{N_{\text{TOTAL}}} \)

Optimized vs Non-Optimized

Optimized response curve

NET: Process window extended from \( 2\sigma \) to \( 5\sigma \)

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Case study 2 – Electrostatic response to Fin profile variation

- Virtual model build of FinFET
  - Using standard 6-T SRAM cell
  - Conventional Graphics input

- Virtual DOE around Fin nominal parameters
  - Depth (100nm), Fin angle (7°)
  - STI recess etch (30nm)

- Apply appropriate meshing

- Output to TCAD system
Case study 2 – Fly cell model build
The final replacement metal gate (RMG) device cross-section is accurately modeled by a calibrated set of high-k parameter values that realistically represent existing published data.
Case study 2 – Large area mesh to TCAD

Export Large Area Mesh

SEMulator3D Expeditor Variation
Study of Fin Profile

Crop Individual Devices

Fin Width vs Mandrel SIT Spacer Width

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Case study 2 – Device Simulation

Hole density profile response to bias condition - key to optimizing performance

3D hole-density contour plot through the middle of the channel from source-to-drain. Note discrete impurity atoms in Fin.
Summary

- Virtual fabrication methodology enables significant yield predictability verified by product results
- Ability to provide predictable process simulations and to emulate fab measurements is key
- Virtual fabrication methodology provides predictable structural variations for electrostatic analysis engines