Introducing Process and Statistical Variability Parametric Yield Analysis through SPICE Simulation

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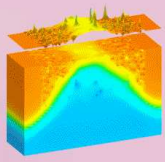
Introduction

Two fundamental types of variability exist in modern silicon chips; process variability and statistical variability. Variability introduced through process variations is complex, but usually well characterized. Process variability presents as a gradual change in parameters across chip, across wafer and wafer to wafer. Statistical variability, which is exacerbated by aggressive scaling, is caused by atomic scale charge and device structure variations including random discrete dopants (RDD), line edge roughness (LER) and polysilicon granularity[1]. Unlike systematic variability, statistical variability is truly stochastic and varies on a transistor to transistor level.



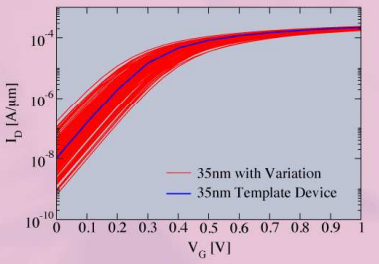


Figure 1: The effect of statitical variability on Id Vg characteristics of MOSFET

Methodology

Large ensembles of SPICE simulations are performed using ***Randomspice***[2], a tool developed at the University of Glasgow which is capable of generating random instances of any nominal circuit with the correct statistical variation in its constituent components.

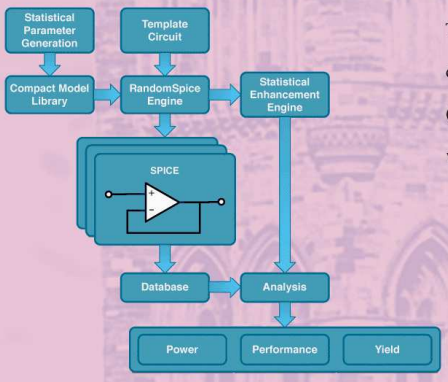


Figure 2: Randomspice process flow

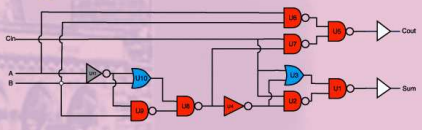


Figure 3: 1 bit adder schematic

The following assumptions are made in the simulations below:

a) statistical variability is captured, to first order, by the distribution of *vth0*, which is assumed to be Gaussian

b) Corners are defined by 1 and 2σ of the threshold voltage (*vth0*) parameter distribution.

c) σ is chosen as 15%, 20% and 30% of the mean threshold voltage.

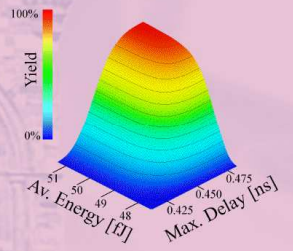


Figure 4: CDF[3] with equi-yield contours, allowing for power/performance/yield tradeoff

Including Process Variability

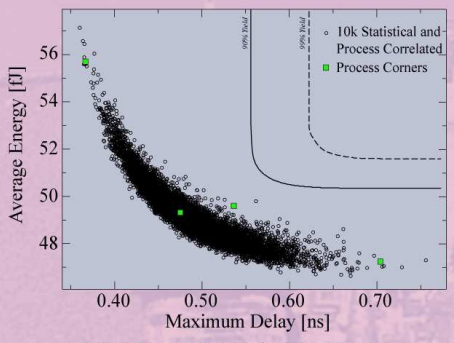


Figure 5: Process and statistical with correlation

Figure 5 showns the same simulations of statistical and process with fully correlated p and n type device process varibility.

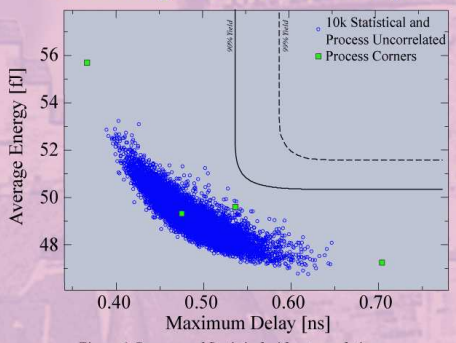


Figure 6: Process and Statistical without correlation

Figure 6 showns process and statistical varibaility without correlation between p and n-type devices.

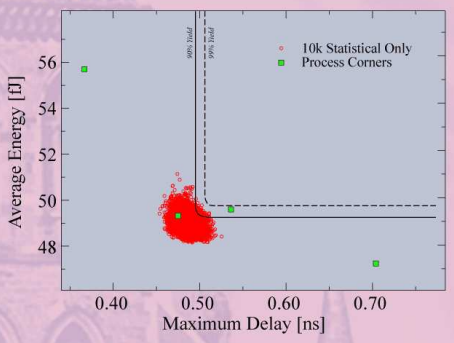


Figure 7: Average energy per transition with maximum delay with 90 nd 99% yield contours

In as system dominated by statistical variability corners are shown to be extrememly pessimistic.

Statistical Variability and Yield

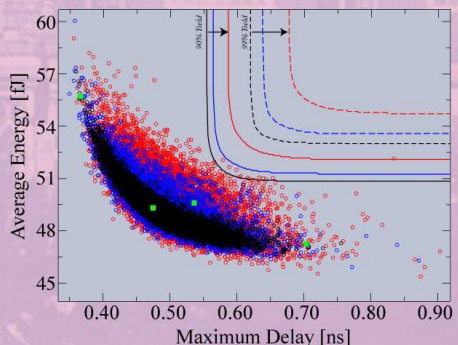


Figure 8: The effect of increasing statistical variability on Yield

As can be seen statistical variability pushes the 99% yield to lower and lower delay/power performance, in this case reducing performance by almost 10%.

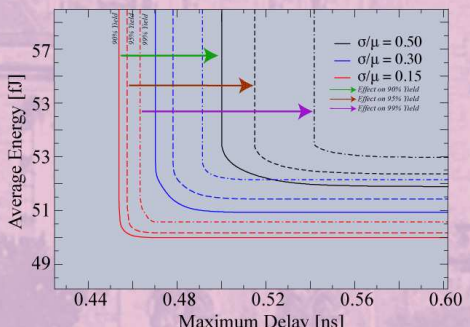


Figure 9: The effect of increasing variability on Yield

As shown in Figure 9, higher amounts of statistical variability causes the high yield contours (99%) to be extened exponentially. This time causing a delay increase of almost 20%.

Conclusions

The effect of increasing varibility on high yield parameters is shown, with high variabity causing an exponential decrease in high yield performance. This is shown to be true in the absence and presence of statistical variability.

References

[1] Gareth Roy, Andrew R. Brown, Fikru Adamu-Lema, Scott Roy, and Asen Asenov "Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs" IEEE Trans. on Electron Devices, VOL. 53, no. 12, 2006

[2] P. Asenov, D. Reid, C. Millar, S. Roy, Z. Liu, S. Furber, A. Asenov "Generic Aspects of Digital Circuit Behaviour in the Presence of Statistical Variability", Proc. VARI 2010

[3] B. W. Silverman, "Density estimation for statistics and data analysis," Chapman & Hall/CRC, 1986, p. 76