A Practical Guide for Accurate Broadband On-Wafer Calibration in RF Silicon Applications

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Arbeitskreis MOS-Modelle und Parameterextraktion
MOS Modeling and Parameter Extraction Working Group

Outline

- Motivation
- Standard Technique vs. On-Wafer Calibration
- Suitable Calibration Methods
- Implementation
- Practical Results
- Summary

Motivation

- The operation frequency of modern RF CMOS devices approaches 110GHz and beyond
- Accurate device characterization at operation frequencies is a must
- Limited accuracy of the standard technique beyond 40 GHz (with the pad parasitic de-embedding)

Motivation

- Historical view:
  - Microwave community: customized on-chip calibration is the standard technique
  - Digital community (Si): off-chip calibration + de-embedding
- Progress in development of customized calibration on silicon over the last years
  - Work from NIST (US), PTB (Germany)

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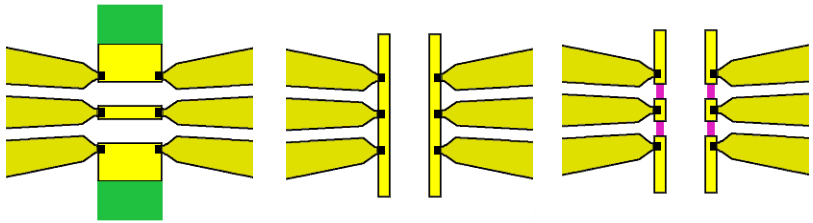
Standard Technique

Standard technique: a two-step approach

- Step 1: calibration to the probe tip end with commercial calibration substrate
- Step 2: de-embedding of DUT contact pads and interconnects

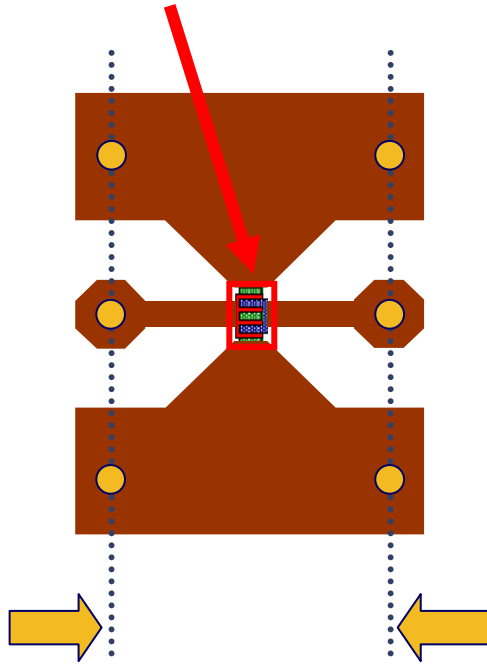
Step1:

off-wafer calibration



Line Reflect Load (Match)

Step 2: Reference plane after de-embedding

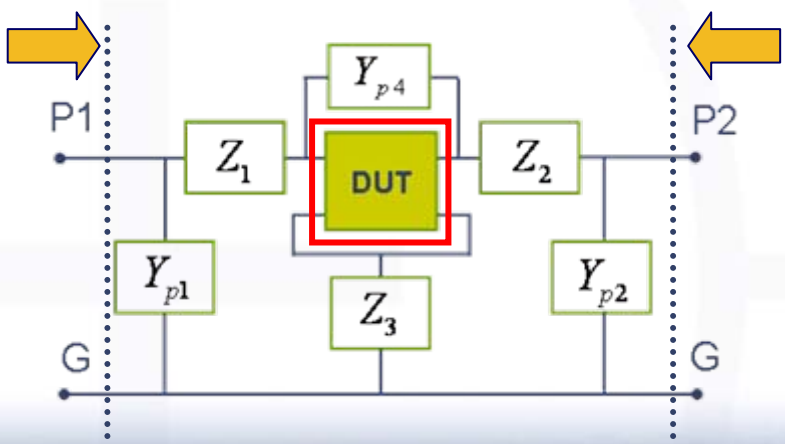


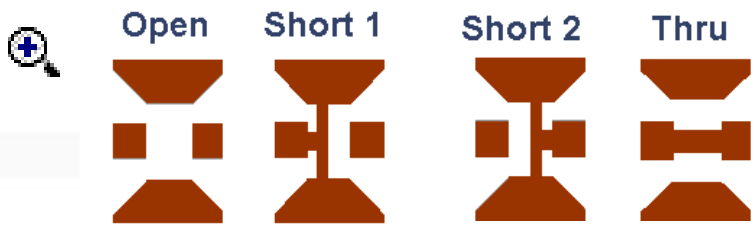
Reference plane at probe-tips after step 1

(off-wafer calibration)

Standard Technique

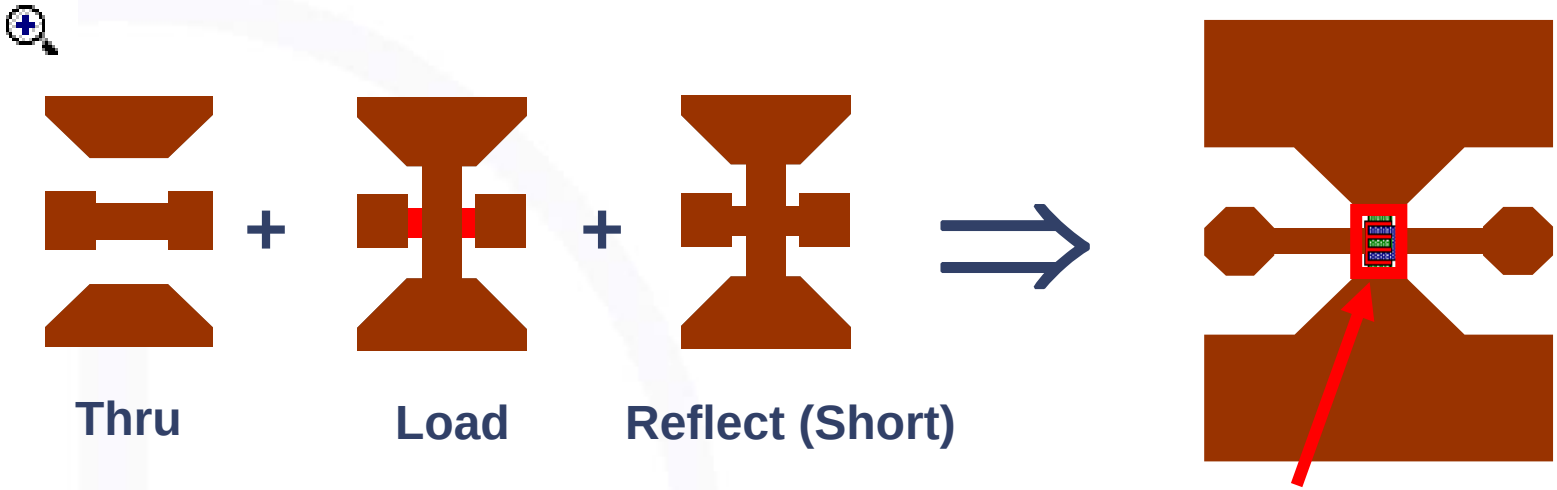
- Why de-embedding fails
  - Based on the impedance equivalent model of pads and interconnects
  - Assumes that a dummy pad represents (a part of) the parasitic impedance
  - Subtracts impedances
- Frequency ↑ → accuracy ↓





On-Wafer Calibration

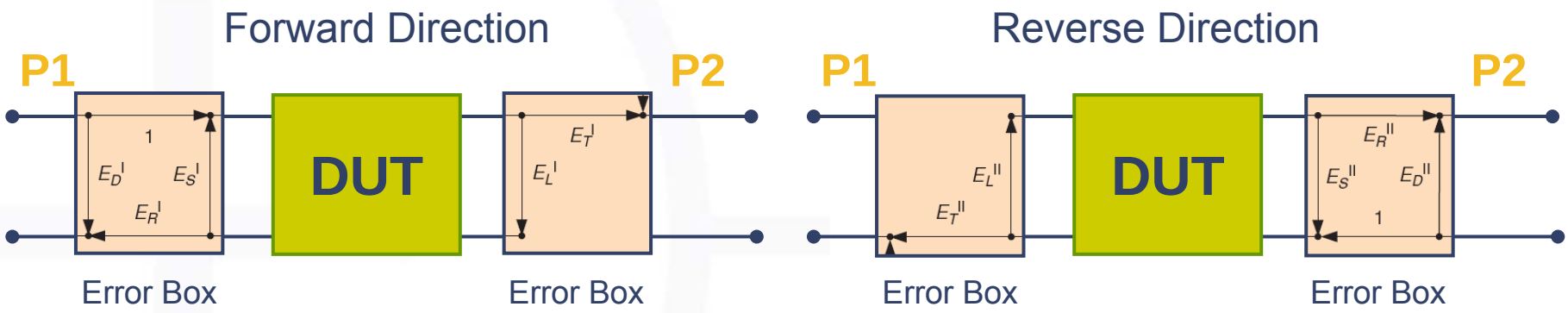
- One step approach
- Example: LRM+ calibration with wafer embedded standards



Measurement reference plane after the on-wafer calibration

On-Wafer Calibration

- Why calibration works
  - Applies the measurement theory: the concept of systematic measurement errors
  - Uses (partly) known standards to define error terms
  - Determines DUT parameters over the error correction procedure
- No frequency limitation



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Suitable Calibration Methods

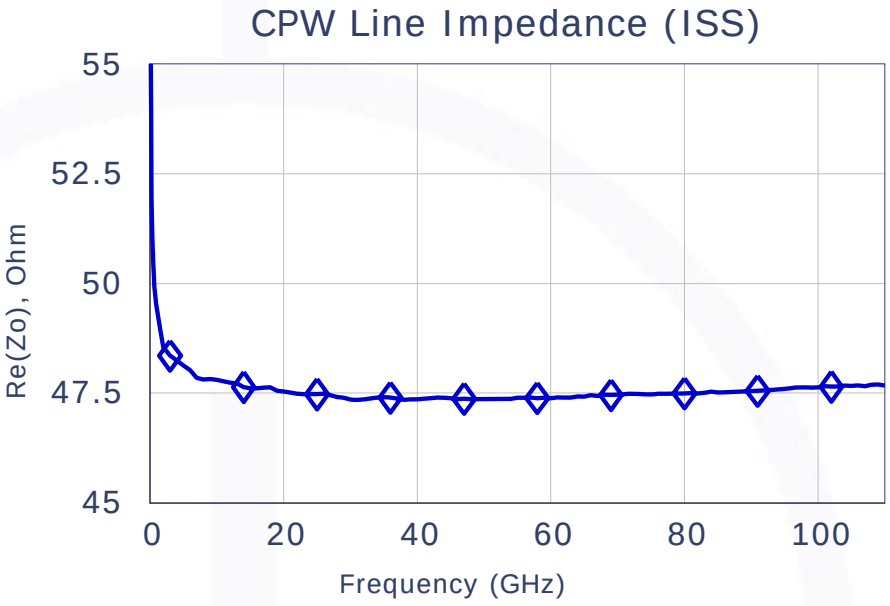
- Multiline TRL:
  - Developed at NIST in early 90s [1]
  - Original application: semi-insulating wafers (GaAs) [2]
  - End of 90s: application techniques for Si [3]
- LRM+:
  - First application: SiGe:C [4]
  - Comparison vs. multiline TRL: GaAs [5], bulk Si [6]

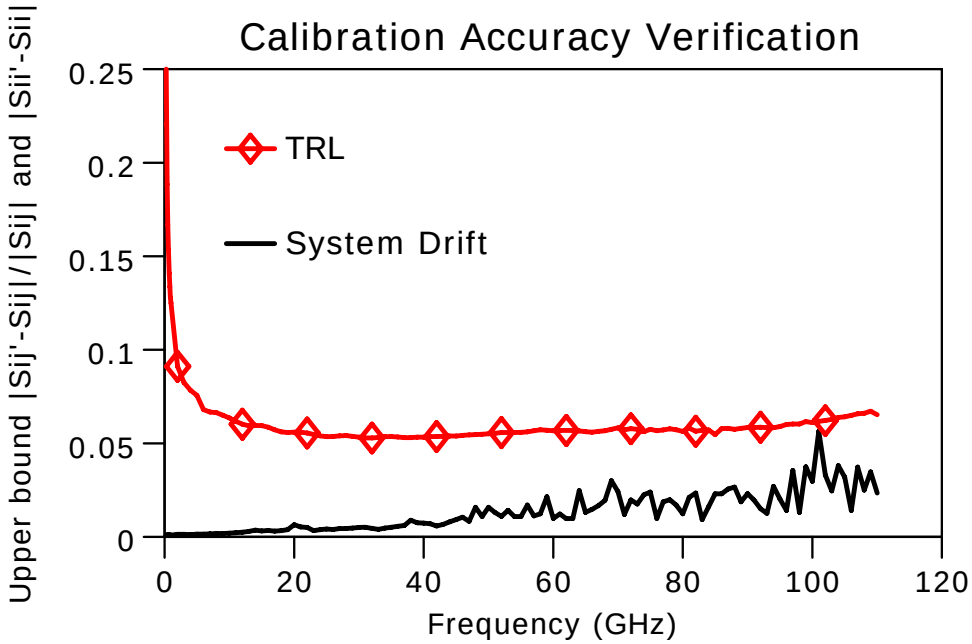
On-Wafer TRL/ NIST Multiline TRL

- Advantages
  - Fundamental calibration
  - Does not require ideal Open or Short
  - Measures line propagation constant
  - Self-consistent
- Challenges
  - Many lines are required for broadband measurements
  - Reference impedance is the line Z_0
  - Measurement of the line Z_0 on lossy substrates

On-Wafer TRL: Residual Calibration Errors

- Alumina CPW TRL (4 Lines) with respect to the 50 Ohm calibration [7]





Methods to characterize the line → accuracy improvement (NIST approaches), e.g. [3]

On-Wafer LRM+

- Advantages
  - Not sensitive to Load asymmetry
  - Arbitrary impedance elements can be used as Loads
  - Does not require known Open or Short
  - Self-consistent
- Challenges
  - Requires known Loads and Thru

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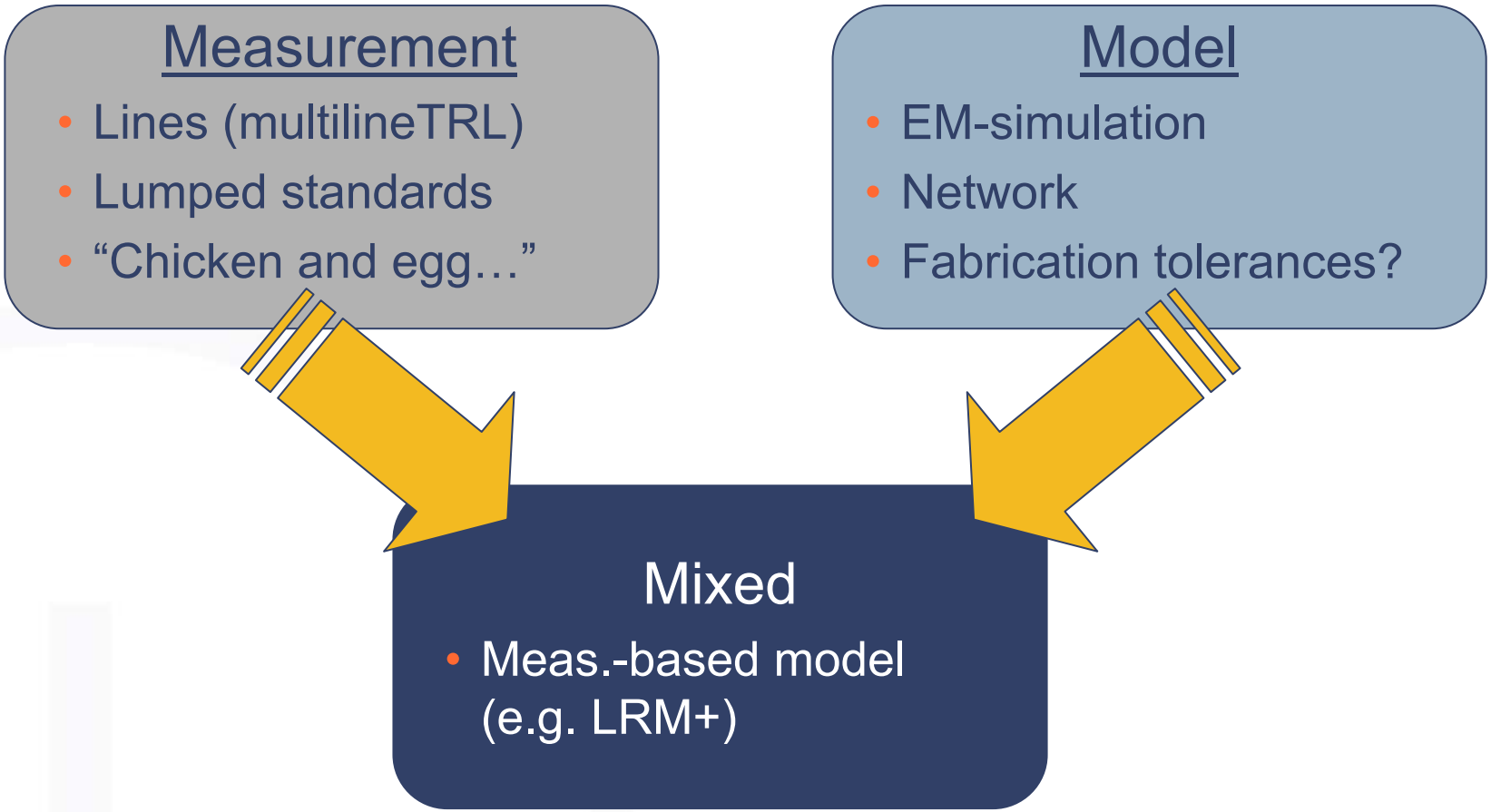
Characterization of Customized Standards



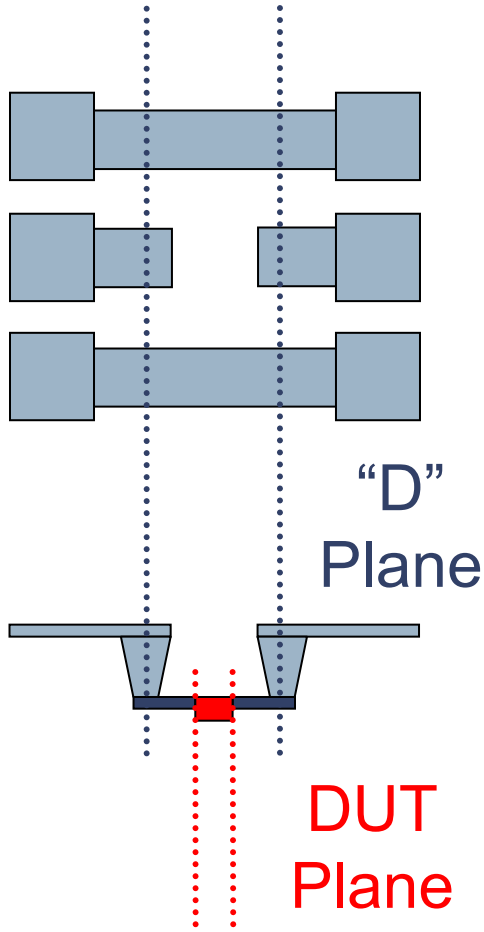
Mixed approach addresses fabrication tolerances

Implementation Challenges

- High loss of silicon substrate:
  - Difficulties in implementing TRL calibration
- Many metal layers:
  - Difficulties in 3D EM simulation of on-wafer standards
- High fabrication tolerances:
  - Inaccurate lumped (open, short and load) and distributed (thru and line) standards
- High price of wafer space

Design of Standards

- GSG pad set
- Ground and signal pads are at the high-level metal
- Lines: high-level metal
- Load, short, and open are at the bottom of the via stacks, at the plane “D”
- Special methods to improve electrical properties of the line



Characterization of Standards: Simulation

- EM simulation technique:
  - Not practical for the complete structures
- Simplified representation:
  - A line with a solid, reference conductor, and a single dielectric (addressing physical dimensions)
- Simulated model of the load standard

Characterization of Standards: Measurements

- Measurement technique:
  - γ of the line from the NIST Multiline TRL
  - Z_0 of the line: from the load method
- Load impedance:
  - From the reference NIST multiline TRL
  - From the 'Mixed Technique'
    - Z → modeled
    - R^* → measured
    - Z^* → reconstructed [4]

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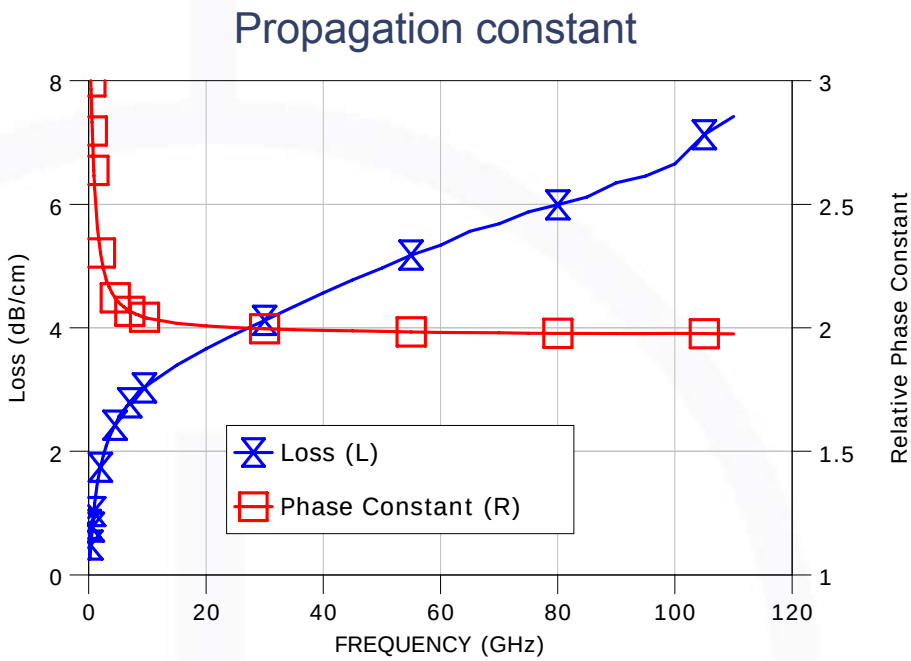
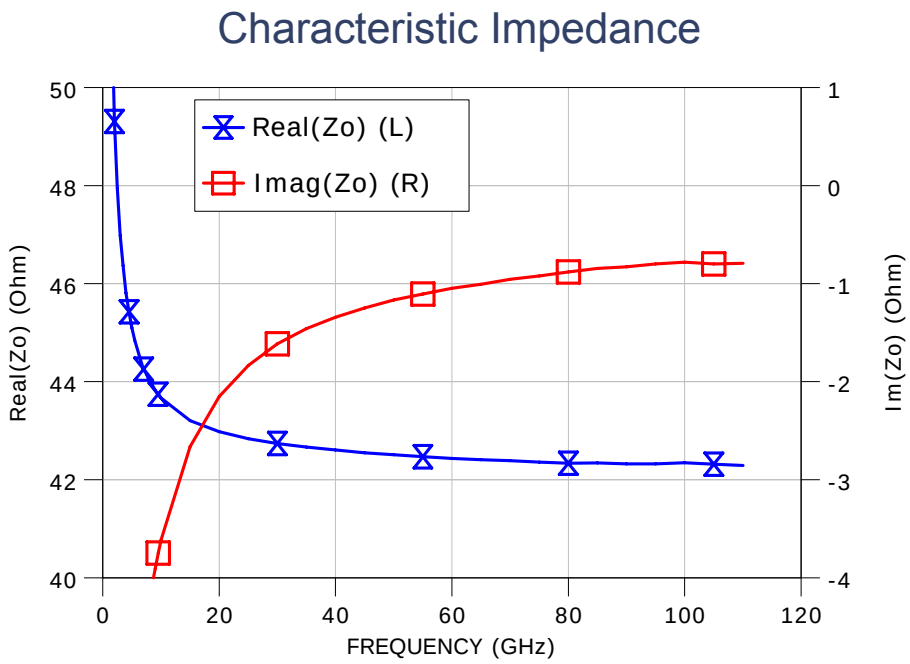
Characterization of Standards

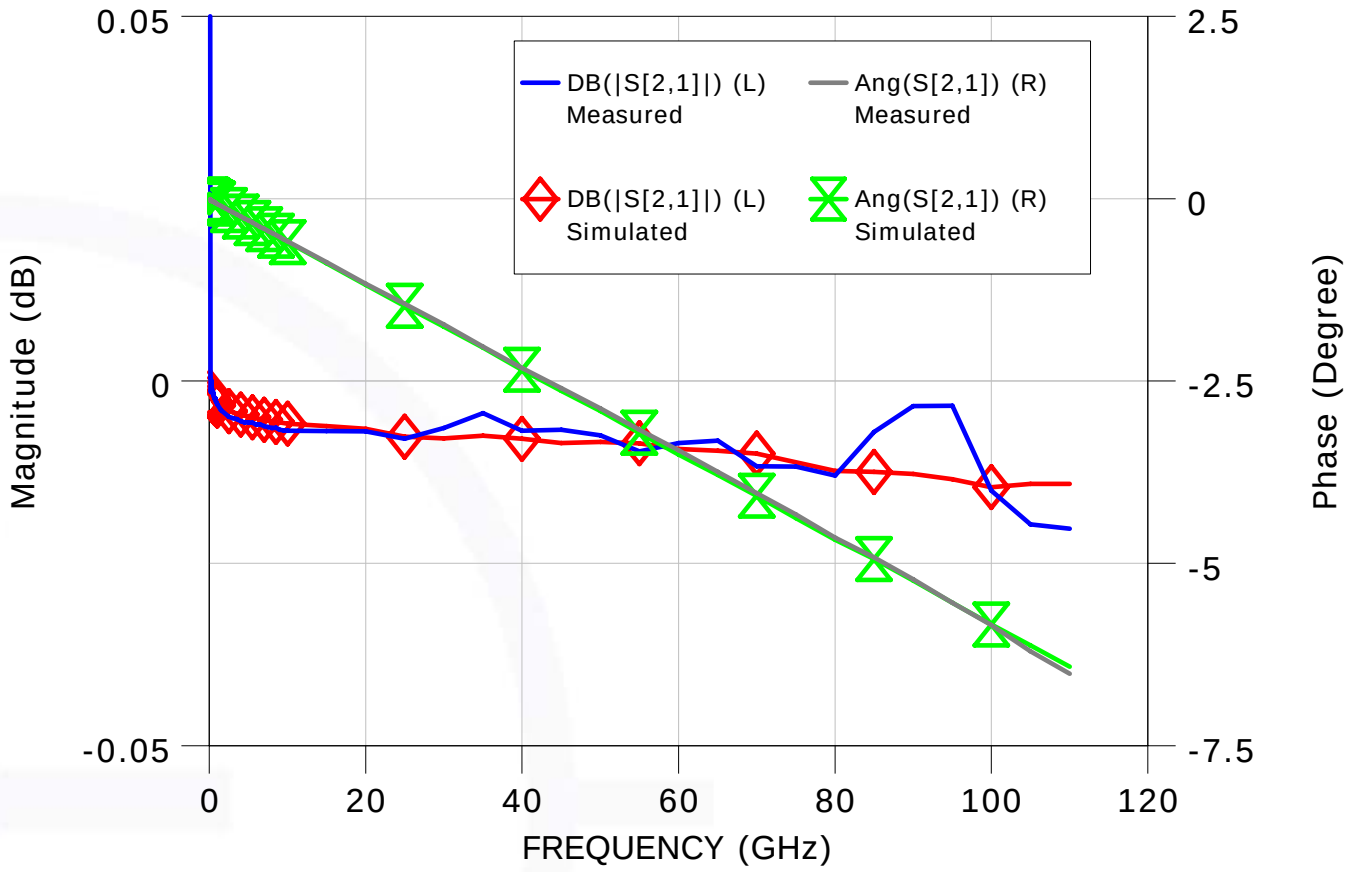
- Line parameters, extracted from multiline TRL [6]





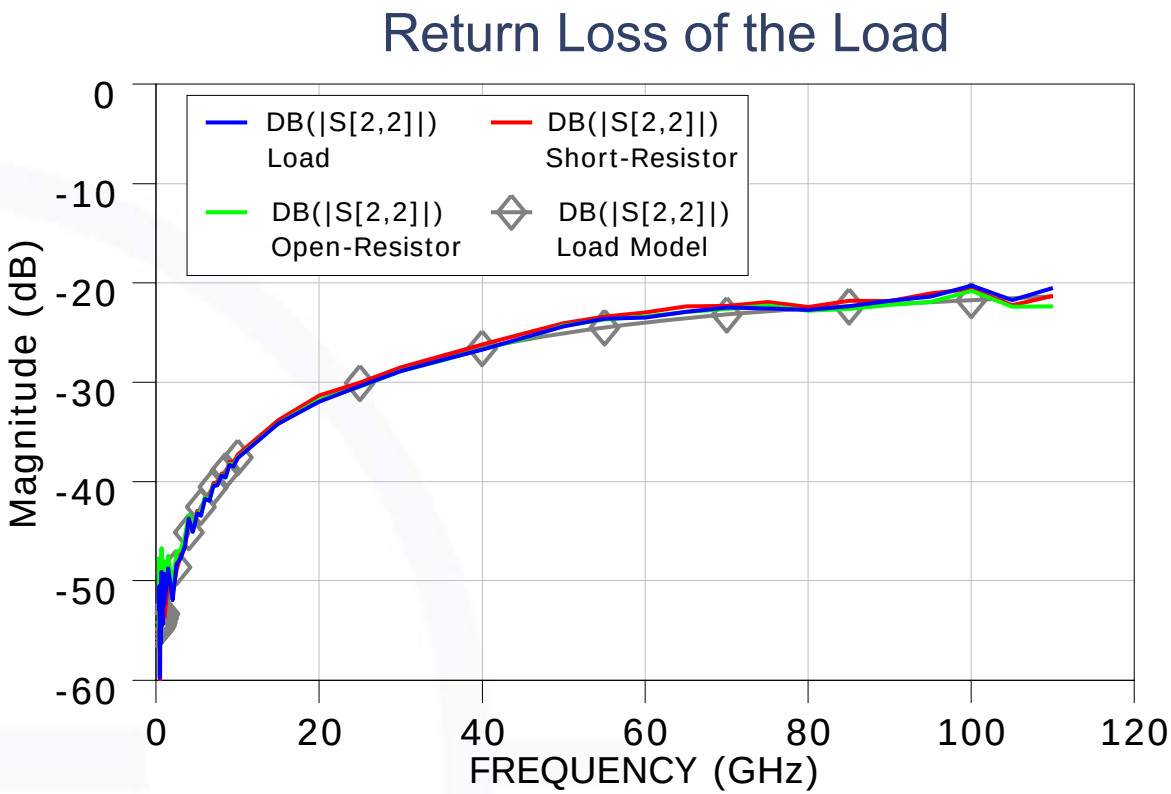
Characterization of Standards

- Thru: measurement vs. simplified simulation [6]



Characterization of Standards

- Load standard: fabrication tolerances within one test chip (mixed model vs. measurement) [6]



Mixed model agrees with measurement results

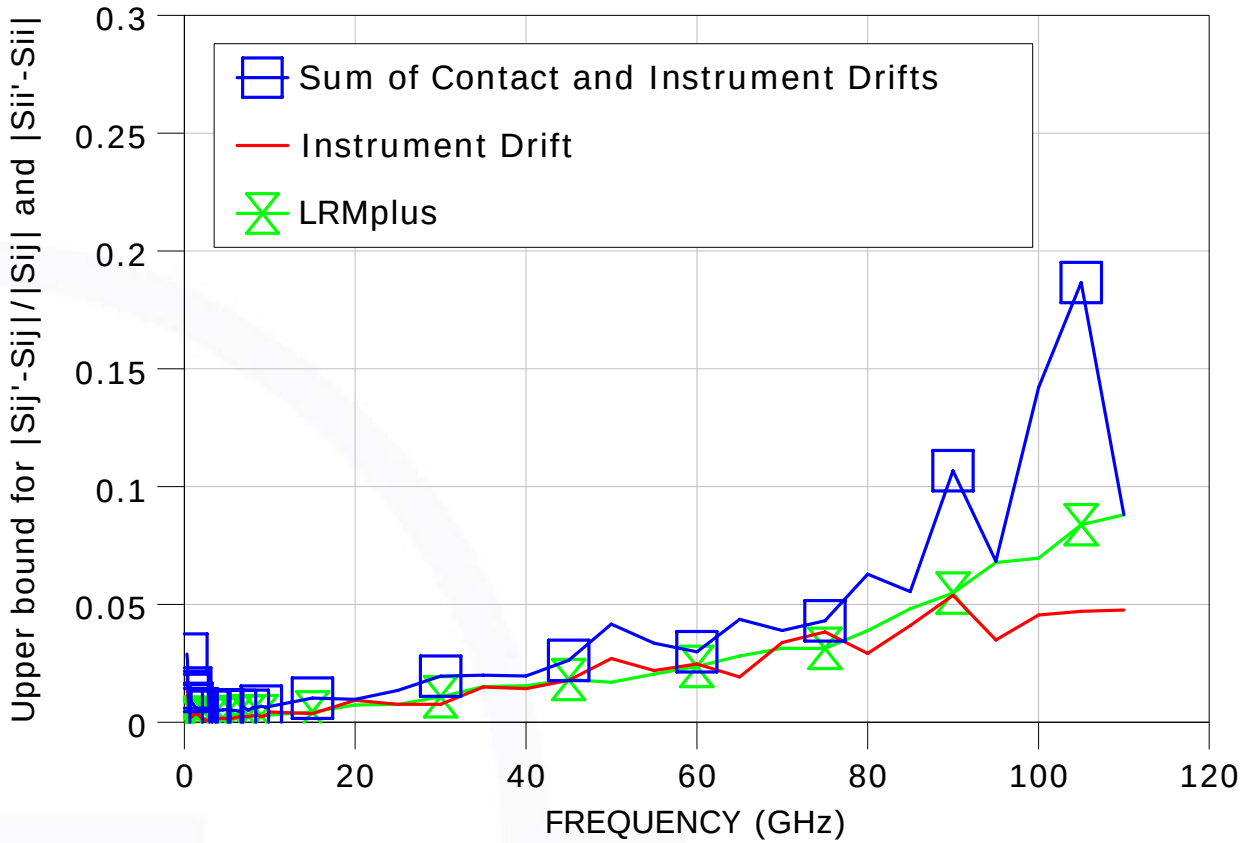
Calibration Accuracy Comparison: NIST Method

- Calibration comparison technique for:
  - Contact repeatability (on Si)
  - Instrument drift*
  - LRM+ accuracy
- Reference calibration:
  - NIST Multiline TRL

* Experimental time: 8 hours

Calibration Accuracy Comparison: NIST Method

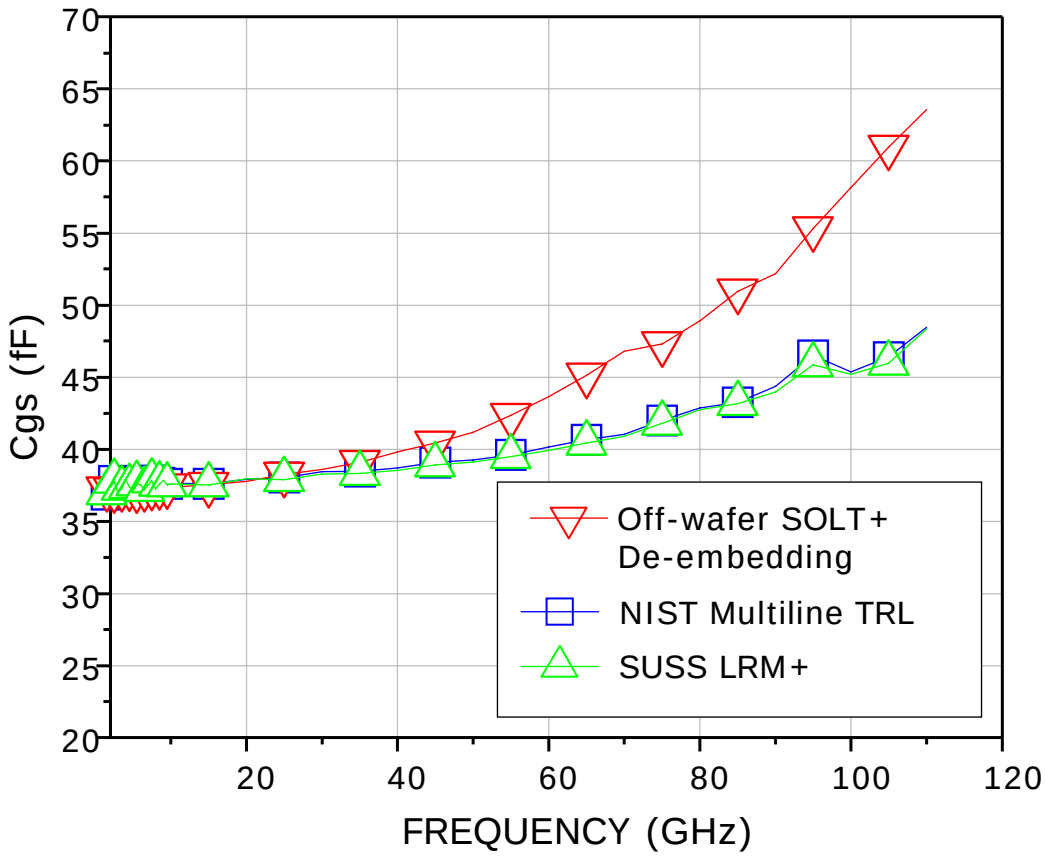
+ LRM+ vs. Multiline TRL [6]



LRM+ is in agreement with the reference multiline TRL

Calibration Accuracy Comparison: DUT

- Verification for FET: advanced 0.13 µm RF-CMOS NFET, [6]



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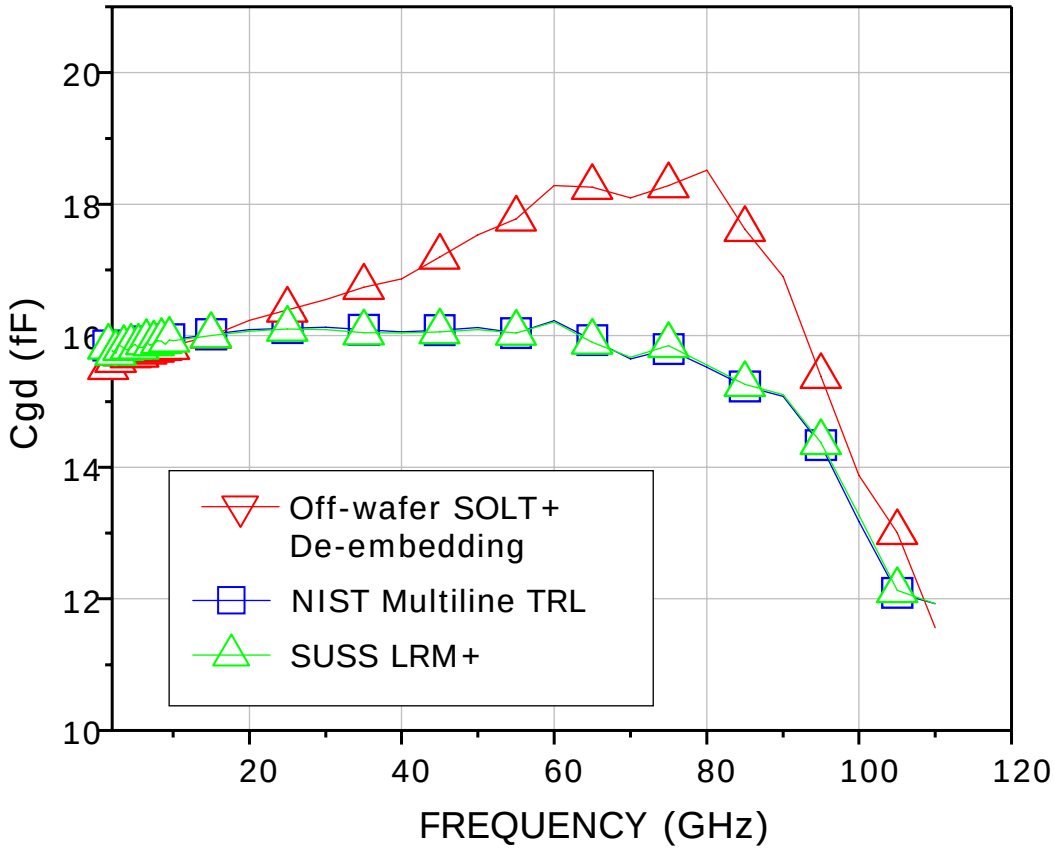

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- Improved design of standards and a consistent reference plane increased on-wafer calibration accuracy
- Simplified 3D EM simulation of standards demonstrated good results
- Wafer-embedded NIST Multiline TRL and LRM+ significantly improve measurement accuracy at mm-wave frequencies

Conclusion

- LRM+ and NIST Multiline (with 3 lines) are comparable for measurement accuracy
- LRM+ is more practical for implementation:
  - Requires fewer standards: 3 vs. 5
  - Saves test chip size by a factor of ~14x
  - Twice as fast: 10 sweeps vs. 20 sweeps
- LRM+ does not require motorized positioners (or operator):
  - Cheaper and faster

Acknowledgement

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References

[1] R. B. Marks, "A multiline method of network analyzer calibration," Microwave Theory and Techniques, IEEE Transactions on, vol. 39, pp. 1205-1215, 1991.

[2] D. Williams, R. Marks, K. Phillips, and T. Miers, "Progress toward MMIC on-wafer standards," in ARFTG Microwave Measurements Conference-Fall, 36th, 1990, pp. 73-83.

[3] D. F. Williams, U. Arz, and H. Grabinski, "Accurate Characteristic Impedance Measurement on Silicon," in ARFTG Conference Digest-Spring, 51st, 1998, pp. 155-158.

[4] R. F. Scholz, F. Korndorfer, B. Senapati, and A. Rumiantsev, "Advanced technique for broadband on-wafer RF device characterization," in ARFTG Microwave Measurements Conference-Spring, 63rd, 2004, pp. 83-90.

[5] R. Doerner and A. Rumiantsev, "Verification of the wafer-level LRM+ calibration technique for GaAs applications up to 110 GHz," in ARFTG Microwave Measurements Conference-Spring, 65th, 2005, pp. 15-19.

[6] A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," ARFTG Microwave Measurements Conference-Fall, 72nd, pp. 132-135, 2008.

[7] A. Rumiantsev, "A review of VNA calibration methods," in European Microwave Conference, 38th. Workshop WMO-3, Determining and Dealing with Errors in Microwave Measurements, 2008.