Semiconductor Device Compact Modelling with Ageing Effects

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UNIVERSITY OF LEEDS

Motivation

- Transistors getting smaller
  - again

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- Transistors getting smaller
- Ageing effects
  - permanent (HCI)
  - temporary (BTI)

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- Transistors getting smaller
- Ageing effects
- Analogue case hardly covered
  - Digital case well understood
  - How does that help?

Motivation

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- Ageing simulation questionable
  - Vendor specific, blackbox based
  - Limited flexibility

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- No compact modelling standard
  - Hard to create models
  - On any hierarchy level

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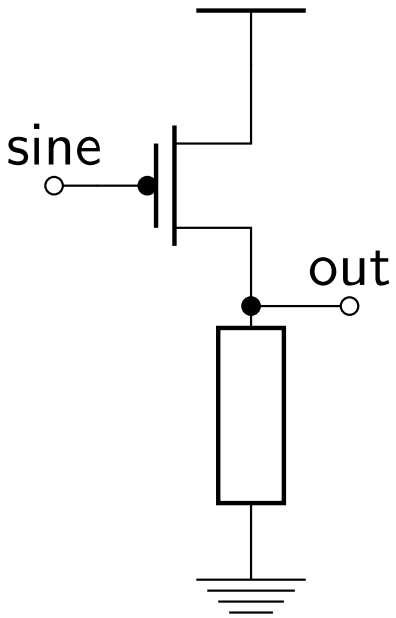
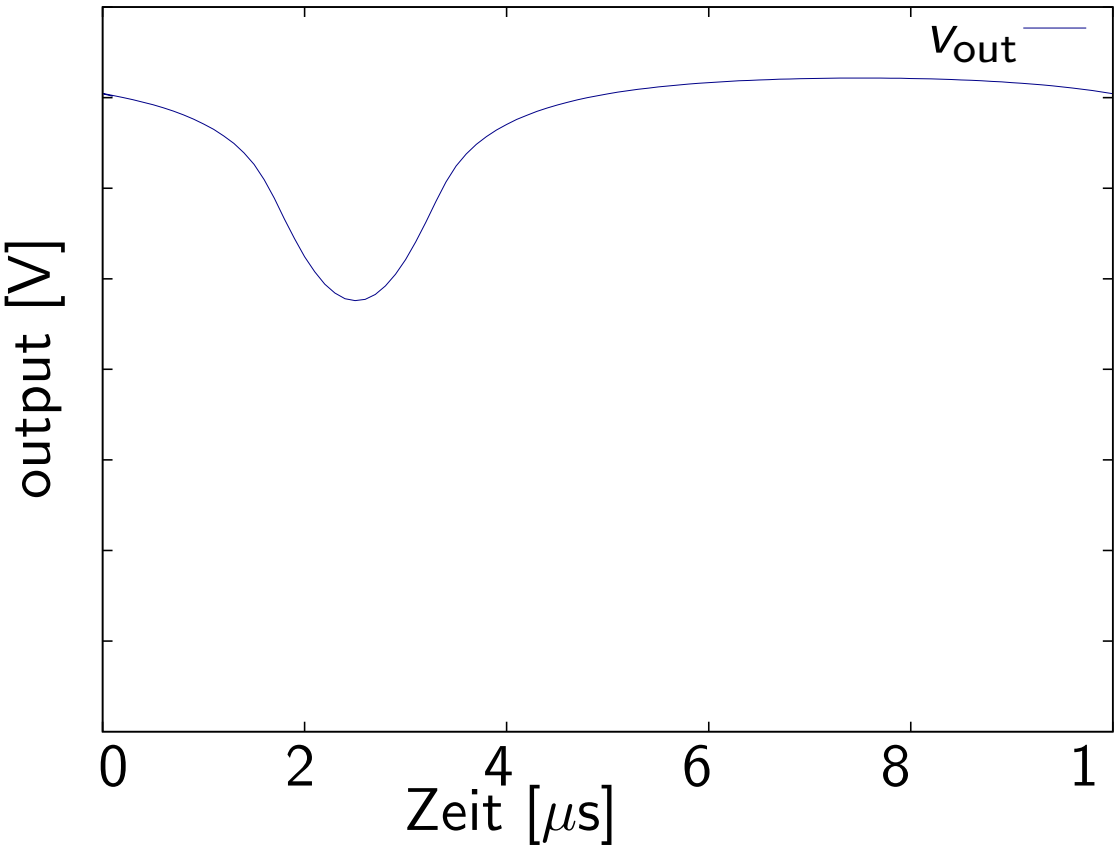
A Transistor





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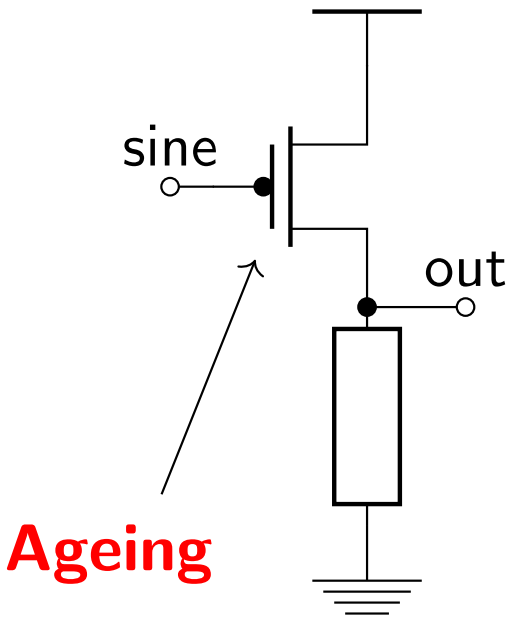

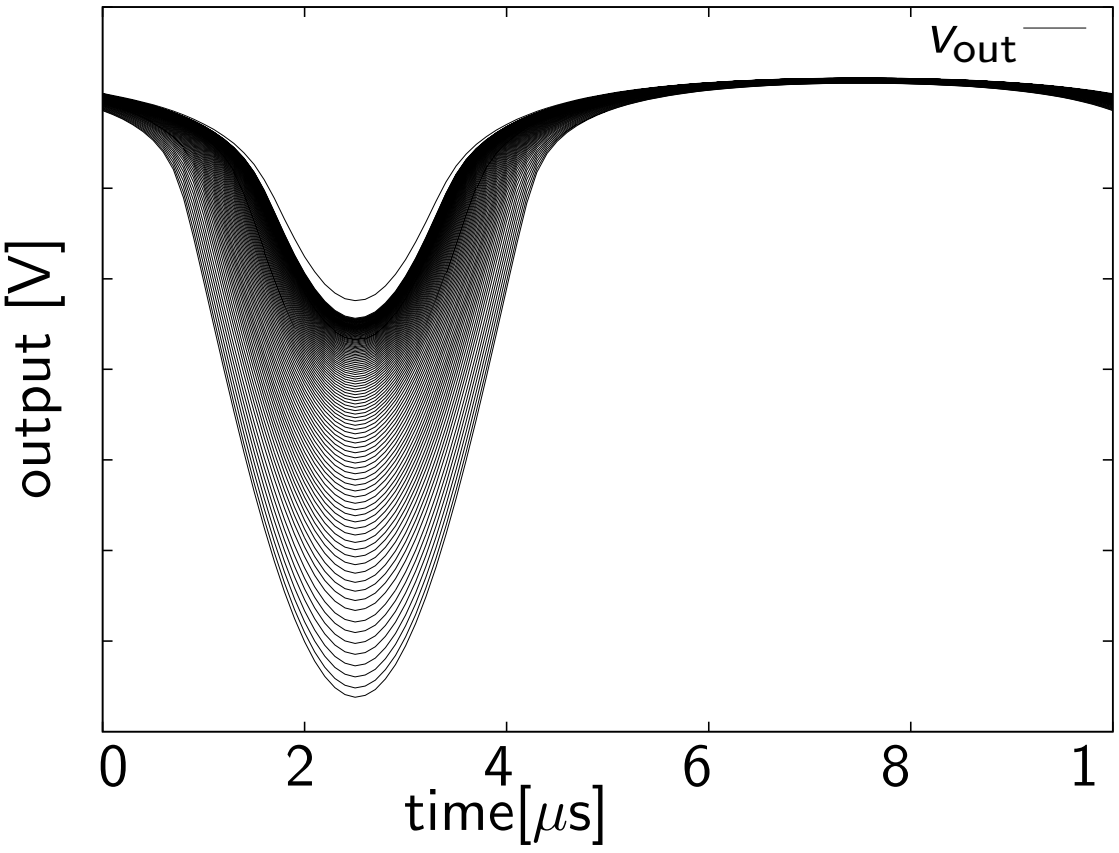

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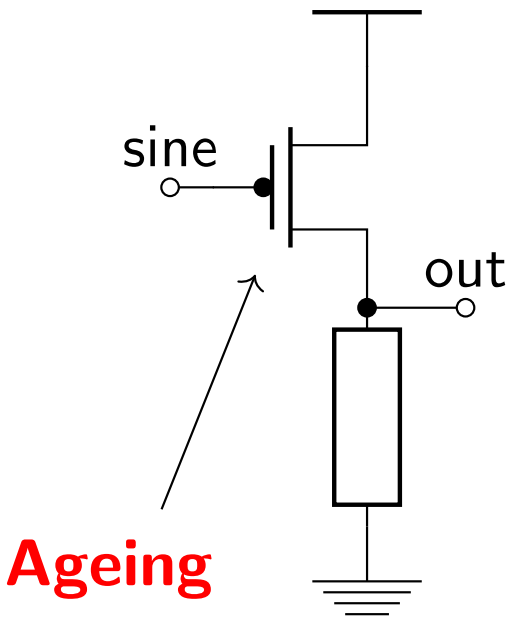

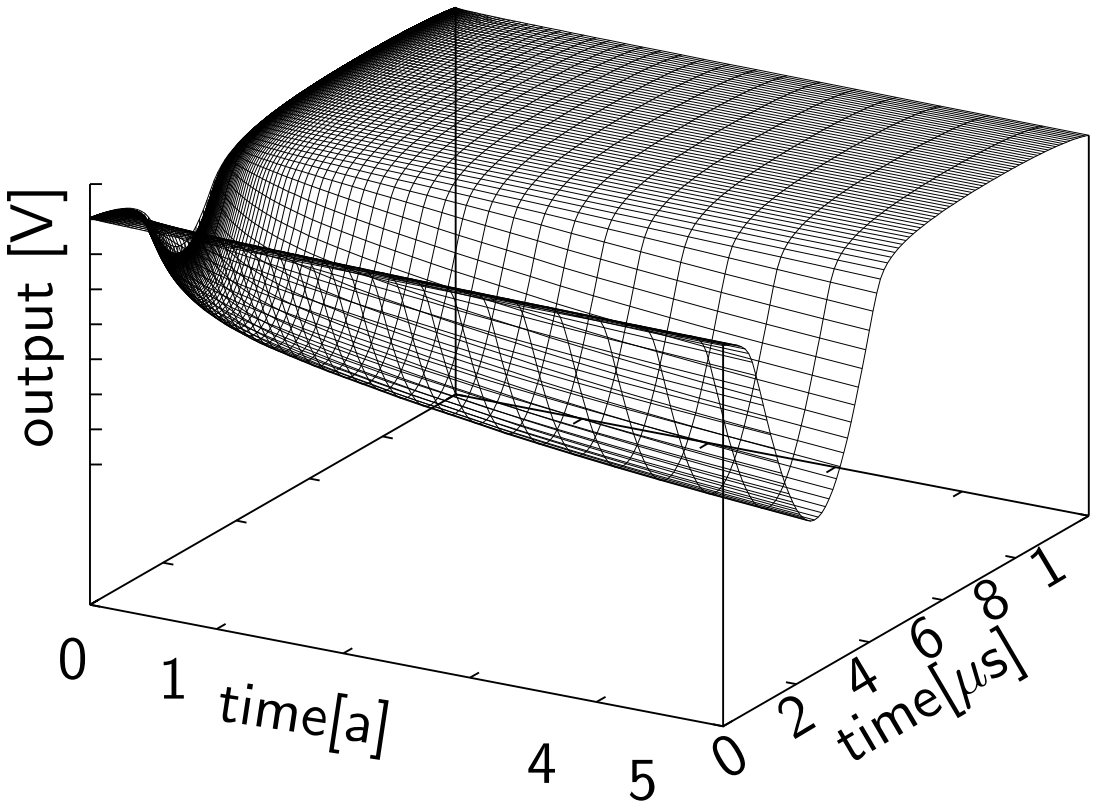

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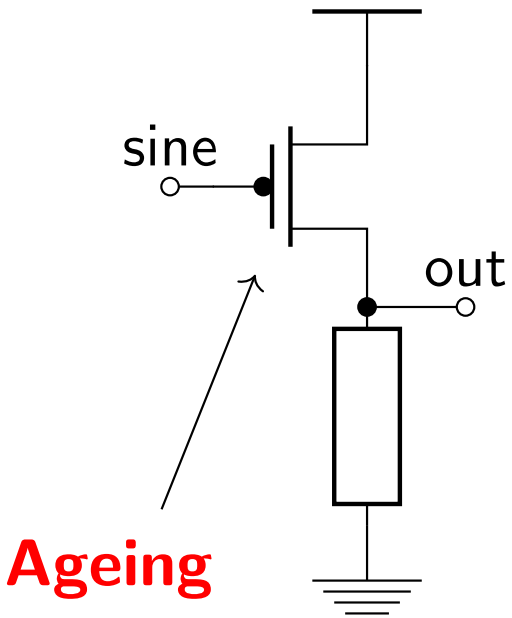

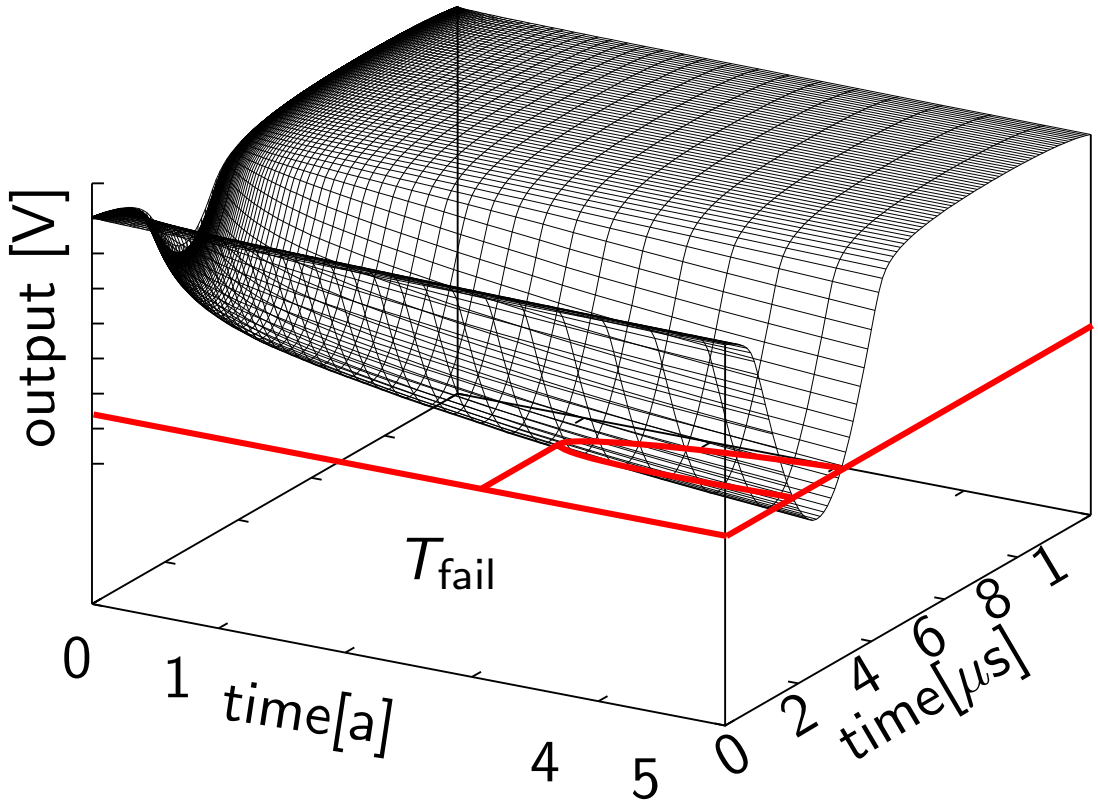

Ingredients

- Material Constitution Model
  - Stress levels
  - Ageing processes

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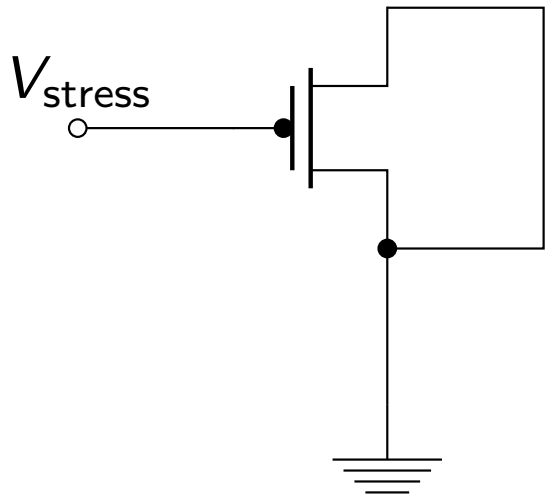
  - ... and workaround
- Simulation
  - Different time scales
  - Efficient model evaluation
- Implementation
  - gnucap-uf (ageing simulation)
  - gnucap-adms (model compiler)

BTI Measurements

- Stress phase



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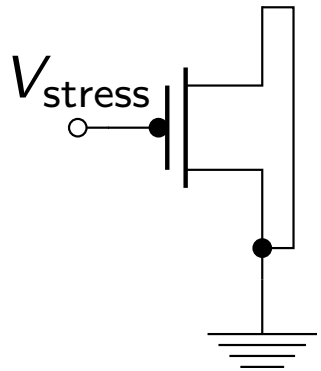
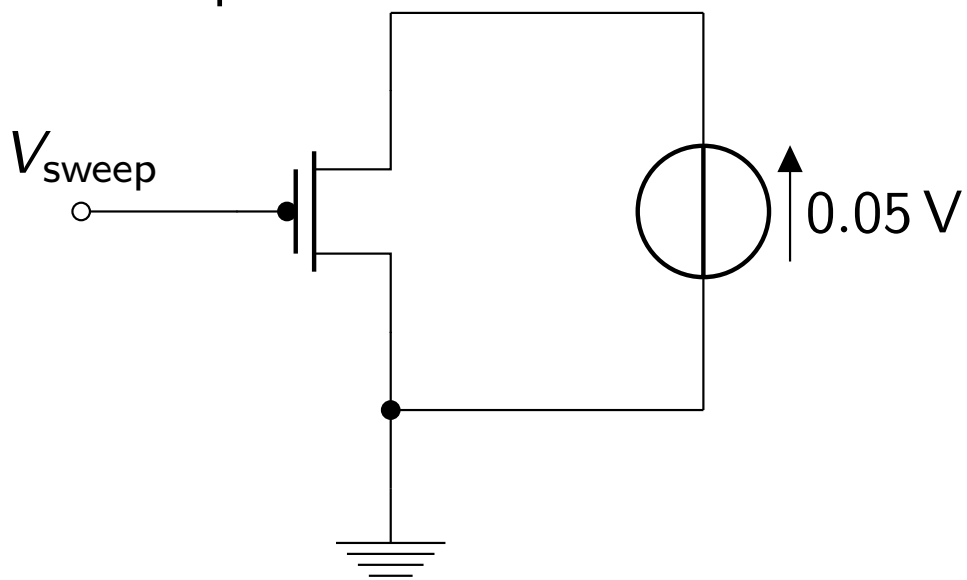


- Measure phase



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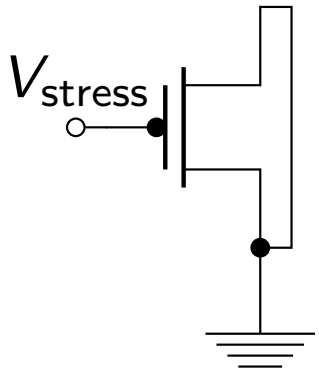

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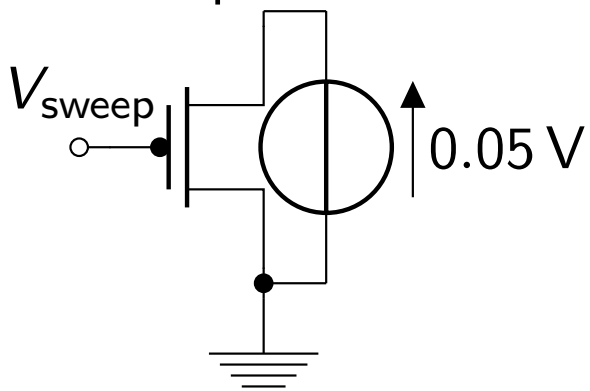

- $\Delta V_{\text{th}} \sim$ trap density

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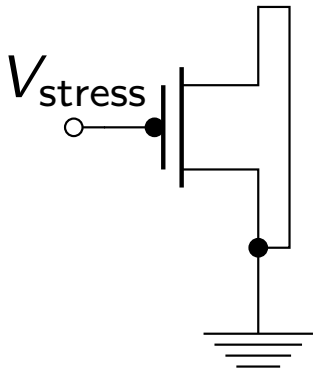

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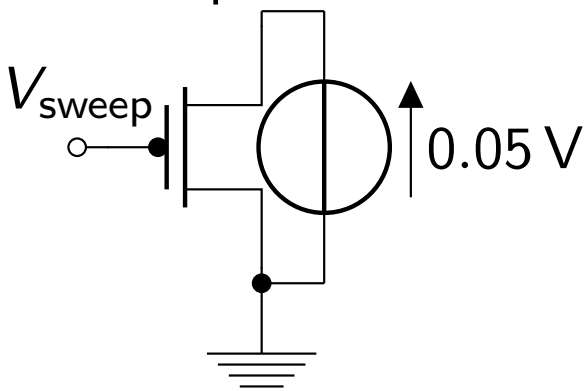
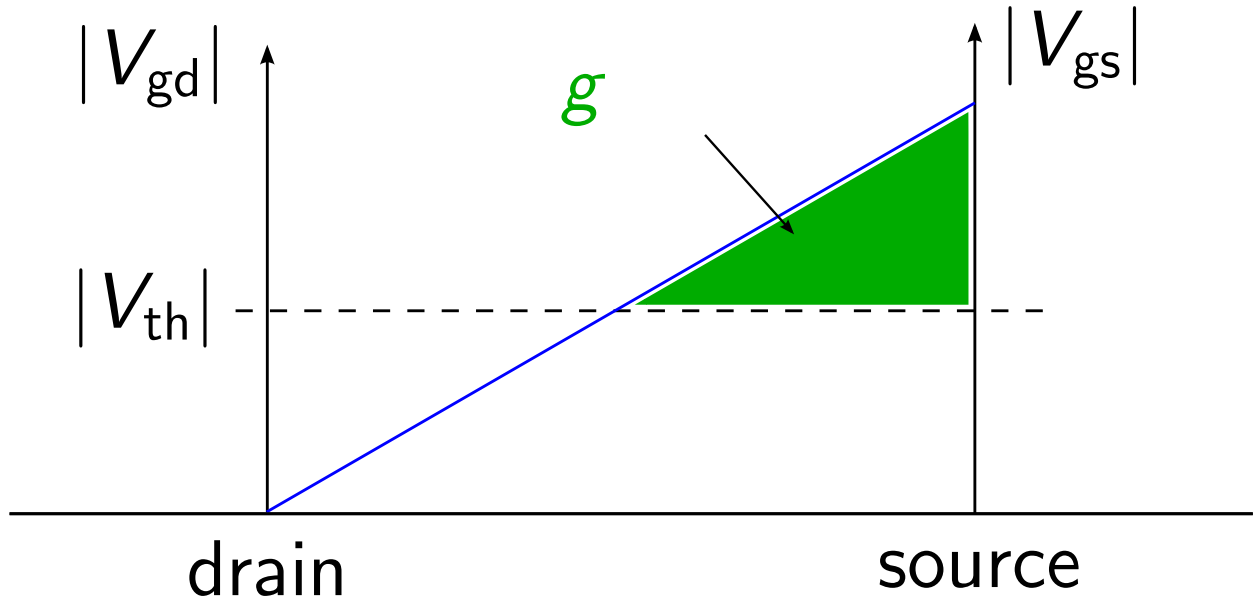


- $\Delta V_{\text{th}} \sim$ trap density
- Not as meaningful in analogue circuits.

Dissecting a Transistor Model

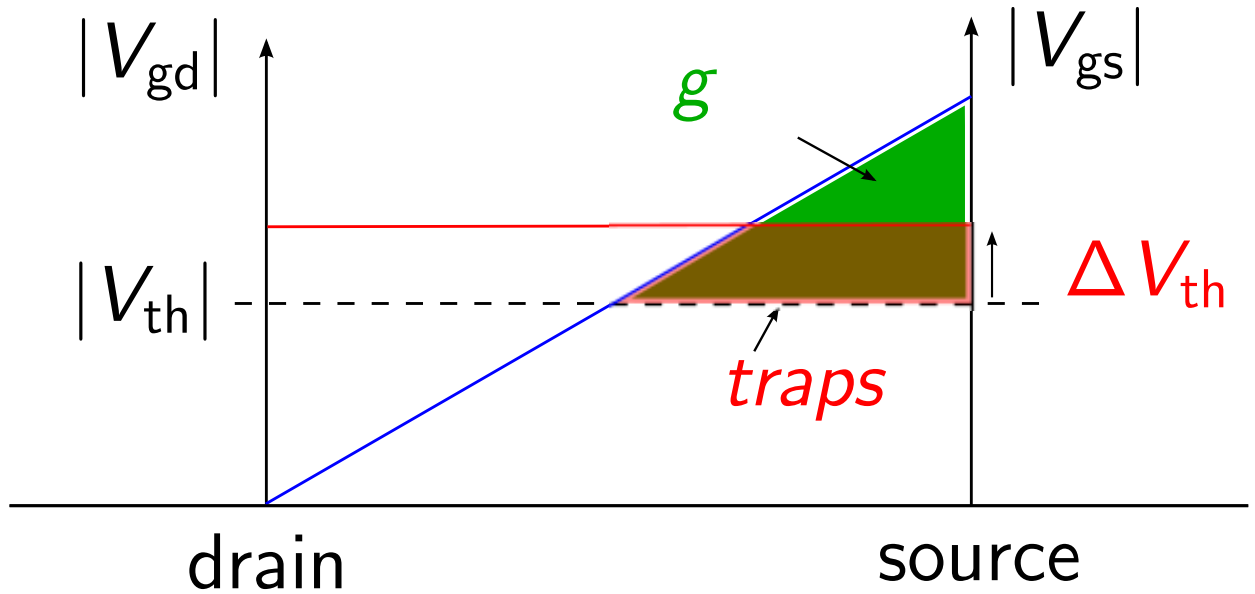
- $|I_{ds}| = K \cdot |V_{gs} - V_{th}|^2$



- $I_{ds} \sim g \cdot V_{ds}$

Threshold voltage change, conventional model

- $|I_{ds}| = K \cdot |V_{gs} - V_{th} - \Delta V_{th}|^2$



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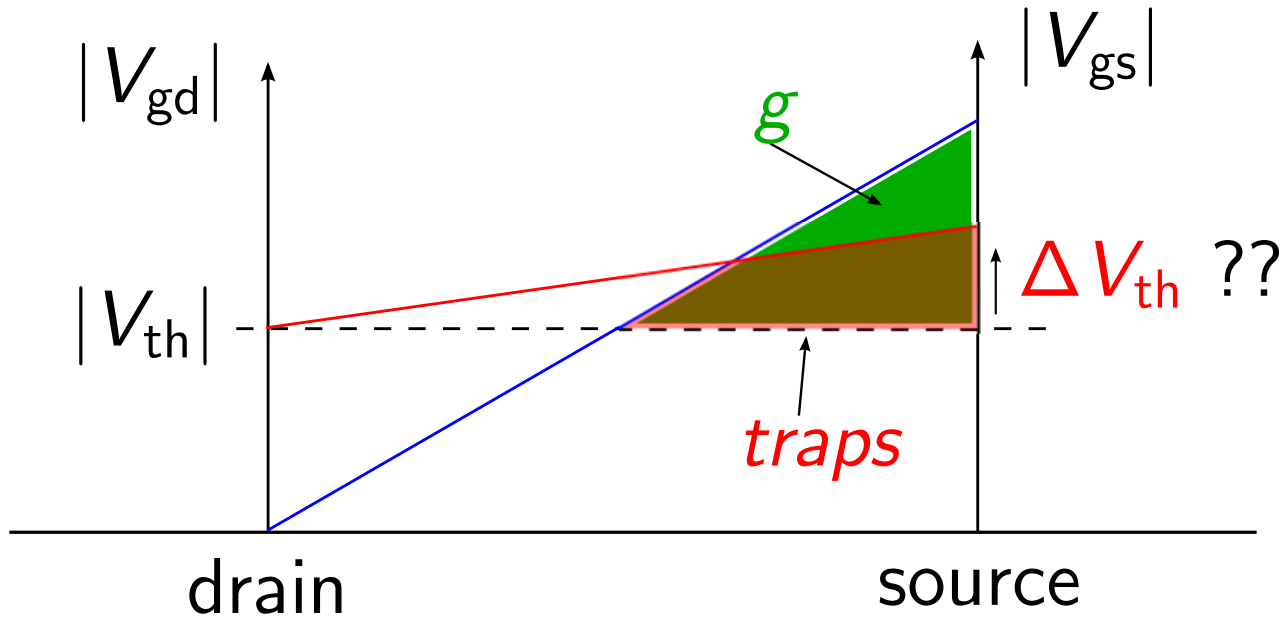
Threshold voltage, the analogue case



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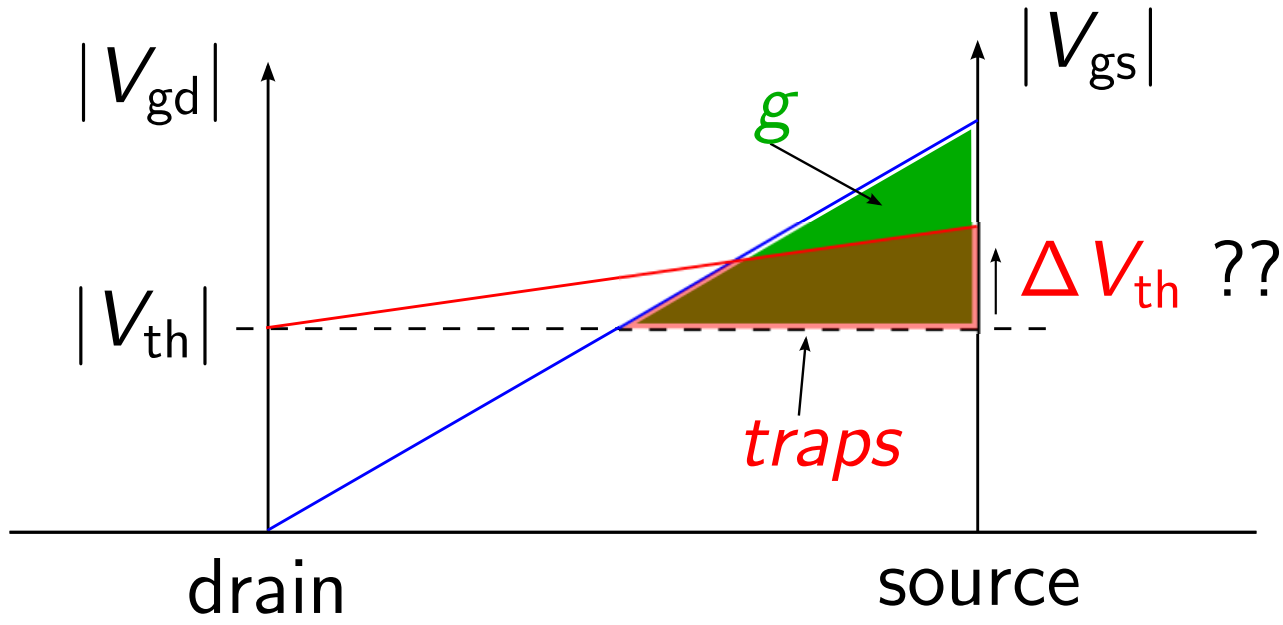
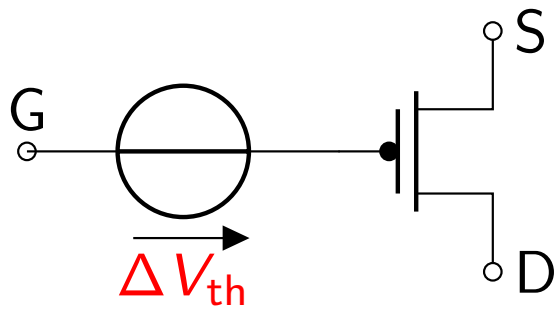


- $|I_{ds}| \sim g_{remain} \cdot |V_{ds}|$
- $\ldots \neq K \cdot |V_{gs} - V_{th} - \Delta V_{th}|^2$

Conventional Block Based Model

```
.model pfet_aged [..] vt=vt0+dvth
```



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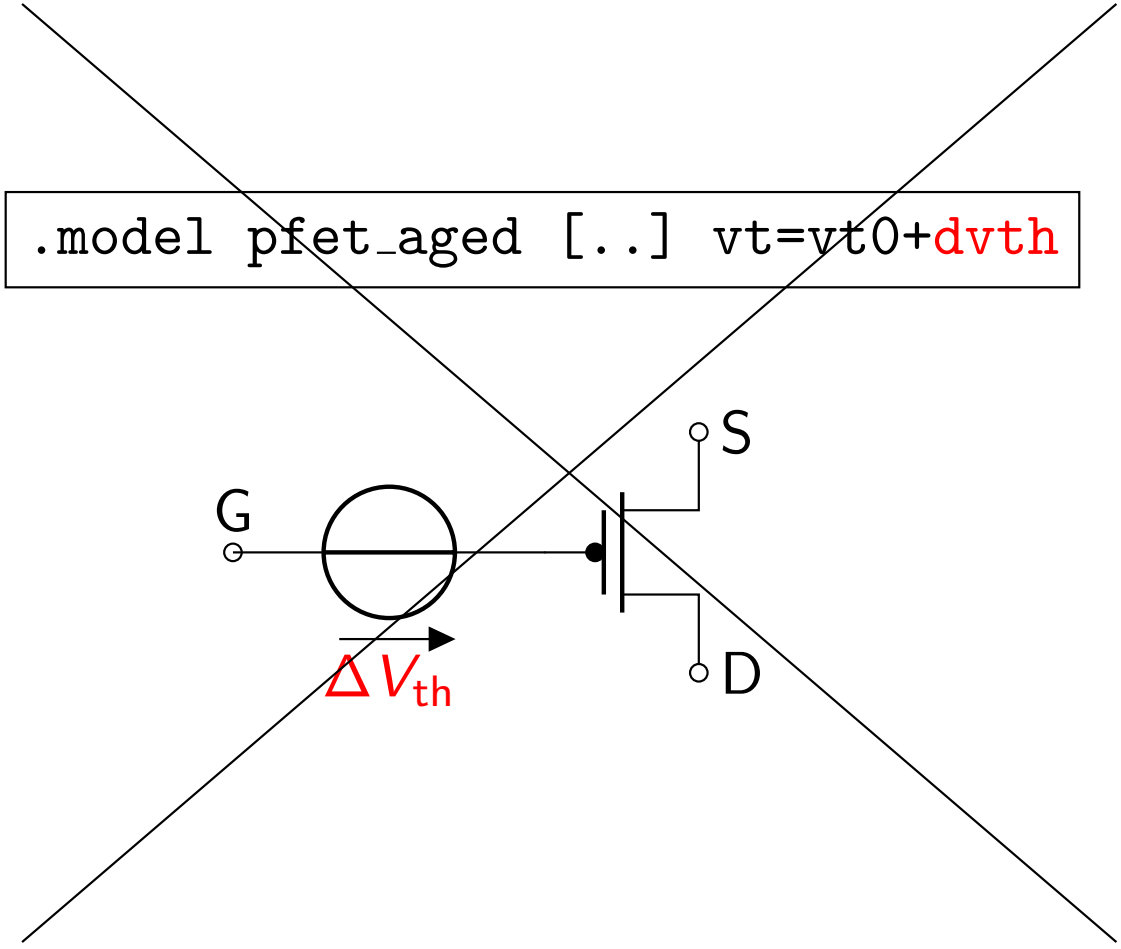

Ageing Processes

- Map stress wave $L\colon [0, t] \to \mathbb{R}$ to ageing state.
- arithmetically simple (ideally).

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$$L \mapsto \int L \mathrm{d}t$$

Ageing Processes

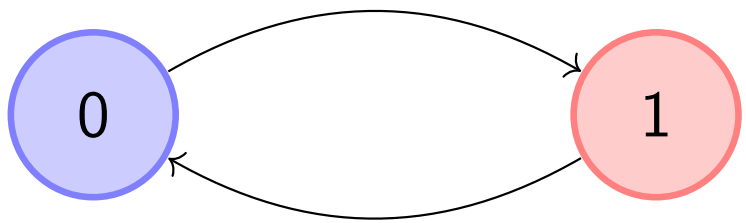
- Map stress wave $L\colon [0, t] \to \mathbb{R}$ to ageing state.
- arithmetically simple (ideally).
- Integrator
- Controlled decay process

$$L \mapsto \exp\left(-\int 1/\tau(L(t))\mathrm{d}t\right)$$

Ageing Processes

- Map stress wave $L\colon [0, t] \to \mathbb{R}$ to ageing state.
- arithmetically simple (ideally).
- Integrator
- Controlled decay process
- Reversely Coupled Decay (RCD) process

$$\tau_c(L) = \exp(k_c - m_c L)$$



$$\tau_e(L) = \exp(k_e + m_e L)$$

Process Based Ageing Effect Model

- In Verilog-A
  - additional discipline
  - no language extension required
  - .. but extra semantics
  - transport stress and ageing states

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- Declaration

```
discipline degradational
  potential Damage;
  flow Stress;
enddiscipline
nature Damage
  units = "1";
  access = State;
endnature
nature Stress
  units = "1";
  access = Level;
endnature
```

Process Based Ageing Effect Model

- In Verilog-A
- Declaration

```
discipline degradational [..]
```

- BTI Subdevice

```
module bti_traps(p, n, d);
    electrical p, n;        // electrical field
    degradational d;        // defect density
    degradational n1, n1;
    rcd_exp #([..]) rcd1 (p, n, n1);
    rcd_exp #([..]) rcd2 (p, n, n2);
    analog begin
        @ ( initial_step ) begin
            State(d) <+ 0; // fresh.
        end
        State(d) <+ w1*State(n1) + w2*State(n2);
    end
endmodule
```

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- Parameters: machine learning.

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    [..]
endmodule
```

- Parameters: machine learning.
- Processes: implemented in/for gnucap-uf

Full Transistor Model

```
module ageing_mosfet(d, g, s, b);
   electrical d, g, s, b;
   electrical ch;                  // channel mid
   degradational a1, a2, a3; // 3 ageing nodes
   bti_traps bti0(s, g, a1);
   bti_traps bti1(ch,g, a2);
   bti_traps bti2(d, g, a3);
   [..]
   analog begin
      Level(a1) <+ V(g,s);
      Level(a2) <+ V(g,ch);
      Level(a3) <+ V(g,d);

      // channel segmentation
      green = f(V(d), V(g), V(s), V(b)
                        State(a1), State(a2), State(a3));

      I(d,s) += green * V(d,s);
   end
endmodule
```

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```
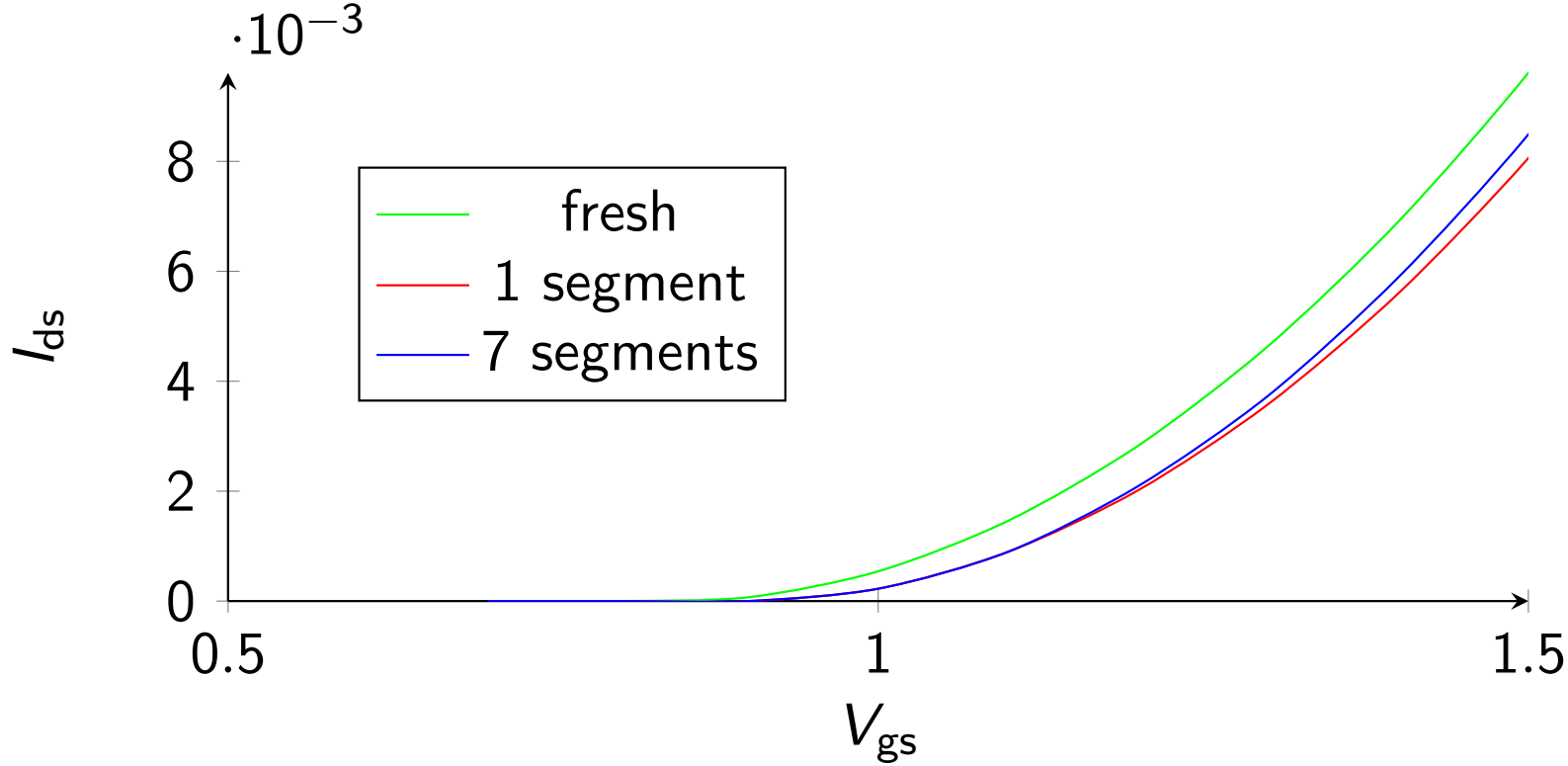

Numerical Result

- Run inverter circuit on sine wave
- Compute I_{ds}/V_{gs} dc-characteristic



- Same ΔV_{th}, still different

Thank You.