Performance Modeling, Parameter Extraction Technique and Statistical Modeling of Nano-scale MOSFET for VLSI Circuit Simulation

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Outline

- Nano-scale bulk MOSFET
  - Major Sources of Intra-die process variability
  - Statistical Simulation through HSPICE
  - RDD Reduction through channel engineering

- Double Gate MOSFET
  - Physics-based Flicker Noise Modeling
Introduction

- Device performance variability due to process variability significantly affects the robustness of an integrated circuit.
  - Among the major challenges to scaling and integration.

- Sources of Process variations
  - Global or inter-die variations.
  - Local or intra-die variations.

- Intra-die variability significant in nano-scale regime.
Limitations of Conventional IC Design Methodology

- Traditional worst case corner analysis suffers from important limitations
  - Correlations between the device parameters are ignored. Significant risk of over or under estimations of process variabilities and the effect on circuit performances.
  - Cannot account for local intra-die process variability.
- Monte Carlo analysis for the complete circuit is often too computationally expensive.
- Paradigm shift in design methodology
  - Statistical IC Design Methodology.
Major Sources of Intra-die variability

Kamsani Noor PhD Thesis: Univ. of Glasgow

Random Discrete Dopant Effect:
- Discreteness of dopant atoms in the channel.
- Statistical fluctuation of the number and position of dopant atoms in the channel.

Line Edge roughness:
- Caused by tolerances inherent to material and tools used in the lithographic process.
- Does not scale with device modeling. Typically ~5nm.

Oxide Thickness Variations
- In scaled MOSFET, tox is typically equivalent to few atomic layers.
- Si/SiO₂ and SiO₂/polySi interface roughness is of the order of 1-2 atomic layers.
Effects of Process Variabilities

- RDD causes variations of I-V characteristics of identical devices.
  - Variations in threshold voltage, off-current and on-current.

- OTV causes fluctuations of the voltage drop across the gate oxide thus causing threshold voltage variations.

- LER causes threshold voltage degradation and higher subthreshold current.
- LER and RDD are statistically independent.
Statistical Simulation Techniques

- Atomistic Simulation: (GARAND: Gold Standard Simulations Ltd)
  - Drift diffusion 3D device simulation
  - Random dopants are introduced in GARAND through a rejection technique based on the continuous doping profile extracted from standard TCAD. LER is introduced in GARAND through randomly generated lines which can be applied to the gate edges.
  - Advantages: High accuracy as seen by verification with expt. Results
  - Limitations: Computationally prohibitive to perform detailed device-level simulation for any circuit larger than inverter.

- TCAD-Param Extraction-SPICE:
  - TCAD-based process and device design. Spice parameter extraction through specialized tools and SPICE simulations

- BSIM- SPICE Parameter Characterization from experimental data or TCAD-results.
### BSIM Parameters Identifications

<table>
<thead>
<tr>
<th>Device Parameter</th>
<th>Definition</th>
<th>BSIM Parameter</th>
<th>Definition</th>
<th>Sources</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tox</td>
<td>Gate oxide thickness</td>
<td>TOXE</td>
<td>Electrical Equivalent Tox</td>
<td>Oxide Thickness Variations</td>
</tr>
<tr>
<td>L</td>
<td>Channel length</td>
<td>XL</td>
<td>L offset due to masking and lithography</td>
<td>Gate length variations LER/LWR</td>
</tr>
<tr>
<td>Vth</td>
<td>Threshold voltage</td>
<td>VTHO</td>
<td>Vth at $V_{SB} = 0$</td>
<td>RDD with $V_{SB} = 0$</td>
</tr>
<tr>
<td>$\mu_{eff}$</td>
<td>Inversion carrier mobility</td>
<td>U0</td>
<td>Low field carrier mobility</td>
<td>Mobility fluctuations</td>
</tr>
</tbody>
</table>
Characterizing Variability

\[ \delta e_i = \sum_k \frac{\partial e_i}{\partial p_k} \delta p_k \]

\[ \sigma^2_{e_i} = \sum_k \left( \frac{\partial e_i}{\partial p_k} \right)^2 \sigma^2_{p_k} \]

- Accurately simulates \( e_i \)
  - this is the real goal of statistical simulation
- Different \( p_k \) for different compact models
- Sensitivities to be evaluated from SPICE simulation

Fab data/ TCAD data

SPICE

calculate
BSIM Parameter Calibration

Calibration for a 42nm/42nm nMOS transistor of oxide thickness 1.7 nm at Vds=1.1 V. (Ref. 1. EDL 2008: A. Cathignol et. al., 2. TED 2006: G. Roy et. al.)

<table>
<thead>
<tr>
<th></th>
<th>Atomistic Simulation Data</th>
<th>Standard deviation of process parameters</th>
<th>Value obtained from HSPICE simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>σVth (LER)</td>
<td>33 mV</td>
<td>σXL = 0.75 nm</td>
<td>33.09 mV</td>
</tr>
<tr>
<td>σVth (RDD)</td>
<td>52 mV</td>
<td>σVth0 = 52 mV</td>
<td>51.55 mV</td>
</tr>
<tr>
<td>σVth (OTV)</td>
<td>2.92 mV</td>
<td>σtox = 2.22e-11 m</td>
<td>2.89 mV</td>
</tr>
</tbody>
</table>
HSPICE-based Statistical Simulation

- V_th variation due to LER
  \[ L = 42 \text{ nm} \]
  \[ V_{gs} = 0.7 \text{ V} \]
  \[ V_{ds} = 1.1 \text{ V} \]
  \[ V_{ds} = 0.05 \text{ V} \]

- V_th variation due to RDD
  \[ L = 42 \text{ nm} \]
  \[ V_{gs} = 0.7 \text{ V} \]
  \[ V_{ds} = 1.1 \text{ V} \]
  \[ V_{ds} = 0 \text{ V} \]

- V_th variation due to OTV
  \[ L = 42 \text{ nm} \]
  \[ V_{gs} = 0.7 \text{ V} \]
  \[ V_{ds} = 1.1 \text{ V} \]
  \[ V_{ds} = 0.05 \text{ V} \]

- 42nm/42nm
  \[ V_{ds} = 1.1 \text{ V} \]
  \[ V_{gs} = 0.7 \text{ V} \]
Statistical Variation of Transconductance

- Non-skewed Gaussian distribution of VTHO, XL and TOXE.
- Skewed Gaussian distribution for RDD and LER.
- Higher moments must be determined and not the mean and standard deviations.
Analytical approach of Statistical Modeling:

From first order Taylor series expansion,

\[ e_1(p) \approx e_1(m_p) + \sum_{i=1}^{N_p} \left. \frac{\partial e_1}{\partial p_i} \right|_{p_i=m_p} (p_i - m_{p_i}) \]

Mean and variance of \( e_1 \) are defined as,

\[ m_{e_1} = e_1(m_p) \]

\[ \sigma_{e_1}^2 = \sum_{i=1}^{N_p} \left( \left. \frac{\partial e_1}{\partial p_i} \right|_{p=p_i} \right)^2 \sigma_i^2 \]
The drain current of a nano-scale MOS transistor for $V_{DS} > V_{DS,sat}$ is given by [BSIM 3]:

$$I_{DS} = W_{eff} v_{sat} C'_{ox} (V_{GS} - V_{th} - A_{bulk} V_{dsat}) \left(1 + \frac{V_{DS} - V_{DS,sat}}{V_{A}}\right)$$

where $V_{DS,sat}$ is given by,

$$V_{DS,sat} = \frac{E_{sat} L_{eff} (V_{GS} - V_{th})}{A_{bulk} E_{sat} L_{eff} + (V_{GS} - V_{th})}$$

The threshold voltage is modeled by,

$$V_{th} = V_{th0} - 0.5 \left(2V_{bi} - \phi_s\right) + V_{DS} \left(\frac{L_{eff}}{L'} - 1\right)$$
Impact of LER/LWR on $I_{DS}$

$$\sigma_{I_{DS,sat(LER/LWR)}}^2 = \left( \frac{\partial I_{DS,sat}}{\partial L_{eff}} \right)^2 \sigma_{L_{eff}}^2$$

Impact of RDD on $I_{DS}$

$$\sigma_{I_{DS,sat(RDD)}}^2 = \left( \frac{\partial I_{DS,sat}}{\partial V_{th0}} \right)^2 \sigma_{V_{th0}}^2$$

Results obtained

<table>
<thead>
<tr>
<th>Standard deviations of performances</th>
<th>Analytical</th>
<th>MC</th>
<th>% error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{I_{DS}(RDD)}$</td>
<td>3.50 µA</td>
<td>3.45 µA</td>
<td>1.45 %</td>
</tr>
<tr>
<td>$\sigma_{g_{ds}(RDD)}$</td>
<td>40.18 nS</td>
<td>40.09 nS</td>
<td>0.22 %</td>
</tr>
</tbody>
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<tr>
<td>$\sigma_{I_{DS}(LER/LWR)}$</td>
<td>2.41 µA</td>
<td>2.36 µA</td>
<td>2.12 %</td>
</tr>
<tr>
<td>$\sigma_{g_{ds}(LER/LWR)}$</td>
<td>1.87 µS</td>
<td>1.85 µS</td>
<td>1.08 %</td>
</tr>
</tbody>
</table>
RDD Reduction through Channel Engineering

- Threshold voltage fluctuation often leads to lowering of the statistical mean threshold voltage of the IC which ultimately leads to higher leakage power dissipation of the circuit.
- Very important to reduce the threshold voltage fluctuation due to RDD effect
  - New device architectures such as extremely thin SOI and FinFET
  - Relatively simple approach is to use channel engineered structure.

Asenov, TED 1999

IEDM 2011
Retrograde channel doping (Jacobs and Antoniadis. TED. Vol. 42. 1995)

- **Abrupt retrograde:**
  \[
  N(x) = \begin{cases} 
  N_s & x < x_s \\
  N_A & x > x_s \end{cases}, \quad N_s < N_A
  \]

- **Graded retrograde:**
  \[
  N(x) = \left[ \frac{(N_A - N_s)x}{x_s} + N_s \right], \quad x < x_s, \quad N_s < N_A
  \]

  \[
  = N_A, \quad x \geq x_s
  \]
Channel Profile Design

- Channel profile design for threshold voltage fluctuation reduction and getting desired threshold voltage for low power applications.

- Primary design parameters
  - Surface doping concentration
  - Transition depth.

- The total mean squared fluctuation of a uniformly doped channel MOS transistor considering dopant number fluctuation is given as (Takeuchi IEDM 1997)

\[
\sigma_{V_{TH}}^2 = \frac{q}{C_{ox}} \sqrt{\frac{N_A W_{dm}}{3LW}}
\]

- \( W_{dm} \): depletion width, \( L \) and \( W \) are channel length and width respectively. \( W_{dm} \) takes care of short channel effects in the transistor.

- For non-uniform doped channel \( N_A \) to be replaced by \( N_{EFF} \) defined as
Profile Design (Contd..)

\[ N_{EFF} = \left[ N_S + (N_A - N_S) \left( 1 - \frac{x_s}{W_{dm}} \right)^3 \right] \]

- For low value of threshold voltage, subthreshold leakage power increases.
  - For mobile computing applications, desired threshold voltage in the linear region \(\sim 0.4V\)
- Long Channel threshold voltage to be calculated for non-uniform doped channel
- Short channel effect considered through the following

\[ \Delta V_{TH} = -\frac{2(V_{bi} - 2\Phi_P) + V_{DS}}{2 \cosh \left( \frac{L}{l_t} \right) - 1} \]
Results: Abrupt Retrograde

Variation of threshold voltage with surface concentration

Variation of threshold voltage with transition depth

Variation of stand. dev. of threshold voltage fluctuation with surface concentration

Variation of stand. dev. of threshold voltage fluctuation with transition depth
Results: Graded Retrograde

Variation of threshold voltage with surface concentration

Variation of threshold voltage with transition depth

Variation of stand. dev. of threshold voltage fluctuation with surface concentration

Variation of stand. dev. of threshold voltage fluctuation with transition depth
Comparison between Abrupt and Graded

Comparison of threshold voltage for fixed transition depth

<table>
<thead>
<tr>
<th>Vds=0.05V</th>
<th>Xs=25(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Abrupt</td>
</tr>
<tr>
<td>Ns=5e17/cm³</td>
<td>Ns=1e17/cm³</td>
</tr>
<tr>
<td>Vth (V)</td>
<td>0.3432</td>
</tr>
<tr>
<td>sigma Vth (mV)</td>
<td>3.7016</td>
</tr>
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Comparison of threshold voltage for fixed surface concentration

<table>
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Observations

- With graded retrograde profile, higher threshold voltage can be achieved compared to abrupt retrograde under the same condition.
  - Beneficial for low leakage power applications.
- For minimizing the standard deviation of threshold voltage fluctuation, abrupt retrograde profile is the preferred structure.
- \( N_s = 5 \times 10^{17}/cm^3 \) and \( X_s = 25 \text{nm} \) may be used as the design parameters.
- Combination of abrupt and graded retrograde profile may be considered as new device architecture.
Verification with TCAD

Comparison of standard deviation of threshold voltage fluctuation for fixed surface concentration

<table>
<thead>
<tr>
<th>V_{ds}=0.05V</th>
<th>( N_s=5\times10^{17}/cm^3 ) (Nominal value)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Abrupt</td>
</tr>
<tr>
<td></td>
<td>( X_s=20\text{nm} )</td>
</tr>
<tr>
<td>sigma V_{th} (mV) (From TCAD)</td>
<td>3.971</td>
</tr>
<tr>
<td>sigma V_{th} (mV) (Analytical)</td>
<td>3.7371</td>
</tr>
</tbody>
</table>
Flicker Noise Modeling

- For analog and RF circuits, important limitations of down scaling of MOS technology are:
  - Statistical variability
  - Low frequency noise

- Scaling leads to increase of low frequency noise because the relative noise spectral density is inversely proportional to the gate area.

- Low frequency noise modeling important for analog and RF circuits:
  - Deteriorates the SNR in opamp and ADC/DAC
  - Increases the phase noise of oscillators in RF applications.

- Low frequency noise (1/f) noise originates from the fluctuations in the conductivity:
  - Fluctuations in the mobility
  - Total number of charge carriers
  - Both
Unified Flicker Noise Model

- Carrier number fluctuation model by McWhorter
  - Random trapping and de-trapping processes of charge in the oxide traps near the Si-SiO₂ interface.
  - Quantum mechanical tunneling transitions of electrons between the channel and traps in the gate oxide.
  - Charge fluctuations result in fluctuations of the surface potential which in turn modulate the channel mobile carrier density.
  - McWhorter model excellent agreement with experiments for n-type MOSFET.

- Mobility fluctuation by Hooge consider the flicker noise due to fluctuations of surface mobility based on Hooge’s empirical parameter.
  - Trapped carrier affects the surface mobility through Coulomb interaction.
  - Better suited for p-type MOSFET

- Unified model: Combinations of carrier number fluctuations and correlated mobility fluctuation model. BSIM3v3 noise model.
  - Independent of inversion carrier density
Physics-based Noise model for DG-FinFET

- Valid for all three regions of operations.
- Effects of mobility degradation due to velocity saturation, carrier heating and channel length modulation taken into considerations.
- Dependence of mobility fluctuations on the inversion carrier density incorporated.

- Generalized expressions implemented that can be used with any kind of mobility model and for a broad variety of noise-generation mechanisms.
- General model applicable for both n-channel and p-channel DG-FinFET.
Model Details

Drain current noise power spectral density is

\[
S_{id} = \frac{1}{I_{DS}L_c^2} \int_0^{V_D} g \left(1 + \frac{E}{E_{crit}} \right)^2 S_{\delta i_n^2} dV
\]

\[
I(x) = g(V, E) E = W \mu(x) Q_{inv}(x) E
\]

\[
g(V, E) = W \mu(x) Q_{inv}(x)
\]

Drain current noise power spectral density is

\[
S_{\delta i_n^2} \bigg|_{flicker} = \left[I_{DS} \left( \frac{q}{Q_{inv}(x) + nC_{ox} \phi_t} + \sigma_{sc} \mu_{eff} \right) \right]^2 \frac{N_{ot}}{Wf}
\]

\[
\sigma_{sc} = \sqrt{\frac{q}{K_1 \times 5.9 \times 10^6 (m/Vs)}}
\]

- Scattering parameter of carriers. K_1 = 1 for electrons and 0.2 for holes
- Not' is the equivalent density of oxide traps and 'f' is the operating frequency
Results (n-channel DG FinFET)

- $V_{GS}$ swept from weak to strong inversion.
- Plot obtained with varying scattering parameter agrees well with expt, data.
- Plot obtained with const. scattering parameter shows considerable mismatch in weak inversion.

In DG FinFET under weak inversion, due to volume inversion, electrons are spread throughout the channel. Thus coulomb scattering decreases and mobility increases. Efficient screening of trapped centres by the charge carriers.
Results (n-channel DG FinFET)

- Flicker noise decreases with increase in channel length.
- For a particular channel length, as $t_{Si}$ decreases, the flicker noise decreases. This is because of more prominent volume inversion effect.
- Below a definite current level, the noise decreases after reaching the peak owing to less number of carriers in the channel.
Results (p-channel DG FinFET)

- Same model applied to p-channel DG FinFET with different values of trap density and scattering parameter.
- Similar trend as n-channel DG FinFET.
Comparison (n and p-channel DG FinFET)

Due to higher value of oxide trap density of p-channel device (~9.6E13/m²) compared to n-channel device (~4.8E11/m²), flicker noise higher for p-channel device.

For same trap density (~9.6E13/m²) flicker noise in p-channel device less compared to n-channel. This is because of lower mobility of holes compared to that of electrons.
Summary and Conclusion

The two major limitations of down scaling of CMOS technology to analog and RF circuits are

- Statistical variations of circuit performances due to intra-die process variabilities
- Increased low frequency noise

Three major causes of intra-die process variabilities are

- Random discrete dopant effect
- Line Edge roughness
- Oxide thickness variations

Conventional deterministic IC design methodology fails to reflect the effect of intra-die process variabilities on circuit performances.

Atomistic and TCAD simulations of statistical variabilities though accurate at the device-level are not suitable at the circuit-level.

HSPICE-based statistical simulation. BSIM characterization of statistical variabilities.
Contd..

- Minimization of process variabilities at the device-level is an efficient approach without increasing the circuit complexity.
- Simple but efficient approach of minimizing RDD at the device-level is by vertical channel engineering approach.
- Retrograde profile is the preferred channel engineering approach
  - Abrupt retrograde profile preferred for minimizing the threshold voltage fluctuation.
  - Graded retrograde is the preferred profile for achieving desired threshold voltage for low power applications.
- Flicker noise to be modeled accurately for new devices like DG FinFET.
  - Physics-based noise model.
  - Valid in all three regions of operations.
- Scattering parameter dependent on inversion charge density plays significant role in DG FinFET under weak inversion region due to volume inversion.
- Flicker Noise in p-channel device is comparatively higher than that of the n-channel device due to higher number of oxide-trap densities in the former.
Team Members

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