TCAD assessment of gate-underlapped, Si and 4H-SiC, normally-on, vertical DG JFETs

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Outline

- SiC based Power Devices
- Comparison of Silicon and Silicon Carbide Materials
- Physical structure of 4H-SiC VJFETs
- Optimization of the Structure
- Thermal Analysis
- Conclusions
SiC based power devices

- SiC Power MOSFETs
- IGBTs
- GaN HEMTs
- SiC VJFETs
- SiC BJTs

- Goal of the project
  - Inverter for photovoltaic applications, using 4H-SiC JFETs
  - Development of compact model
Silicon and 4H-Silicon Carbide

❖ 4H-SiC

✔ SiC bandgap is three times that of Si
  ■ Breakdown field (10 times greater than Si)
  ■ Thinner highly doped voltage-blocking layers
  ■ High-temperature applications possible >> 300°C
✔ 4H-SiC: mobility much higher than for 6H- or 3C-SiC
✔ Saturated electron velocity of 4H-SiC is twice that of Si

❖ Si

■ Higher mobility than 4H-SiC
■ Higher switching speed
■ Low cost, ease of fabrication

<table>
<thead>
<tr>
<th>Property</th>
<th>6H SiC</th>
<th>4H SiC</th>
<th>3C SiC</th>
<th>GaAs</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wide Energy Bandgap (eV)</td>
<td>2.9</td>
<td>3.26</td>
<td>2.2</td>
<td>1.43</td>
<td>1.12</td>
</tr>
<tr>
<td>Electric Field Breakdown (10^8 V/cm @ 1000V operation)</td>
<td>2.5</td>
<td>2.2</td>
<td>2.0</td>
<td>0.30</td>
<td>0.25</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm °C @ Room T)</td>
<td>4.9</td>
<td>4.8</td>
<td>4.9</td>
<td>0.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Saturated Electron Drift (10^7 cm/s @ E &gt;2×10^5 V/cm)</td>
<td>2.0</td>
<td>2.0</td>
<td>2.5</td>
<td>1.0</td>
<td>1.0</td>
</tr>
</tbody>
</table>
TCAD simulation – mobility parameters

- Caughey-Thomas mobility model

\[
\mu_{n0} = \text{MU1N \_CAUG} \cdot \left( \frac{T_L}{300K} \right)^{\text{ALPHAN \_CAUG}} \\
+ \frac{\text{MU2N \_CAUG} \cdot \left( \frac{T_L}{300K} \right)^{\text{BETAN \_CAUG}}}{1 + \left( \frac{T_L}{300K} \right)^{\text{GAMMAN \_CAUG}}} - \frac{\text{MU1N \_CAUG} \cdot \left( \frac{T_L}{300K} \right)^{\text{ALPHAN \_CAUG}}}{\text{NCRITN \_CAUG}} \cdot \left( \frac{N}{\text{NCRITN \_CAUG}} \right)^{\text{DELTAN \_CAUG}}
\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Si</th>
<th>*4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU1N</td>
<td>cm²/Vs</td>
<td>55.2</td>
<td>40</td>
</tr>
<tr>
<td>MU2N</td>
<td>cm²/Vs</td>
<td>1429</td>
<td>950</td>
</tr>
<tr>
<td>NCRITN</td>
<td>cm⁻³</td>
<td>9.68×10¹⁶</td>
<td>2×10¹⁷</td>
</tr>
<tr>
<td>ALPHAN</td>
<td>-</td>
<td>0</td>
<td>-0.5</td>
</tr>
<tr>
<td>BETAN</td>
<td>-</td>
<td>-2.3</td>
<td>-2.4</td>
</tr>
<tr>
<td>GAMMAN</td>
<td>-</td>
<td>-3.8</td>
<td>0.0</td>
</tr>
<tr>
<td>DELTAN</td>
<td>-</td>
<td>0.73</td>
<td>0.76</td>
</tr>
</tbody>
</table>

*Roschke, Schwierz, IEEE TED 48(7), 2001
VJFETs with and without channel extension

- Normally-on VJFET **with** channel extension
  - $V_T$ depends on doping of channel & dimensions
  - $V_T$ less sensitive to drift region doping
  - Better performance (Ron vs. Breakdown voltage)

- Normally-on VJFET **without** channel extension
  - $V_T$ depends on doping of channel, drift region & dimensions
  - Highly sensitive to drift region doping

- Channel extension VJFET is desirable
Optimization of channel extension vertical DG JFET structure

- Normally-on VJFET with channel extension
  - $V_T$ not sensitive to drift region doping ($N_{dr}$)
  - Increase in drain current with increase of drift region doping

- Blocking voltage: slightly changes with $N_{dr}$
Optimization (breakdown vs. on-resistance)

- Normally-on VJFET with channel extension
  - Improved on-resistance ($R_{on}$) with higher $N_{dr}$
  - Almost same breakdown voltage
Comparison: Si and 4H-SiC vertical JFET

- Si and 4H-SiC (same physical parameters)
  - $V_T$ difference ~ 1.0 V
  - Breakdown field for 4H-SiC (~10 times greater than Si)
Comparison: Si and 4H-SiC vertical JFET

- **Si and 4H-SiC**
  - Optimize channel doping of Si JFET for similar $V_T$
  - Maintaining the ratio of channel doping ($N_{ch}$) to drift region doping ($N_{dr}$)

- 30% higher drain current for Si JFET (higher mobility)

$V_{ds} = 10 \text{ mV}$

$L_{ch} = 2 \mu\text{m}$

$T_{si} = 0.8 \mu\text{m}$

$V_{DS} = 10 \text{ mV}$

$N_{ch} = 4.3e16 \text{ cm}^{-3}$

$N_{dr} = 1e16 \text{ cm}^{-3}$

$N_{ch} = 5e16 \text{ cm}^{-3}$

$N_{dr} = 1.25e16 \text{ cm}^{-3}$

Si

4H-SiC

$V_{BD} = 1267 \text{ V}$

$V_{BD} = 134 \text{ V}$

$L_{ch} = 2 \mu\text{m}$

$T_{si} = 0.8 \mu\text{m}$

$V_{GS} = 0.0 \text{ V}$
Thermal analysis

- Si and 4H-SiC vertical JFET
  - Higher drain current for Si JFET
  - Drain current decreases slightly more for 4H-SiC with temperature
Thermal analysis

- Si and 4H-SiC vertical JFET
  - Lower $R_{on}$ for Si JFET
  - $R_{on}$ increases with increasing temperature
  - The increase in $R_{on}$ with increasing temperature is less for Si JFET
Outlook: compact model development

- First JFET charge-based model presented at MOS-AK 9/2012
- New model development underway
- Full charge-based intrinsic model for channel region
- Short-channel effects, scalability
- Drift extension modelling
Conclusions

- **Optimization**
  - Channel extension JFET is desirable for better on-resistance vs. breakdown voltage
  - Channel extension JFET, less sensitive for drift region doping.
  - Ratio of channel doping-to-drift region doping is very important.

- **TCAD based analysis, Si vs. 4H-SiC JFET**
  - 4H-SiC JFET – good for very high voltage, high power applications
  - Si JFET – performs better up to 150 V applications
  - Si JFET - less sensitive to temperature

- **Full scalable compact model for power JFETs underway.**
Acknowledgments

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