SMASH-ACMI*

for integration and validation of Verilog-A compact models into a SPICE simulator

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* ACMI = Automated Compact Model Injector
1. Context & Goals

2. How to generate the SPICE model

3. Automated validation

4. Performance comparison

5. Integration of BSIM-CMG into SMASH

6. Conclusion
1. Context & Goals

- Robust growth of the microelectronics industry during the past decades
- Demand for integrated circuits has led to the production of very complex designs
- Designers rely on compact models to accurately describe the behavior of devices

**Why is SPICE still trendy?**

- SPICE is not conjoint to any specific technology, therefore is extensively used
  - Semiconductor foundries deliver models of their devices in SPICE language
  - Schematic editors generate netlists for use in SPICE simulators
  - Designers implement circuits in SPICE

- Currently SPICE models are simulated faster and consume less memory than equivalent Verilog-A models in almost all EDA tools

- The microelectronics industry has accumulated important knowledge during few decades in SPICE language and SPICE-like simulators

“Designers take great pride in the knowledge that they accumulate at a great personal cost over the span of their career. As such, they are loath to give up their simulator, regardless of how badly it has treated them. This is a form of Stockholm syndrome.”

Ken Kundert, *Life after SPICE*
Why traditional manual implementation of compact models into SPICE-like simulators is out-of-date?

- SPICE is not standardized
  - Behavior of compact models can depend on the SPICE simulator

- SPICE model has already been integrated into another SPICE-like simulator
  - Any SPICE functionality is managed (collapsed conditions, SCALE option, ...)

- Equation translation into a programming language is complex and fastidious
  - Increase of "human errors" and risks of wrong behaviors
  - Increase in development and validation time

- Equation derivatives (needed by solver) are often manually computed
  - Wrong derivatives can slow simulations and/or cause convergence problems
  - Increase in development and validation time

- Compact model updates (added physical effects or corrections) are recurrent
  - Increase risks of adding regressions

Traditional manual method requires months of work

IC designers need access to compact models as soon as possible
• Why use Verilog-A Compact Model to obtain SPICE model?

- Verilog-A is a simple and high-level behavioral language, ideal for analog model development
  - Writing compact model in Verilog-A is faster than in a programming language

- Verilog-A is standardized and it is not tied to any specific simulator
  - Reduce risks of having different compact model behaviors in different simulators

- Verilog-A differs from SPICE on some points
  - Some SPICE behaviors are not intended in Verilog-A (collapse conditions, scaling, ...)

- Equation derivatives are automatically computed by the compiler/generator
  - Reduce convergence problems and increase simulation speed
  - Vastly reduce development and validation time

- Automated SPICE model generation depends on the compiler/generator
  - Risk to get wrong behaviors ⇒ Validation is always necessary and important
  - One defect corrected in the compiler/generator corrects all generated SPICE models

- Verilog-A compact model can be used as reference
  - Simplify validation phase and reduce validation time

⇒ Generating a SPICE model from a Verilog-A model requires some weeks
And it is safer than traditional manual implementation
2. How to generate the SPICE model

Modify

Initial Verilog-A model

Include

Modified Verilog-A model

SMASH-ACMI generator

Generate

SPICE model

Validation circuit files

Simulation Waveforms

Result

SMASH simulator

Automated validation

Post process

SMASH NRT feature

Equivalence check fails

Equivalence check succeeds

Validated SPICE model
2. How to generate the SPICE model

- Modifications to BSIM-CMG v106.0 Verilog-A Compact Model

Unlike the Verilog-A model, the SPICE model takes into account two types of parameters:
- Instance parameters
- Model parameters

The Verilog-A model modifications consist in adding attributes to parameters.
  - This just takes a few days.

  - Declare instance parameters
    - Add attribute `type=instance`
      ```
      (* type="instance" *) parameter integer NF = 1 from [1:inf);
      ```

  - Declare model and instance parameters (BSIM-CMG specific)
    - Add attributes `type=model` and `type2=instance`
      ```
      (* type="model", type2="instance" *) parameter real NRD = 0.0 from [0:inf);
      ```

  - Declare parameter aliases of existing internal parameters (for SMASH)
    - Add attributes `spice_name=name` and `alias=yes`
      ```
      (* spice_name="as", alias="yes" *) parameter real ASEO = 0 from [0:inf);
      ```

  - Add SMASH SPICE model documentation
    - Add attributes `info=text` and `unit=name`
      ```
      (* info="Body (Fin) thickness", unit="m" *) parameter real TFIN = 15n from [1n:inf]
      ```
3. Automated validation

- Generated DC, TRANSIENT, AC and NOISE circuit files (netlists)

Each netlist setup comprises:

- **Simulator control file**
  - Simulation conditions
  - Analysis type (DC, TRAN, AC or NOISE)
  - Waveforms to check

- **Circuit file**
  - SPICE BSIM-CMG device
  - Verilog-A BSIM-CMG device
  - Identical supplied voltage sources

- **Analog Verification file**
  - NRT directives
• Check equivalence between SPICE and Verilog-A simulation results

SMASH specific feature for non-regression testing
In EDA tools, the main goal is to integrate device models in order to have:

- Low memory consumption
- Fast simulation runtime

- Complex circuits used for performance comparisons

<table>
<thead>
<tr>
<th>Elements</th>
<th>Gendac (switch-capacitor techniques)</th>
<th>Memory</th>
<th>Switch inverter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>6 900</td>
<td>227 100</td>
<td>1</td>
</tr>
<tr>
<td>SPICE nets</td>
<td>320</td>
<td>4 350</td>
<td>20 000</td>
</tr>
<tr>
<td>BSIM-CMG MOS</td>
<td>550</td>
<td>10 800</td>
<td>40 000</td>
</tr>
<tr>
<td>Others elements (R, C, D, sources)</td>
<td>105</td>
<td>1 200</td>
<td>20 000</td>
</tr>
</tbody>
</table>
### Memory consumption comparison

Memory consumption depends principally on the number of complex devices such as MOS transistors.

<table>
<thead>
<tr>
<th>Memory consumption [Mb]</th>
<th>SMASH</th>
<th>Simulator B</th>
<th>Ratio Verilog-A / SPICE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Verilog-A</td>
<td>SPICE</td>
<td>Verilog-A</td>
</tr>
<tr>
<td>Gendac (550 MOS)</td>
<td>28</td>
<td>20</td>
<td>73</td>
</tr>
<tr>
<td>Memory (10,800 MOS)</td>
<td>97</td>
<td>88</td>
<td>619</td>
</tr>
<tr>
<td>Inverter (40,000 MOS)</td>
<td>207</td>
<td>187</td>
<td>Error</td>
</tr>
</tbody>
</table>
4. Performance comparison

- **Simulation runtime comparison**

Simulation runtime takes into account:

- Loading phase
- Operating point analysis
- Transient simulation

Simulation conditions are similar in both simulators (time step, number of threads, accuracy)

<table>
<thead>
<tr>
<th>Circuit runtimes [s]</th>
<th>SMASH</th>
<th>Simulator B</th>
<th>Ratio Verilog-A / SPICE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Verilog-A</td>
<td>SPICE</td>
<td>Verilog-A</td>
</tr>
<tr>
<td>Gendac (550 MOS)</td>
<td>1 370s</td>
<td>225s</td>
<td>3 880s</td>
</tr>
<tr>
<td></td>
<td>30.3k Iter</td>
<td>30.3k Iter</td>
<td>28.8k Iter</td>
</tr>
<tr>
<td>Memory (10,800 MOS)</td>
<td>2 260s</td>
<td>230s</td>
<td>6 430s</td>
</tr>
<tr>
<td></td>
<td>3.54k Iter</td>
<td>3.54k Iter</td>
<td>3.33k Iter</td>
</tr>
<tr>
<td>Inverter (40,000 MOS)</td>
<td>1 665s</td>
<td>270s</td>
<td>Error</td>
</tr>
<tr>
<td></td>
<td>0.78k Iter</td>
<td>0.78k Iter</td>
<td>0.80k Iter</td>
</tr>
</tbody>
</table>

Iter = Analog computed/converged time points
• **Advantages**

Integration of **BSIM-CMG v106.0** model into SMASH has been realized. Compared to the Verilog-A compact model, the SPICE model is:

- Equivalent
- With better performance (in terms of simulation speed and memory consumption)

• **Difficulties**

However, **some specific difficulties** have been met integrating BSIM-CMG v106.0:

- **Instance and model parameters**
  
  ```
  parameter real LRSD = L from (0:inf);
  ```

  What is the default value of instance parameter "LRSD"?
  
  Instance "L" or model "LRSD"?

- It cannot be checked with the Verilog-A implementation and the behavior is not specified in the documentation.

- **Collapse conditions - Adding drain/source series resistance**

  External source/drain resistance can be added depending on collapse conditions, checked during the instantiation phase.

  - Collapse conditions should be **"static"** and not change during simulations
  - In BSIM-CMG v106.0, collapse conditions are **"dynamic"**
    - Depend on potentials $V(g)$, $V(di)$ and $V(si)$
• Next BSIM-CMG release v106.1

What does BSIM-CMG release v106.1 (Sep. 2012) change?
  ▪ **Collapse conditions to add drain/source resistance are removed**
    - “dynamic” collapse conditions problems are solved
    - SPICE simulation runtime is slowed (x2)
      - Internal nodes “di” and “si” are always instantiated

Which BSIM-CMG release to integrate into SMASH?
  ▪ **BSIM-CMG release v106.1**
    - Need to apply latest model improvements
    - No dynamic collapse conditions
    - Slowed SPICE simulation runtime can be solved by adding “static” collapse conditions in the Verilog-A code
SMASH-ACMI
6. Conclusion

- **Automatic integration of Verilog-A compact models into a SPICE simulator is a better method compared to the “traditional” manual method**
  - Model integration can be from 6 to 12 times faster
    - 1-2 weeks for automated integration
    - ~3 months for traditional manual method
  - Risks of errors are considerably reduced (reduction of “human” intervention)

- **Integration of Verilog-A compact models into SPICE simulator is necessary to simulate complex circuits**
  - Simulation runtime can be from 6 to 10 times faster
  - Memory consumption can be reduced up to 40%

- **Integration of BSIM-CMG into a SPICE simulator**
  - Integration in a couple of weeks for v106.0, update to v106.1 in a couple of days
  - Difficulty to integrate v106.0 with external D/S resistances
  - Need to integrate v106.1 and to add static collapse conditions

- **Future updates of SMASH-ACMI (Automated Compact Model Injector)**
  - Develop a graphic interface to generate the SPICE model and manage validation circuits
  - Extend automated validation
    - transient noise analysis, multiplicity checking, additional model cards...
  - **Provide SMASH-ACMI to Compact Models developers**
Thanks!

Reference
« Why- & How to- Integrate Verilog-A Compact Models in SPICE Simulators »
by Maria-Anna Chalkiadaki, Cedric Valla, Frederic Poulet, Matthias Bucher
International Journal of Circuit Theory and Applications