Thermal Network Extraction in Ultra-Thin-Body SOI MOSFETs

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Outline

- Introduction
- Thermal Network Characterization
- Results
- Other News

Introduction

- Carrier scattering leads to heat generation
- Dominant at drain end of MOSFET due to high field
- Temperature increase affects device parameters e.g. threshold voltage, mobility etc.

Power Density and scaling

1971

2,300 transistors in Intel 4004 processor (10µm)

Technology Progress

Technology node

Number of Transistor

1.4 billion transistors in Intel Ivy Bridge 4C (22nm)

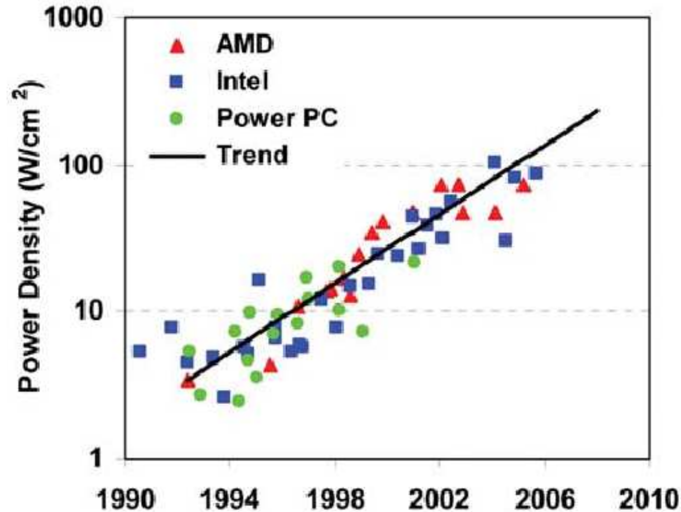


Figure : Trend of on chip power density over the past 10 years. Solid line marks an exponential trend.

Source: E. Pop et al., "Heat Generation and Transport in Nanometer-Scale Transistors", Proceedings of the IEEE , August 2006.

Self Heating & Technology Scaling

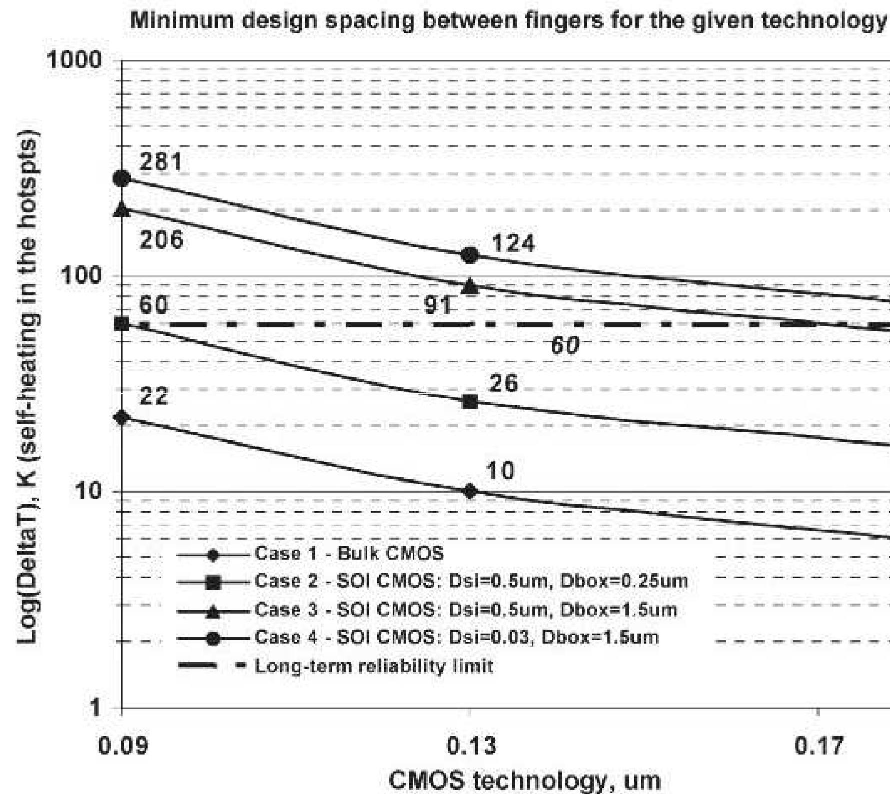


Figure: Increase in ΔT with technology scaling

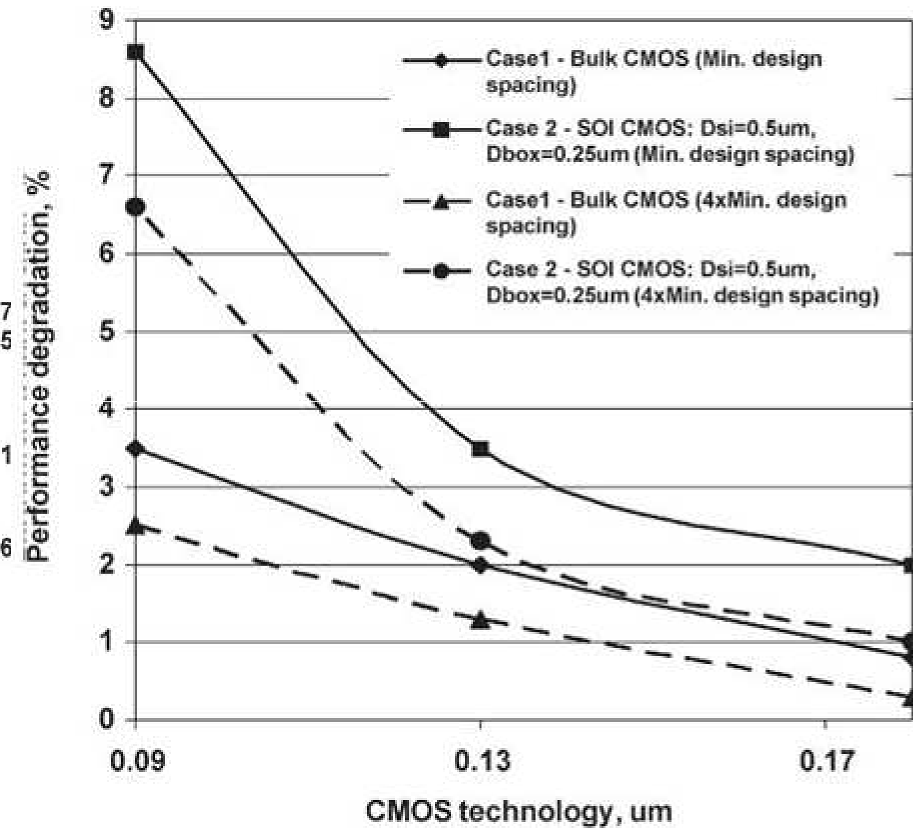


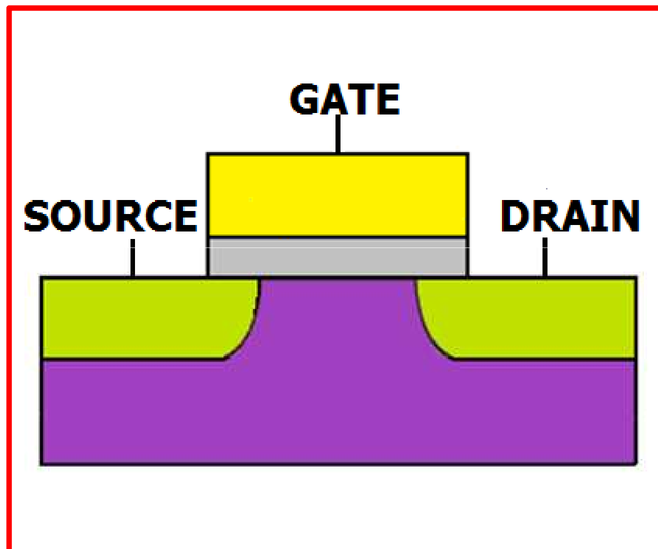
Figure: Performance degradation of a three stage ring oscillator due to self heating effect versus technology scaling

Source: O. Semenov et al., IEEE Tras. on Device and Materials Reliability, March 2006

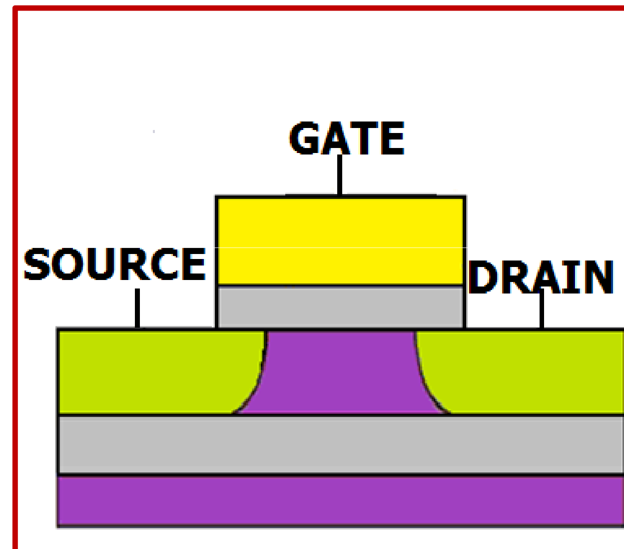
Self Heating: Effect of Structure/Technology

Evolution of MOSFET Architecture

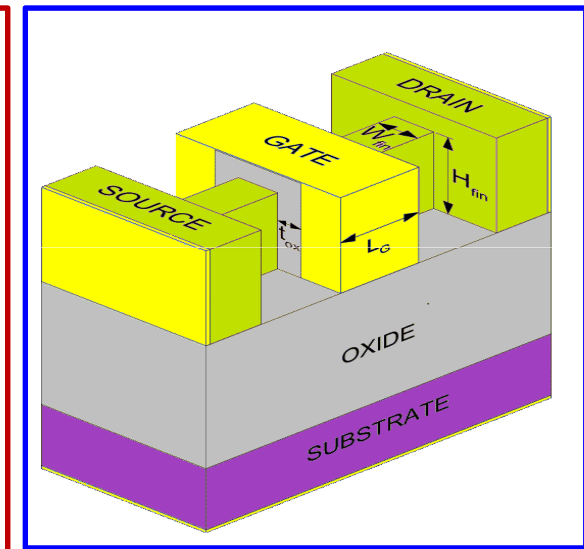
Bulk MOSFET



SOI MOSFET



FinFET

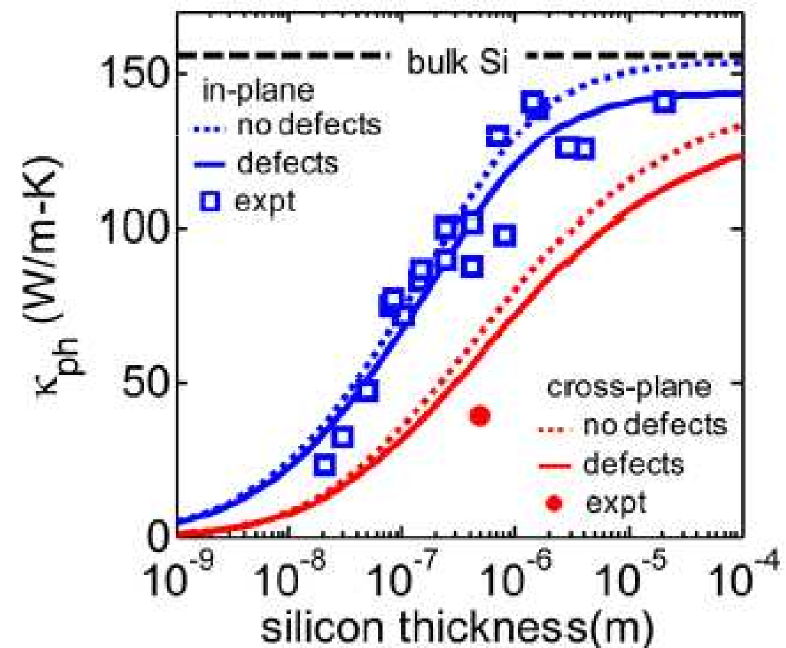


- Technology scaling achieved by
  - New materials (SOI, High-K dielectric, Strained Silicon etc.)
  - Highly confined geometry
- New materials and greater confinement increased self heating effect

Confinement & Thermal Conductivity

- Bulk Si – 50% of the heat conduction is carried by phonons with a mean-free-path greater than about 1 μ*m*.
- For film thickness is smaller than ~200*nm*, 50% of the heat is carried by phonons with mean-free-paths longer than the film thickness.

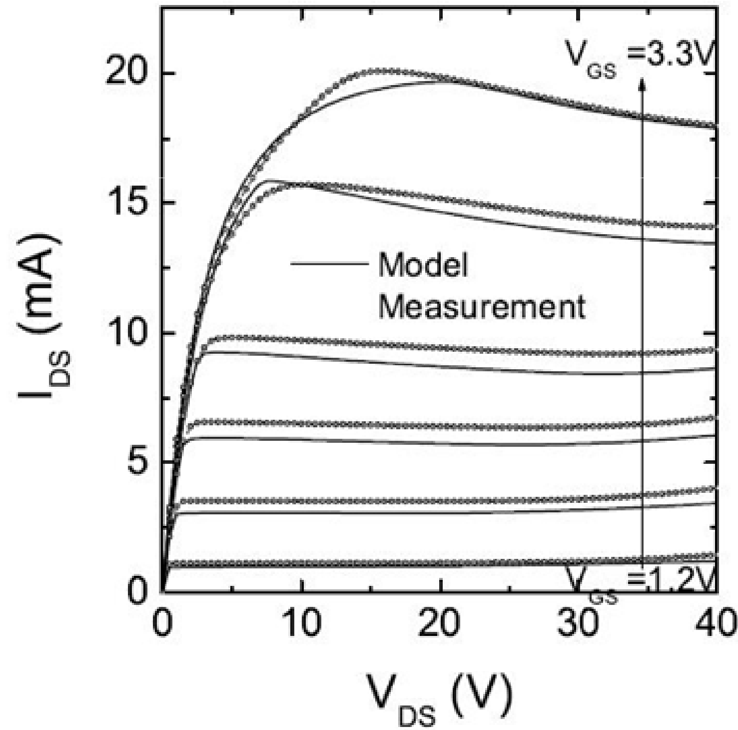
Material	Thermal conductivity (W/m-K)
Si(Bulk)	149
Ge	60.2
SiO_2	1.4
HfO_2(>500nm)	1.2
HfO_2(3nm)	0.27-0.49

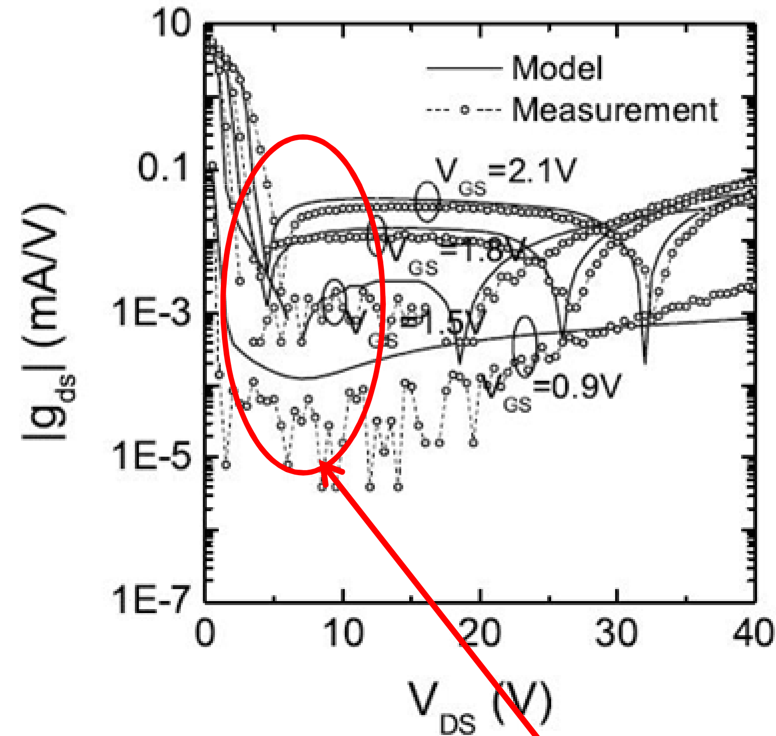


Source: Ch. Jeong, S. Datta, M. Lundstrom "Thermal conductivity of bulk and thin-film silicon: A Landauer approach" JOURNAL OF APPLIED PHYSICS 111, 093708 (2012)

Impact of Self Heating

Note decrease in current with VDS

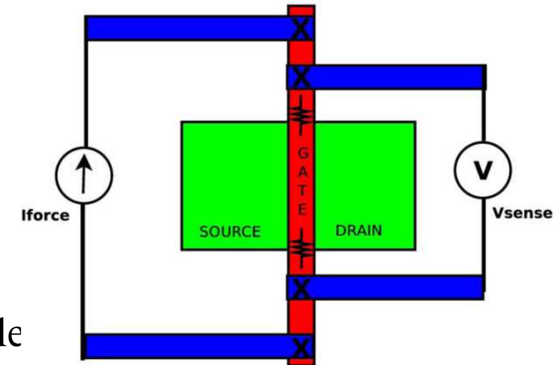




Negative g_{ds}

Self Heating Measurement

- Gate Current measurement
  - Requires dedicated structures
  - Measures gate temperature



Ref.: S. Khandelwal et al., "Scalable Thermal Resistance Model for single and multi-finger Silicon-on-Insulator MOSFETs", IEEE ICMTS, April 2011

- Pulsed measurement technique
  - DC structures can be used
  - Requires dedicated setup
  - Works upto limited frequencies.

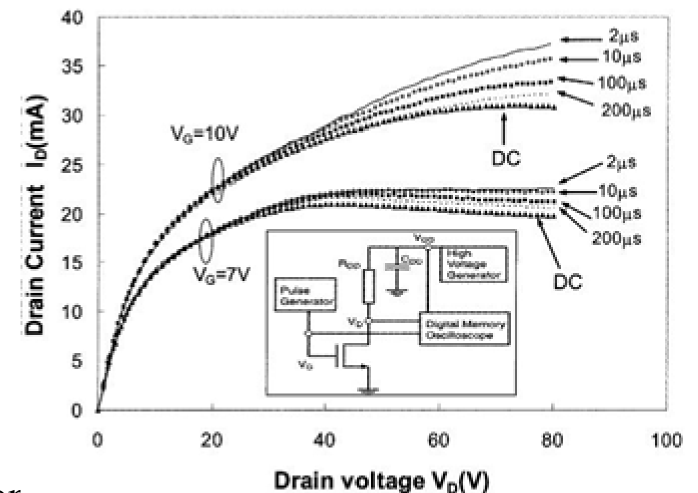


Figure: Output characteristics of n-channel DMOSFET. Comparison b/w steady state DC measurement and different pulse width measurement. Inset the measurement setup.

Ref.: C. Anghel et al., "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs",IEEE EDL 2004

Self Heating Measurement

- Small signal conductance technique
  - DC structures can be used
  - Widely used technique
  - What if there is no clear self heating free region?

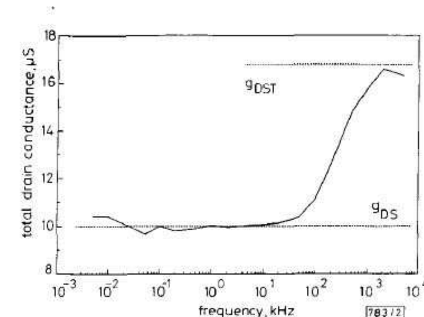


Fig. 2 *Measured drain conductance against frequency for 20 µm wide, 3 µm partially depleted SIMOX MOSFET with source connected body-tie* [8]
$V_{DS} = 2$ V, $I_{DS} = 745$ µA

Ref.: W. Redman-White et al., "Direct Extraction of MOSFET Dynamic Thermal Characteristics from Standard Transistor Structures using Small Signal Measurements", Electronics Letters, June 1993.
Ref.: Wei Jint et al.,"Self-Heating Characterization for SOI MOSFET Based on AC Output Conductance", IEDM 1999

- S- parameter measurement technique
  - Versatile technique
  - Requires dedicated RF structures and measurements

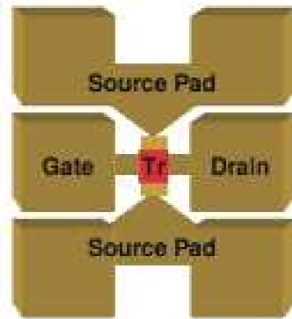
Ref. 1: M. A. Karim et al., "Extraction of Isothermal Condition and Thermal Network in UTBB SOI MOSFETs", IEEE EDL 2012
Ref. 1: A.J. Scholten et al., "Experimental assessment of self-heating in SOI FinFETs", IEDM 2009
Ref. 2: N. Rinaldi et al., "Small-Signal Operation of Semiconductor Devices including Self-heating, with Application to Thermal Characterization and Instability Analysis", IEEE TED 2001

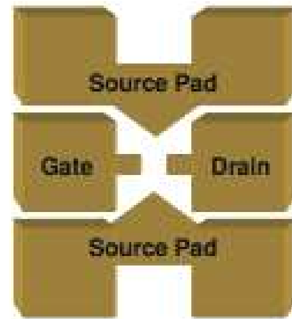
S-parameter measurement

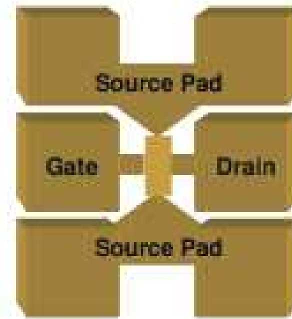
- S-parameters measured using vector network analyzer (VNA) (e.g. Agilent E5071C ENA with frequency range of 100 kHz–8.5 GHz)

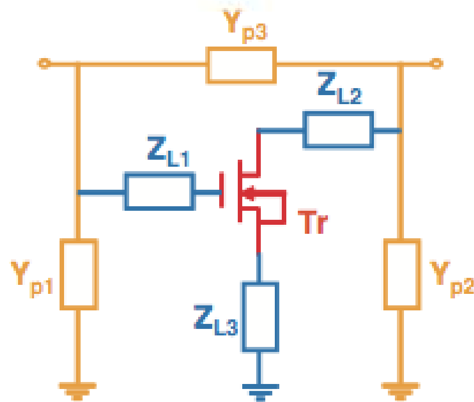
- De-embedding
  - Use de-embedding to remove parasitics
  - Probe/wire parasitics are de-embedded using calibration substrate
  - Pads to device parasitics are de-embedded using OPEN-SHORT de-embedding

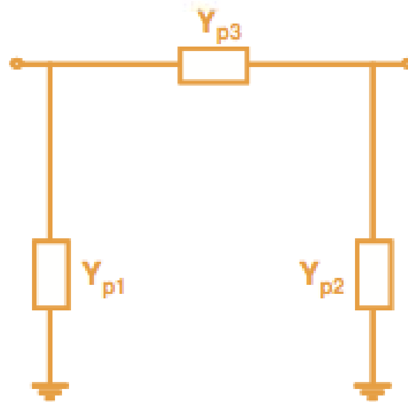
Self Heating: Open-Short De-embedding

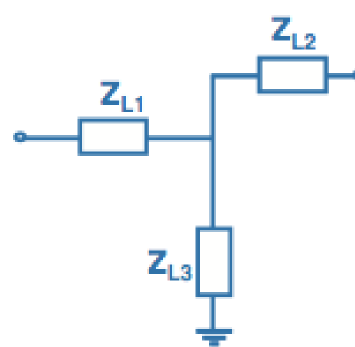












(a) (b) (c)

Device Open Short

De-embed from Open:

$Y_{DUT/Open} = Y_{Total} - Y_{Open}$

$Y_{Short/Open} = Y_{Short} - Y_{Open}$

Convert to Z:

$Z_{DUT/Open} = Z(Y_{DUT/Open})$

$Z_{Short/Open} = Z(Y_{Short/Open})$

De-embed from Short:

$Z_{DUT} = Z_{DUT/Open} - Z_{Short/Open}$

Convert to S:

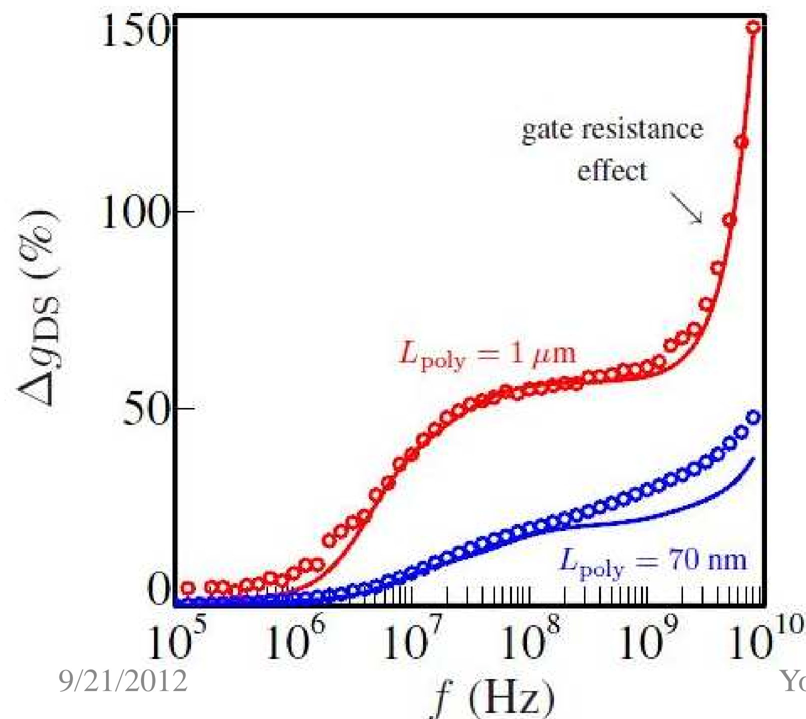
$S_{DUT} = S(Z_{DUT})$

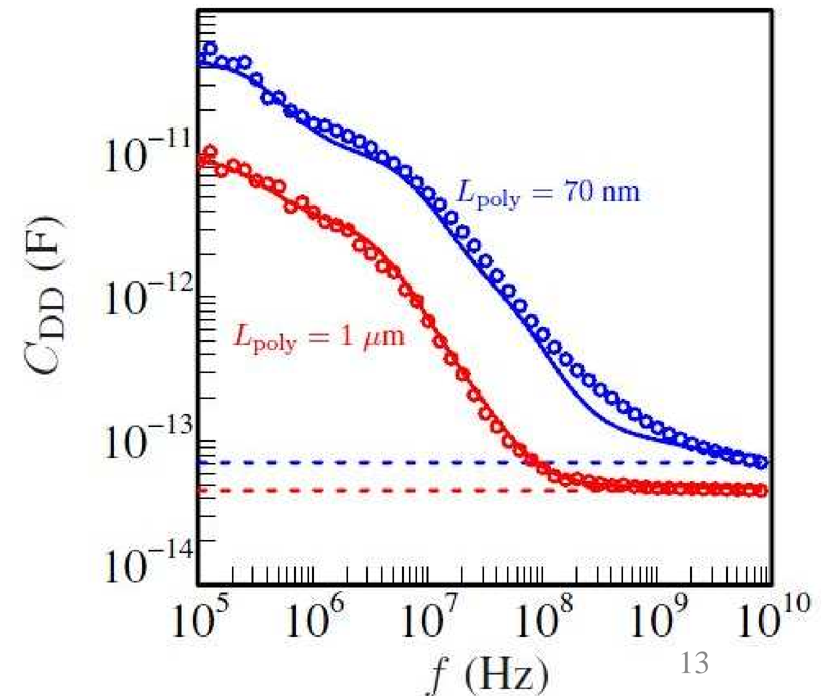
Courtesy: Agilent Technologies

Issues in thermal network extraction

- No self heating free region in gds due to parasitics in short channel devices
- Electrical contribution in C_{DD} cannot explain 2-3 order decrease

Ref.: A.J. Scholten et al., "Experimental assessment of self-heating in SOI FinFETs", IEDM 2009





Issues in thermal network extraction

- Impact of choosing arbitrary isothermal frequency

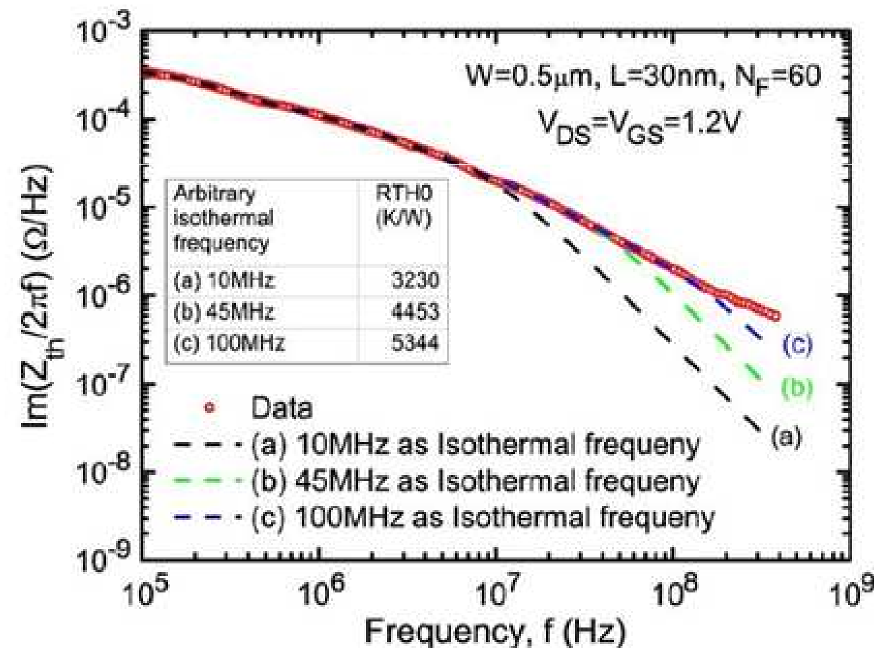


Figure: Extraction of DC thermal resistance (RTH0) using different arbitrary isothermal frequencies.

Our Approach: Thermal Network Extraction

- Thermal contribution in $Im(Y_{DD})$ dominates over electrical (substrate and/or gate resistance network) at low-frequency
- $Im(Y_{DD})$ at V_{GS}=1.4V $\propto$ $Im(Y_{DD})$ at V_{GS}=1.2V
  - Proportionality constant depends on the ratio of currents
- Around isothermal frequency, electrical contribution start dominating over thermal contribution to $Im(Y_{DD})$, and proportionality relationship becomes invalid
- Frequency at which splitting happens is the isothermal frequency

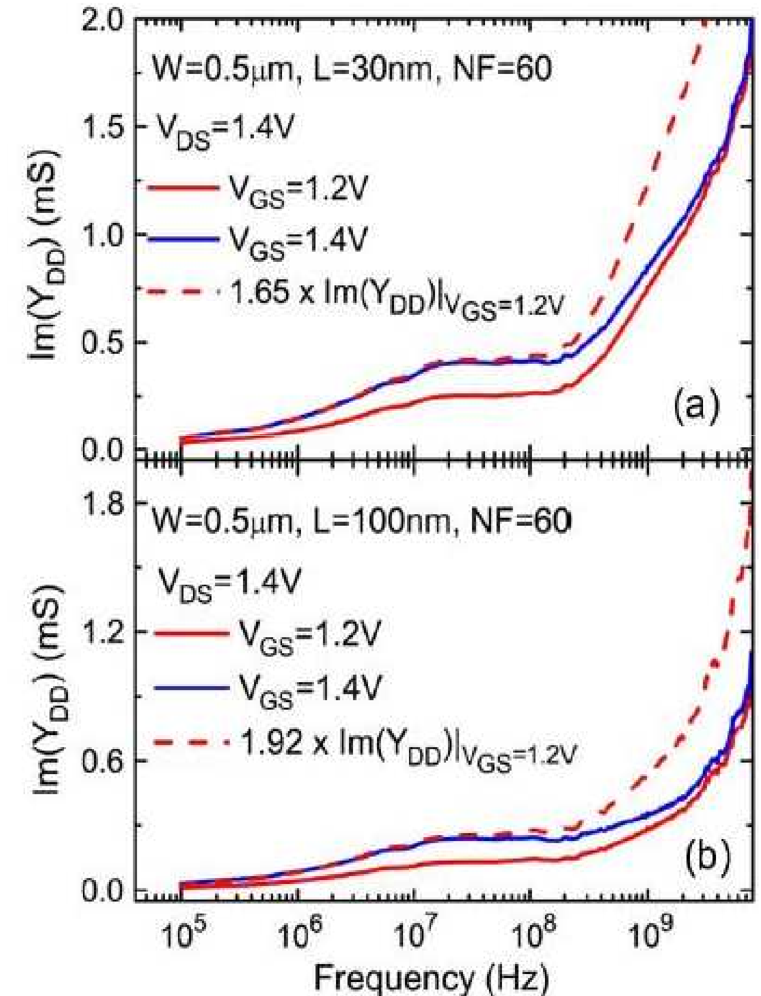


Figure: Measured $Im(Y_{DD})$ of UTBSOI MOSFET

Our Approach: Thermal Network Extraction

- Simultaneous fitting of $Re(Y_{DD})$ and $Im(Y_{DD})$ as both are sensitive to change in temperature.

$$Z_{th} = \frac{Y_{DD} - Y_{DD}^{iso}}{\frac{dI_{DS}}{dT_{abm}}\left(I_{DS} + V_{DS} \cdot Y_{DD}\right)}$$

$$Im\left(Y_{DD}\right) = \frac{Im\left(Z_{th}\right)\left[Re\left(Dn\right)^2 + Im\left(Dn\right)^2\right]}{Re\left(Dn\right)} + \frac{\left[Re\left(Y_{DD}\right) - \left(Y_{DD}^{iso}\right)\right] Im\left(Dn\right)}{Re\left(Dn\right)}$$

Where,

$$Dn = \frac{dI_{DS}}{dT_{amb}}\left(I_{DS} + V_{DS} \cdot Y_{DD}\right)$$

Self Heating: Thermal network

Thermal impedance of nth order thermal N/W

$$Z_{th} = \sum_{i=1}^{n} \frac{R_{thi}}{1 + j(2\pi f) R_{thi} C_{thi}} \quad \text{or} \quad Z_{th} = \sum_{i=1}^{n} \frac{R_{thi}}{1 + (2\pi f)^2 (R_{thi} C_{thi})^2} - j(2\pi f) \sum_{i=1}^{n} \frac{R_{thi}^2 C_{thi}}{1 + (2\pi f)^2 (R_{thi} C_{thi})^2}$$

Equivalent Thermal resistance R_{th}

$$\mathrm{Re}(Z_{th}) = \sum_{i=1}^{n} \frac{R_{thi}}{1 + (2\pi f)^2 (R_{thi} C_{thi})^2}$$

Equivalent Thermal capacitance C_{th}

$$\mathrm{Im}(Z_{th}) / (2\pi f) = \sum_{i=1}^{n} \frac{R_{thi}^2 C_{thi}}{1 + (2\pi f)^2 (R_{thi} C_{thi})^2}$$

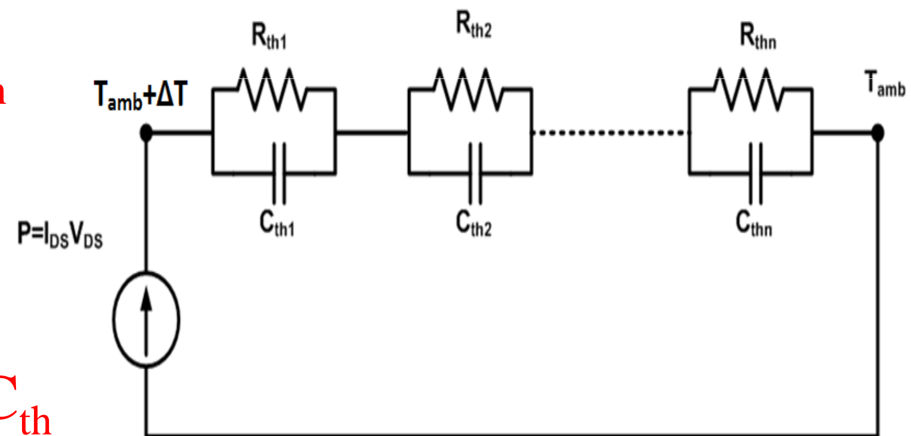


Figure: nth order thermal network

DC Thermal resistance RTH0

$$\mathrm{RTH0} = R_{th}\big|_{f=0} = \sum_{i=1}^{n} R_{thi}$$

Order of thermal network

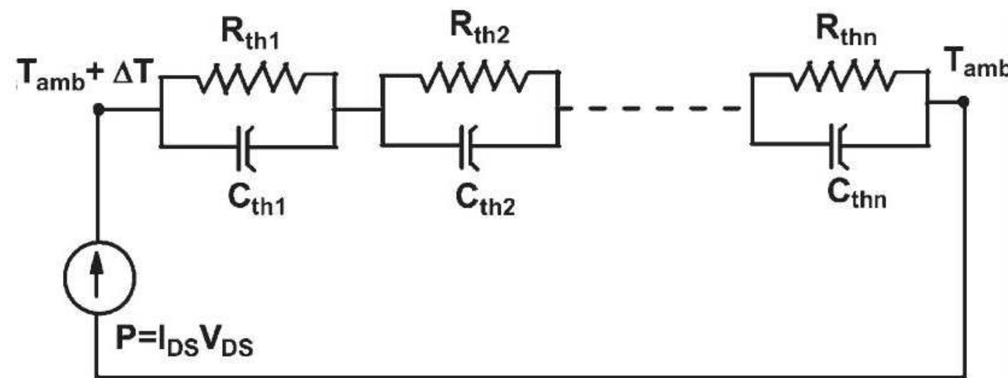


Figure: nth order thermal network

Accuracy increase with order of network but computational efficiency of the model goes down

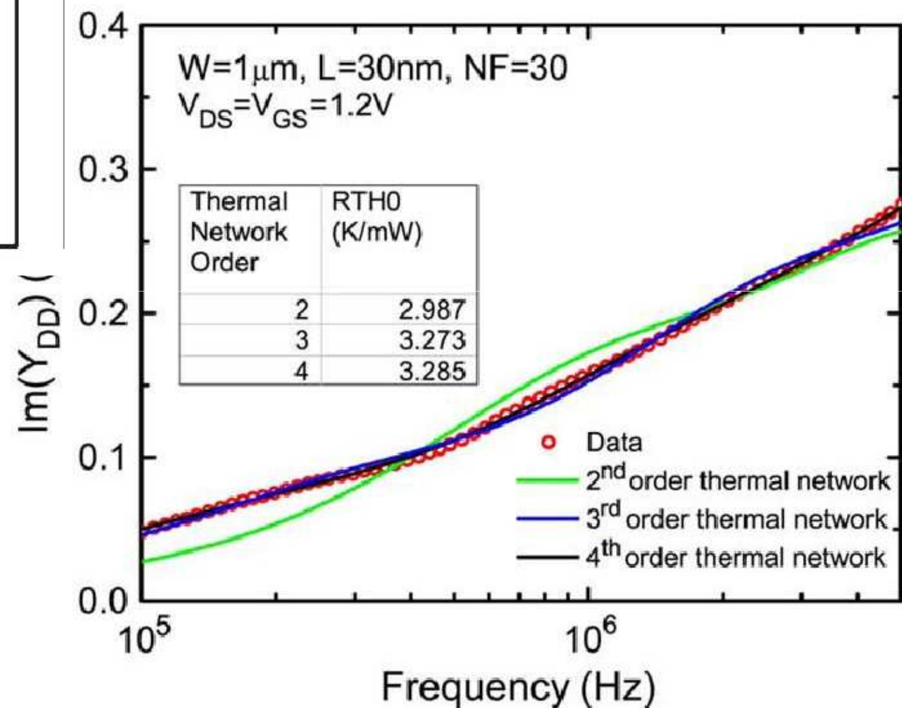


Figure: Fitting of $Im(Y_{DD})$ using various-order thermal networks independently. Results are shown for the self-heating dominated segment of the spectrum

Results

- Third order network extracted by simultaneous fitting of $Re(Y_{DD})$ and $Im(Y_{DD})$

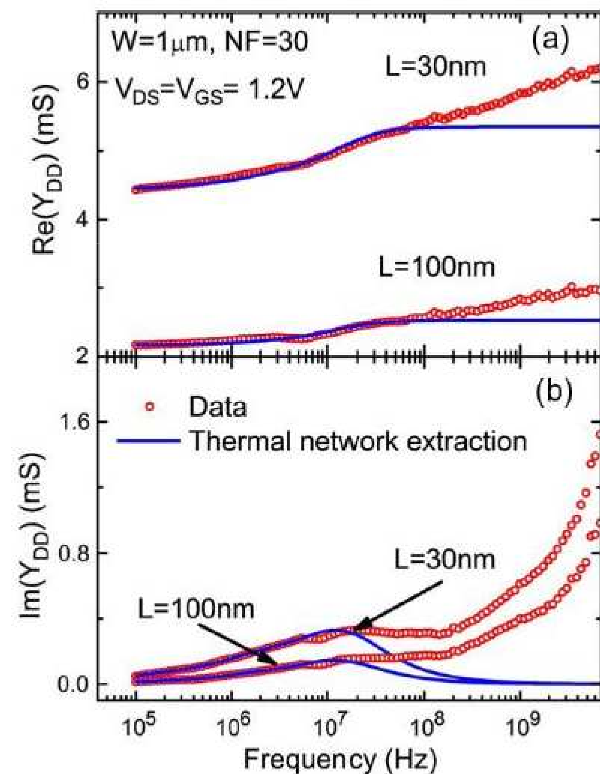


Figure: Measured and extracted $Re(Y_{DD})$ and $Im(Y_{DD})$ on 30nm and 100nm length UTBSOI devices. $V_{GS}=V_{DS}=1.2V$.

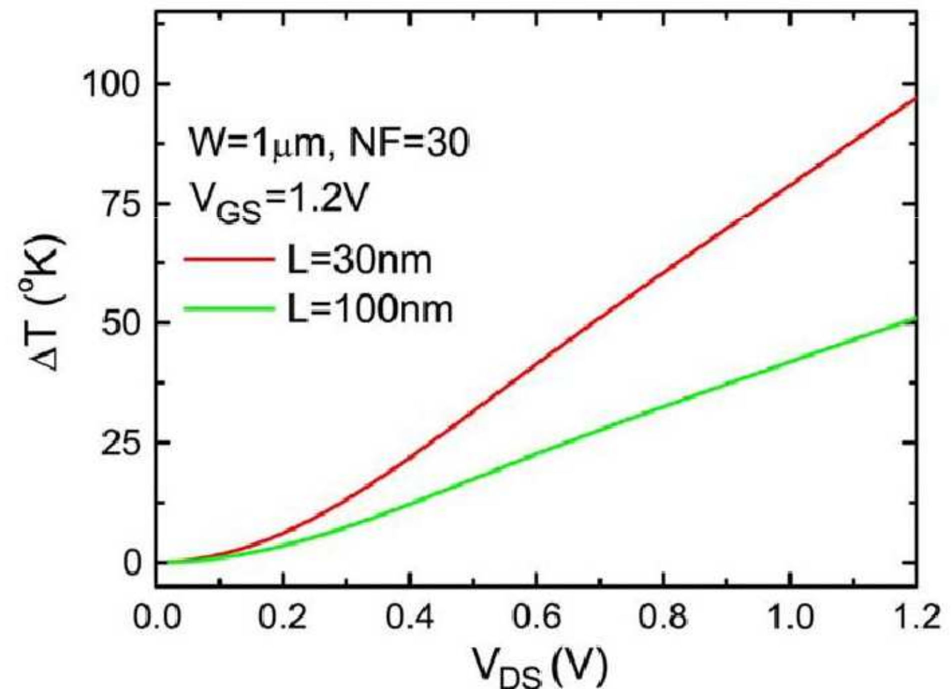


Figure: DC temperature rise for 30nm and 100nm length devices due to self heating effect.

Self Heating – Should we care?

- Digital circuits operate in 1-2 GHz range
  - No effect of self heating ☺
- RF circuits operate in 5-100 GHz range
  - No effect of self heating ☺

- Analog circuits operate in KHz-MHz range
  - Self heating is dominant up to ~30-40 MHz
  - Analog designers should be careful ☹

Conclusion

- A better approach for thermal network extraction was presented
- Temperature may rise by more than 100ºC due to self heating effect in SOI devices
  - I_{dsat} decreases around 4-5%
- Digital and RF circuits doesn't get affected by SHE
  - Analog circuits do have performance degradation
- Ref.

    - M. A. Karim, Y. S. Chauhan, S. Venugopalan, A. B. Sachid, D. D. Lu, B. Y. Nguyen, O. Faynot, A. M. Niknejad, and C. Hu, "Extraction of Isothermal Condition and Thermal Network in UTBB SOI MOSFETs", IEEE Electron Device Letters, Vol33, No.9, Sept. 2012.

Other News

- Released BSIM6.0.0-beta8 in Aug. 2012 with improved global scaling
  - Received Excellent feedback on the model
- Released CMC standard BSIM-CMG 106.1.0 in Sept. 2012
- Released BSIM4.7.1-beta for testing
- Released BSIMSOI4.5-beta for testing

Acknowledgment

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