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Pursuing Excellence

Millimeter-Wave CMOS Device Modeling and Issues

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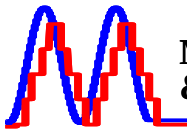


Matsuzawa
& Okada Lab.

Outline

- Motivation
  & Brief introduction of 60GHz CMOS transceiver
- Modeling issues
  - Measurement issues
  - Substrate modeling issues
- Layout optimization
- Transistor characterization
- Summary & Conclusion

Motivation

- **60GHz CMOS transceiver for multi-Gbps wireless communication**

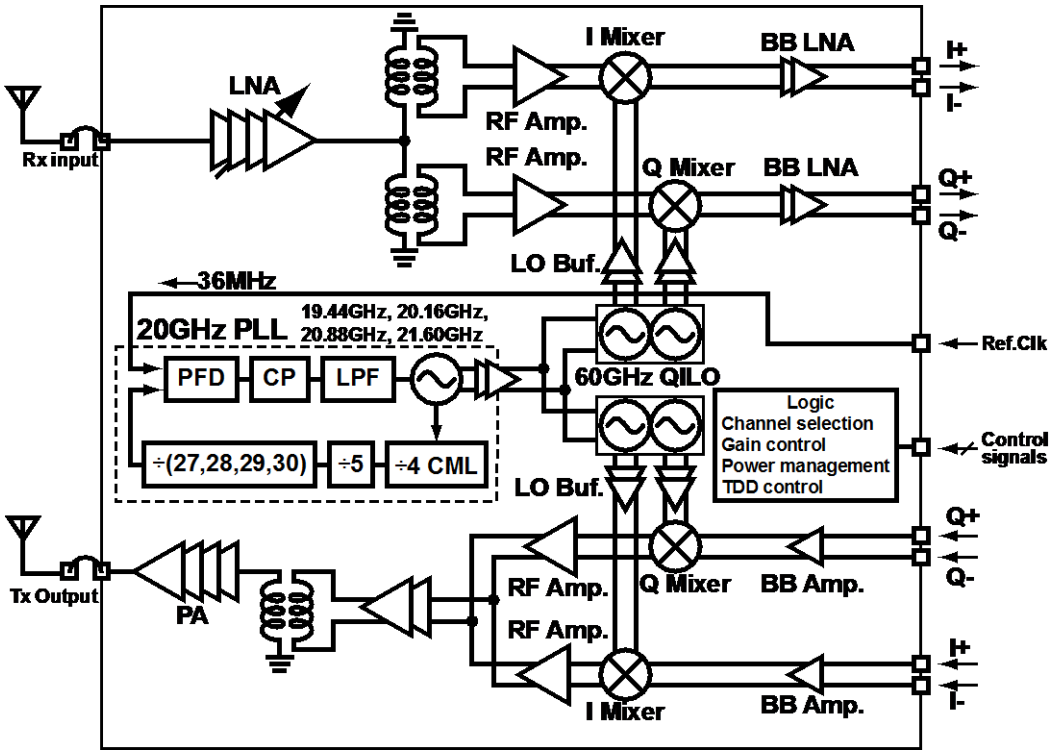
IEEE 802.11ad specification

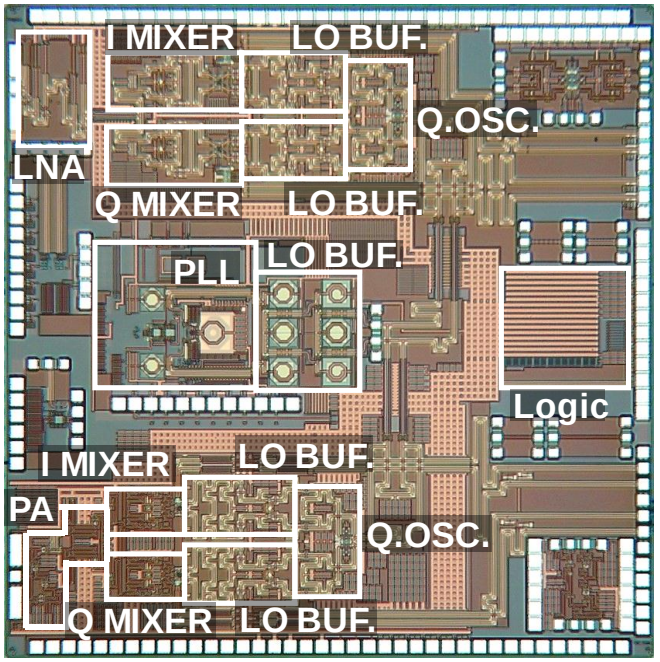
- **57.24GHz - 65.88GHz**
- **2.16GHz/ch x 4channels**

	QPSK	16QAM	64QAM
2.16GHz x1ch	3.4Gbps	6.8Gbps	10.1Gbps
2.16GHz x4ch	13.5Gbps	27.0Gbps	40.6Gbps

60GHz Direct-Conversion Transceiver

- **2.4GHz *vs* 60GHz (25x)**
  - ➔ **RF front-end (Tx/Rx/LO)**
    - **– Simulation/Modeling, Gain, Noise, Pout**



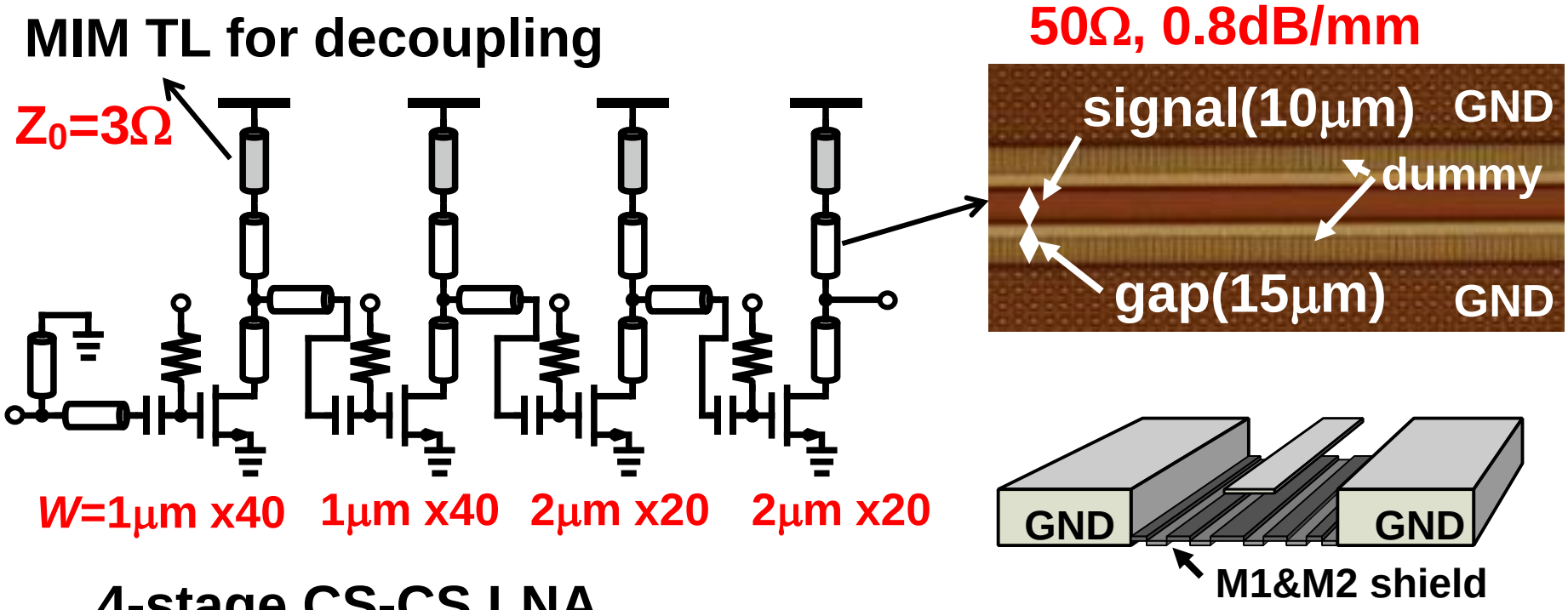


65nm CMOS, 4.2x4.2mm

[1] K. Okada, *et al*., ISSCC 2012

TL-Based Design

- TL-based design for simulation accuracy
- Low-loss TL & MIM TL



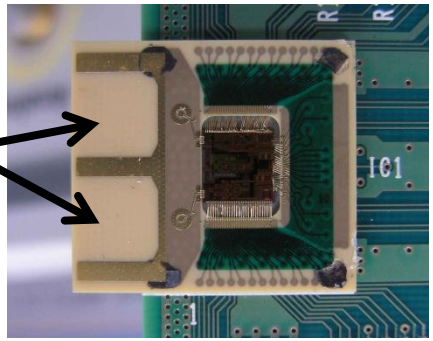
4-stage CS-CS LNA

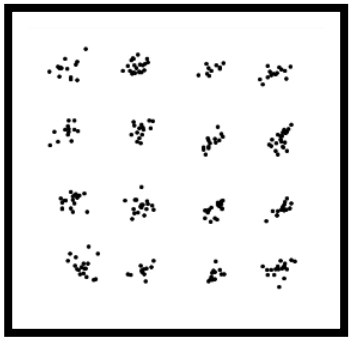
[2] K. Okada, *et al*., ISSCC 2011

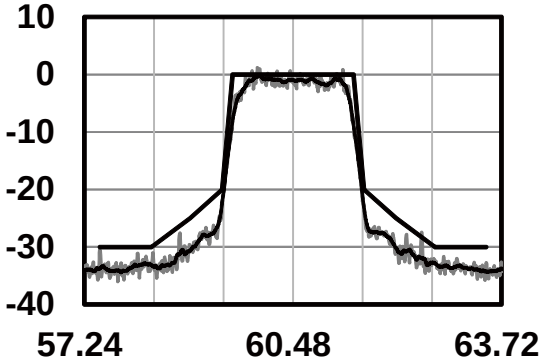
Performance Summary

	Arch.	Max. rate in 16QAM	Distance for BER $<10^{-3}$	P_{DC} (Tx/Rx)
IMEC[3]	Direct	7Gb/s	ch.1-4 (EVM < -17dB) (w/o PLL)	176mW / 112mW
SiBeam [4]	Hetero	7Gb/s	ch.2-3 (EVM < -19dB) 50m(LOS), 16m(NLOS)	1,820mW / 1,250mW
This work	Direct	10Gb/s-	ch.1-4 (EVM < -23dB) 1.3-1.6m (QPSK) 0.3-0.5m (16QAM)	319mW / 223mW

6dBi antennas







[3] V. Vidojkovic, *et al*., *ISSCC* 2012 [4] S. Emami, *et al*., *ISSCC* 2011

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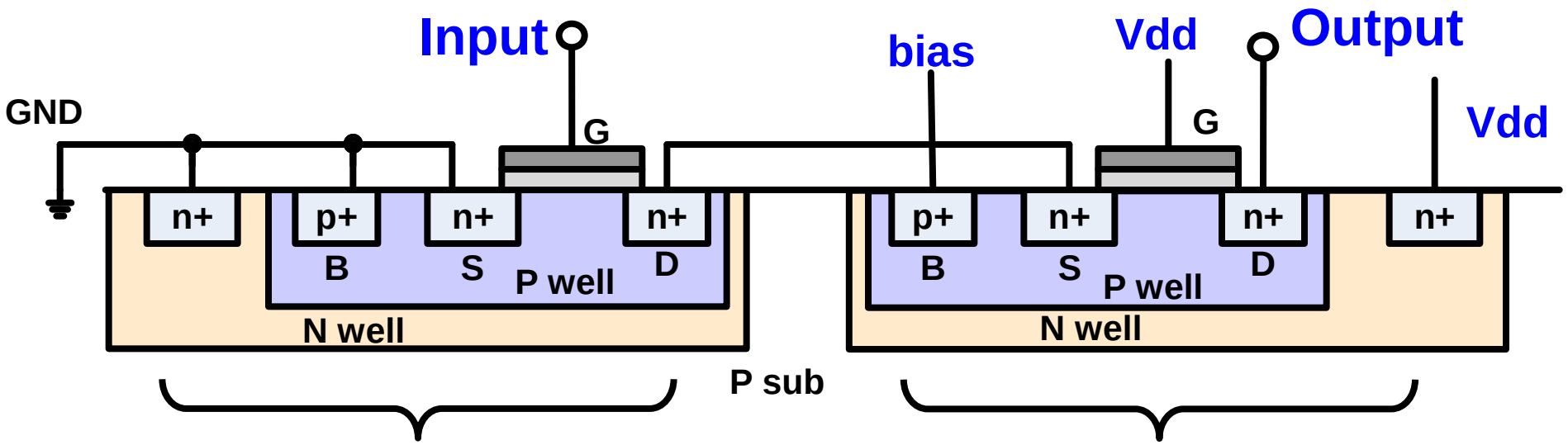
Issues of mmW Tr Modeling

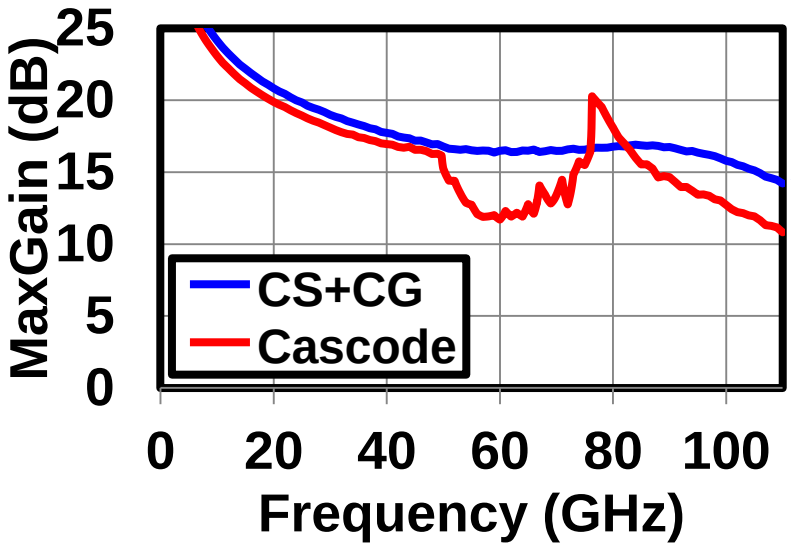
- **Bias scalability**
- **L & W scalability**
- **Linearity**
  - **Large-signal accuracy for RF and mmW**
- **Noise**

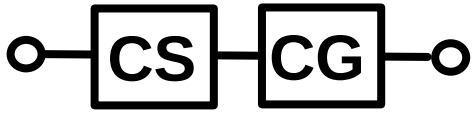
caused by

- **Measurement inaccuracy**
- **Complex physical and electrical structure of miniaturized transistors**
  - **Substrate model**

Substrate Coupling







connect S-parameters measured individually

completely same layout but different characteristics

Substrate model issue

- **Measurement through drain, gate and source is not so reliable to build an equivalent circuit of the substrate network.**
- **Up to 10GHz**
- **CS meas. + CG meas. ≠ Cascode meas.**
- ***L*, W_f-scalability, V_B dependence**

Current status & Target

	DC (< 1GHz)	RF (< 10GHz)	mmW (> 10GHz)
Bias dep. (V_G, V_D)	✓	✓	✓
Bias dep. (V_S)	✓	✓	partially
Bias dep. (V_B)	✓		
#finger scalability	✓	✓	✓
W_f scalability	✓	✓	
L scalability	✓		
Non-linearity (IM3)	✓	✓	partially
Large-signal	✓	partially	
Noise	✓	partially	

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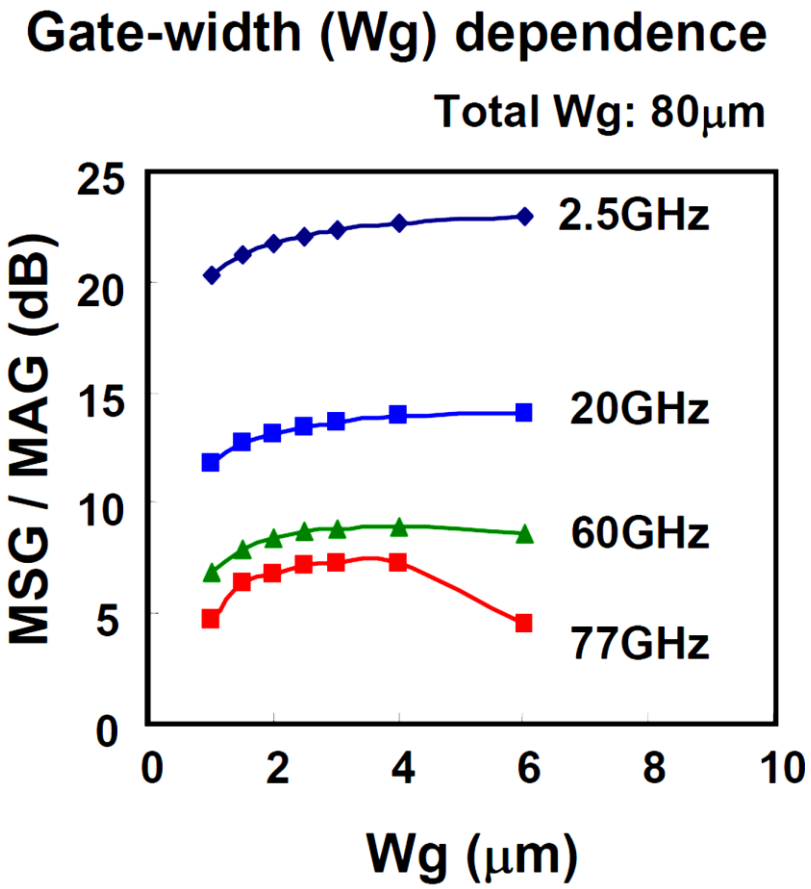
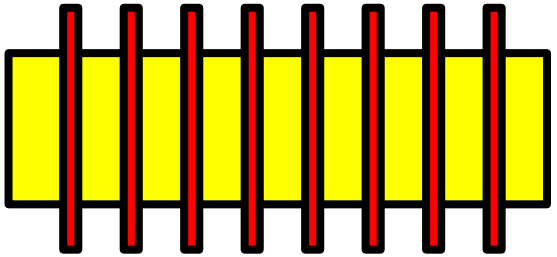
Finger Width Optimization



[5] T. Suzuki, ISSCC 2008

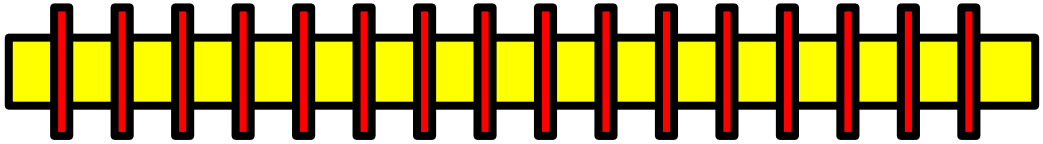
W=2umx8

- **MAG peak ↗**



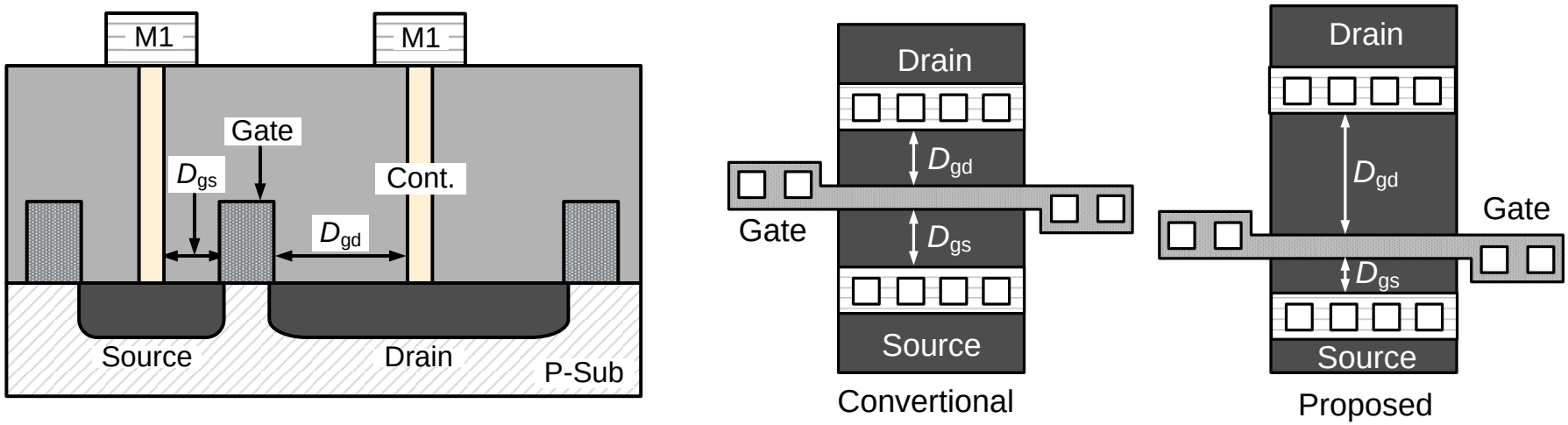
W=1umx16

- **Rg ↘**
- **Diffusion capacitance ↗**
- **MAG ↘**
- **NF ↘**



Asymmetric Source/Drain Layout

- **D_{gd} should be longer for smaller C_{gdsw}.**
- **D_{gs} should be shorter for smaller R_s.**

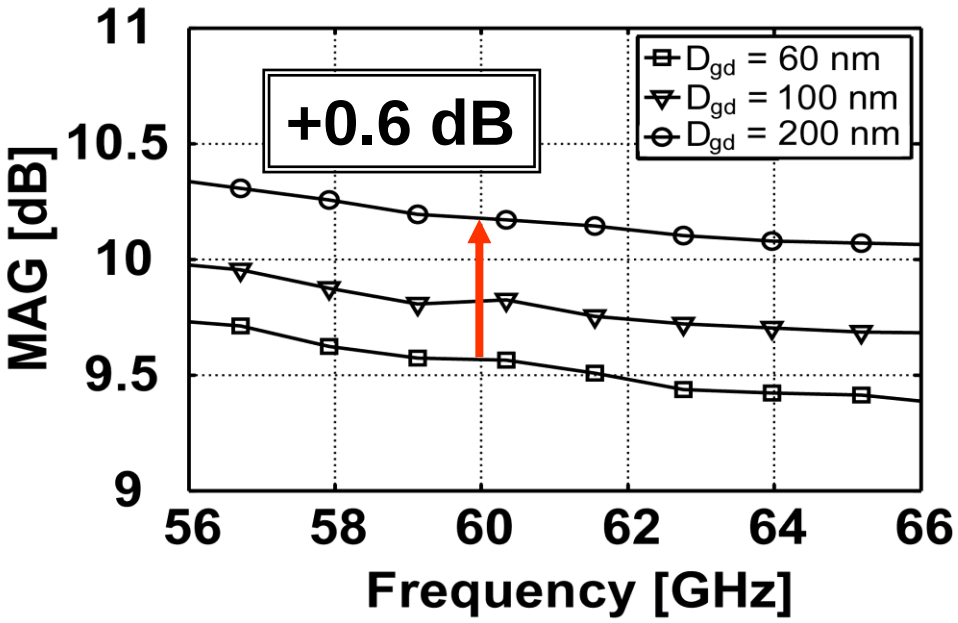


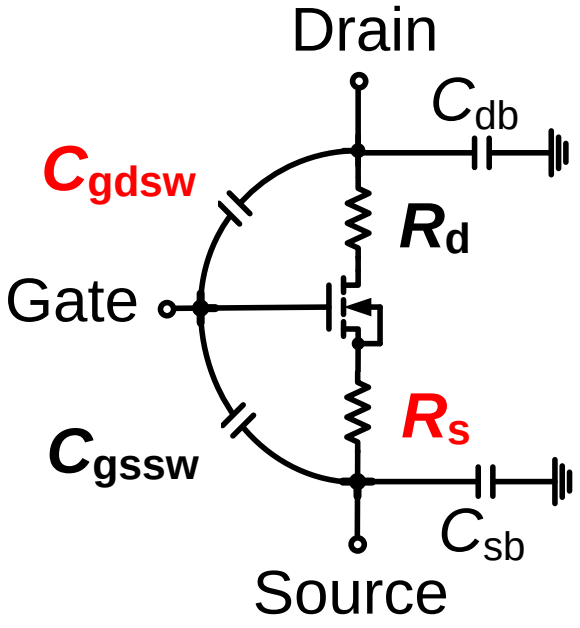
- **D_{gd} : Gate to drain contact distance**
- **D_{gs} : Gate to source contact distance**

[6] N. Li, *et al*., ESSCIRC 2010

D_{gd} Optimization

- **MAG is improved by 0.6 dB.**





- **Small C_{gdsw} will increase f_{max}**
  - **Larger D_{gd} (*e.g.* 200 nm)**
- **Large R_s will degenerate the transistor**
  - **Smallest D_{gs} (*e.g.* 60 nm)**

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- **Device models for mmW design are still not developed well as compared with lower frequency.**
- **L, W_f, #finger, V_B, V_S scalability**
- **Noise and linearity are also headachy.**

Acknowledgement

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