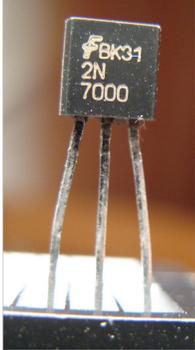
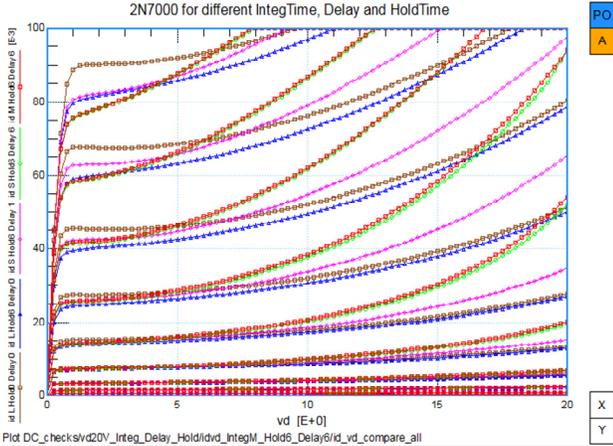


Device Modeling DC Measurements Challenges





Plot DC_checksvd20V_Integ_Delay_HoldIdvd_IntegM_Hold5_Delay6Idvd_vd_compare_all

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Abstract:

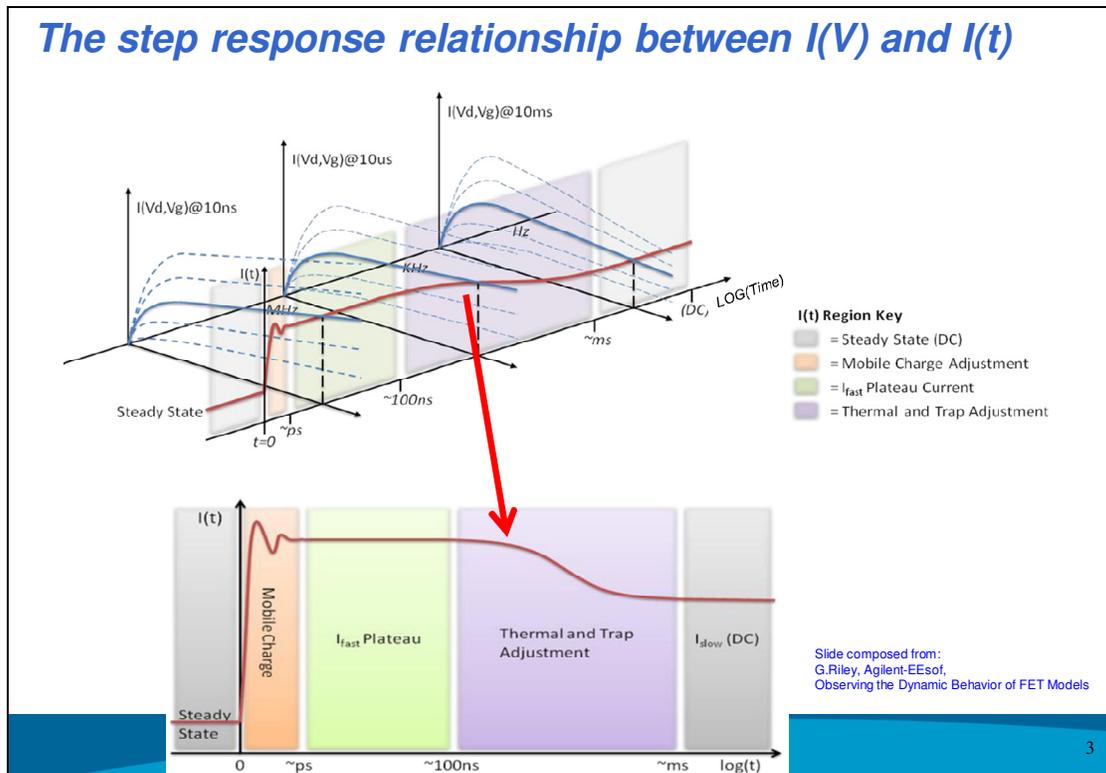
Chip designs, expected to satisfy all their specifications with the first production run, depend on reliable, good device models. And device models depend on reliable, verified measurements. In many cases, however, modeling engineers performing these measurements don't put too much emphasis to ensure that these measurements are delivering correct results. Keywords for commonly underestimated problems are bias-dependent self-heating, unknown contact resistances, left-open pins during CV measurements or too much applied RF signals for S-Parameter measurements. This talk will therefore describe rules and tests to ensure good, qualified measurement results for accurate device models.

Agenda



- Fundamentals of Self-Heating During DC Measurements
- Conventional CW Curve Tracer DC Measurements
- Pulsed DC Measurements
- Data Consistency Checks
- Conclusions


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In the slide above, you can see the $I_d(t)$ response of an FET to a step change in applied voltage at $t=0$. After $t=0$ the mobile charge in the channel responds very rapidly and then $I(t)$ settles down to the “Ifast Plateau” current region.

Next, depending on the actual size and construction of the device, the change in conditions will begin to affect channel temperature and also the charge state of any “traps” *.

Changes in channel temperature and trap states will in turn begin to affect the apparent mobility of carriers in the channel and over time the current flow will adjust until it reaches an equilibrium “Islow” – a new quiescent state. This change over time can also be viewed as the device responding in a different way to different applied frequencies. This is often called “dispersion”.

Consider the case where a terminal voltage changes from the steady state condition to a new value and back again as say a 100 nanosecond pulse - the current flowing will respond by changing to a level in the Ifast plateau time region before returning to the original quiescent level. No noticeable change in trap state or channel temperature would occur during this fast pulse. In the same way a sinusoidal voltage at say 1 GHz will cause changes in current according to $\delta i/\delta v$ represented by the Ifast plateau region. A longer pulse or lower frequency will start to see the adjustment region, and if long/slow enough will respond as per $\delta i/\delta v$ represented by the Islow DC region.

On the lower part of the slide above, you can see the relationship between $I(V)$ taken at different effective pulse lengths and the step response. Note the relationship between the time and frequency axes. The key learning here is that the device $I(V)$ characteristic measured at “DC” will not be the same $I(V)$ characteristic seen by a high frequency signal.

* Traps are dislocations/imperfections in the device material lattice which show up as discrete energy levels in the material band gap. Carriers which reach these levels are cut off from the conduction band – hence “trapped”. The effect is very much visible with e.g. GaN devices. The presence of stored charge in traps in or around a FET channel will affect device behavior by altering the electric field present in the channel. The quantity of charge stored in traps can be changed by applying/changing an external electric field or by carriers tunneling back into the conduction band. Both these processes have time constants.

Note: the paper of G.Riley, 'Observing the Dynamic Behavior of FET Models' is available at the Agilent-EESof KnowledgeCenter (Oct.2010):

<http://edocs.soco.agilent.com/display/eesofkc/Pulsed+IV+Curve+Simulation+DesignGuide+for+FETs>

Remarks on Measurement Instruments Trigger Statements

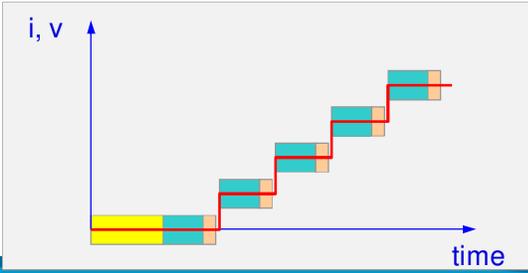
Hold Time
Time to allow for DC settling before starting the (primary) sweep

Delay Time
Time the instrument waits before taking a measurement at each step of a sweep

Integration Time
Sets the integration mode for A/D converter (nr.of samples)
Can be set to Long, Medium or Short








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For DC measurements of devices which are temperature dependent, make sure that at *each* measurement point, the *final temperature rise* has really settled.

This is achieved by setting the DELAY time to an appropriate value.

For DC output characteristics, when the Drain or the Collector voltage is re-swept at every incrementation of v_{GS} or v_{BE} , make sure to set the HOLD time to a value which allows the device to cool down completely, before v_{DS} or v_{CE} is incremented again.

This will allow the device to cool down from the last v_{DSmax} bias condition to the new $v_{DS}=0V$ condition at the next v_{GS} bias point !

Note: Making thermally repeatable measurements, especially for packaged devices, may require extremely slow measurements with long HOLD and DELAY settings.

Agenda

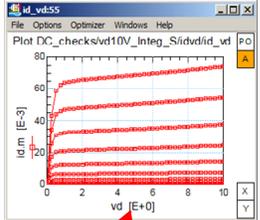
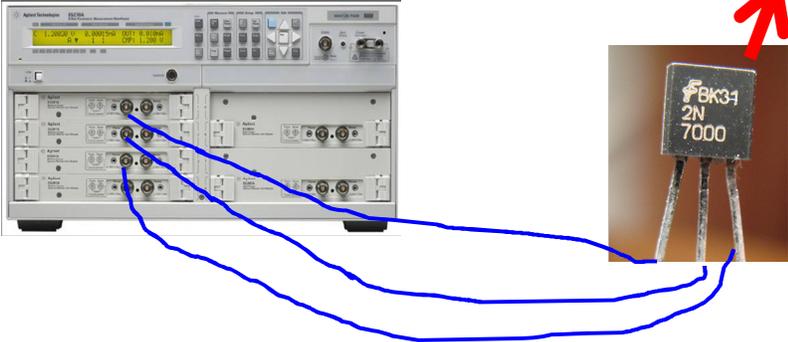


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The Standard i_d - v_d DC Measurement

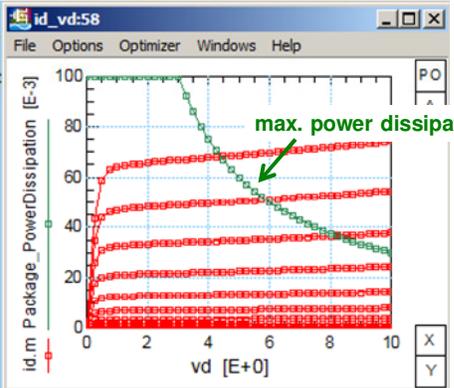
The standard setup for a MOS i_d - v_d s curve tracer measurement:



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Setting up a DC measurement for a transistor is quite simple, as shown above

A simple DC i_d - v_d s measurement is only simple and easy if the power at your device is below the max. power dissipation of the package or of the thermo chuck



In our example, for the TO92 packaged MOS 2N7000, the max. power dissipation in free air is 300mW

Note: a best practice value for on-wafer measurements is ~50mW 

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The very first electron passing your transistor or diode will already create a thermal heat-up of the device. The question is, however, if this temperature rise is still negligible or not. If the power cannot be dissipated any more by the measurement environment, the unavoidable increase in temperature will affect the measurement result.

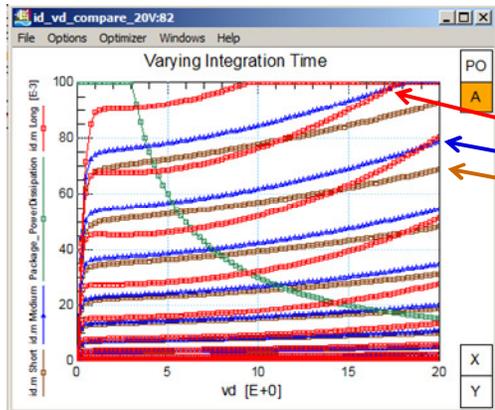
a few examples ...

NOTE:

For the next slide sets,
we apply DC measurements in **CW mode (no pulses!!!)**



Output Characteristics: Different Integration Time



DC Analyzer Integration Time:
Long
Medium
Short

Different self-heating due to different DC Analyzer Integration Times!!!

-> in both Plots, the bias voltage stimuli conditions are the same, and also the Hold Time (0 sec.), only the Integration Time of the DC analyzer has been changed:
no steady-state device temperature was reached at each measurement point



Varying the DC Analyzer ‘Integration Time’ is a common measurement trick to obtain a better current resolution.

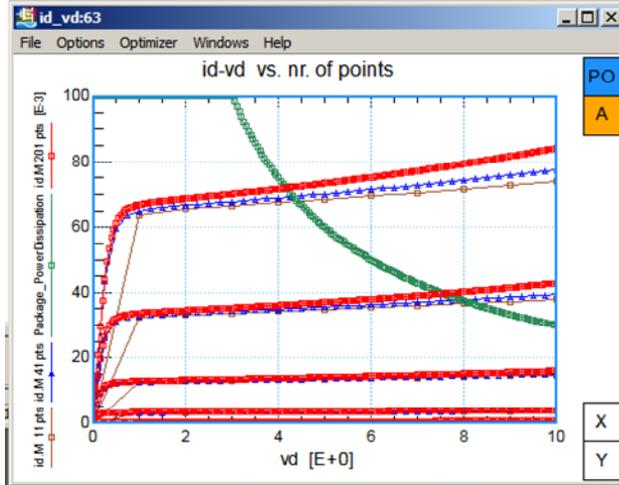
However, when in the range or even above the max. power dissipation limit of the measurement setup, this may lead to different self-heating effects:

- in the case of ‘Integration Time’ Short, the measurement of the current may already happen while the device still heats up
- in the case of ‘Integration Time’ Medium, the device heat up will even higher
- in the case of ‘Integration Time’ Long, the device heat up may have reached its final value, but the measurement result may be the mean value of many measurement samples, taken during heating-up, i.e. a part from the cold device, a part from the heating-up period, and a part from the final steady-state temperature.

==> The problem for device modeling: a standard DC simulation always considers the final steady-state device temperature !

To avoid this problem, set the Hold Time and Delay Time to big values (can even be minutes !).

Output Characteristics: Nr. of Sampling Points

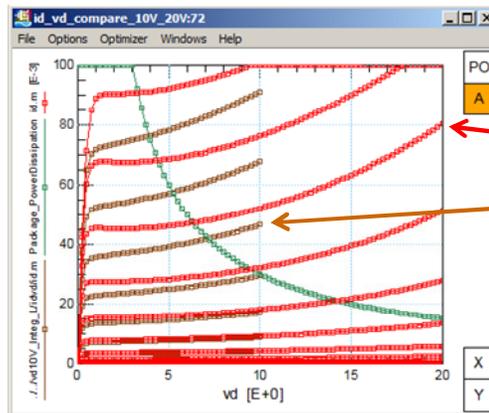


Different self-heating due to **different number of sampling points!!!**

-> in both Plots, the stimuli voltage limits are the same, but the nr. of points of the vc sweep is different !
 With Delay Time = 0sec, the measurement was obviously performed too fast, and no steady-state final device temperature was reached when the current was sampled

To avoid this problem, set the Hold Time and Delay Time to big values (can even be minutes !).

Output Characteristics: Different vd-max



vdmax:

20V

10V

Different self-heating due to **different vd-max !!!**

-> in the plot, you see two output characteristics with different vdmax overlaid, same vg conditions, Integration Time Short, Hold Time = 0 sec.
 The one with the bigger vdmax represents a more self-heated transistor than the other !!!

To avoid this problem, set the Hold Time and Delay Time to big values (can even be minutes !).

Output Characteristics: Different Sweep Ramping Directions

Both, v_{DS} and v_{GS} ramping up
ramping down

Different self-heating due to **stimulus up or down ramping !!!**
-> in the plot, you see two output characteristics with different v_{dmax} overlaid
The one with the bigger v_{dmax} represents a more self-heated transistor than the other !!!

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To avoid this problem, set the Hold Time and Delay Time to big values (can even be minutes !).

Output Characteristics: Applying DoubleSweeps

Most DC analyzers support also double sweeps.
This allows to check for inconsistent self-heating without much data handling, or programming.

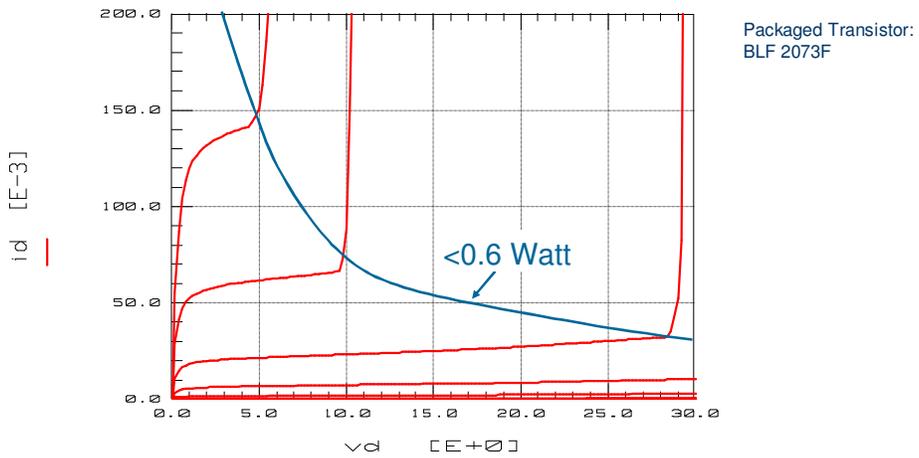
-> just apply the double sweep, and check the plot !

Different self-heating due to **stimulus up-down ramping !!!**

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To avoid this problem, set the Hold Time and Delay Time to big values (can even be minutes !).

Last not least, the worst case:
Thermal Runaway due to a weak heatsink



Such a thermal runaway is due to a too small heat sink.

=> The device will stay only alive if the current or power compliance has been defined properly !

A bigger practical problem, however, is the self-heating, *before* the runaway happens!

... in a nut shell:

DC Measurements in CW mode:

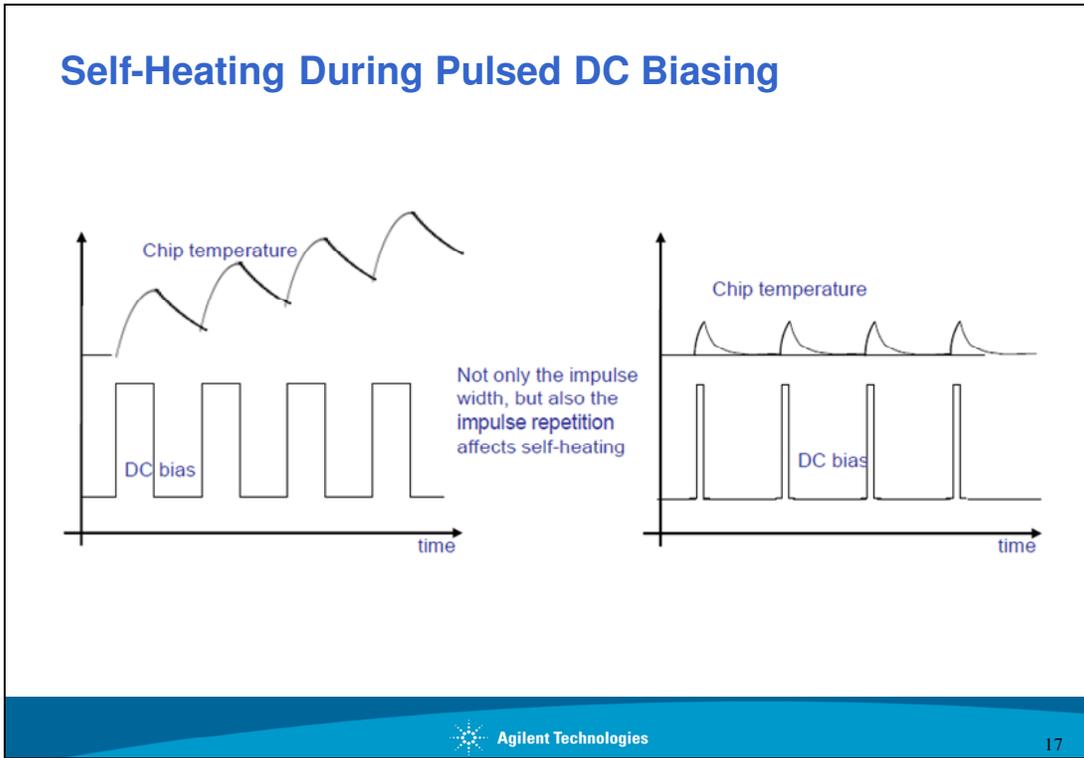
Make sure the sampling of the current happens
after the device has reached its final temperature
at this bias point.

-> Adjust the instrument's Delay and Hold Time accordingly !

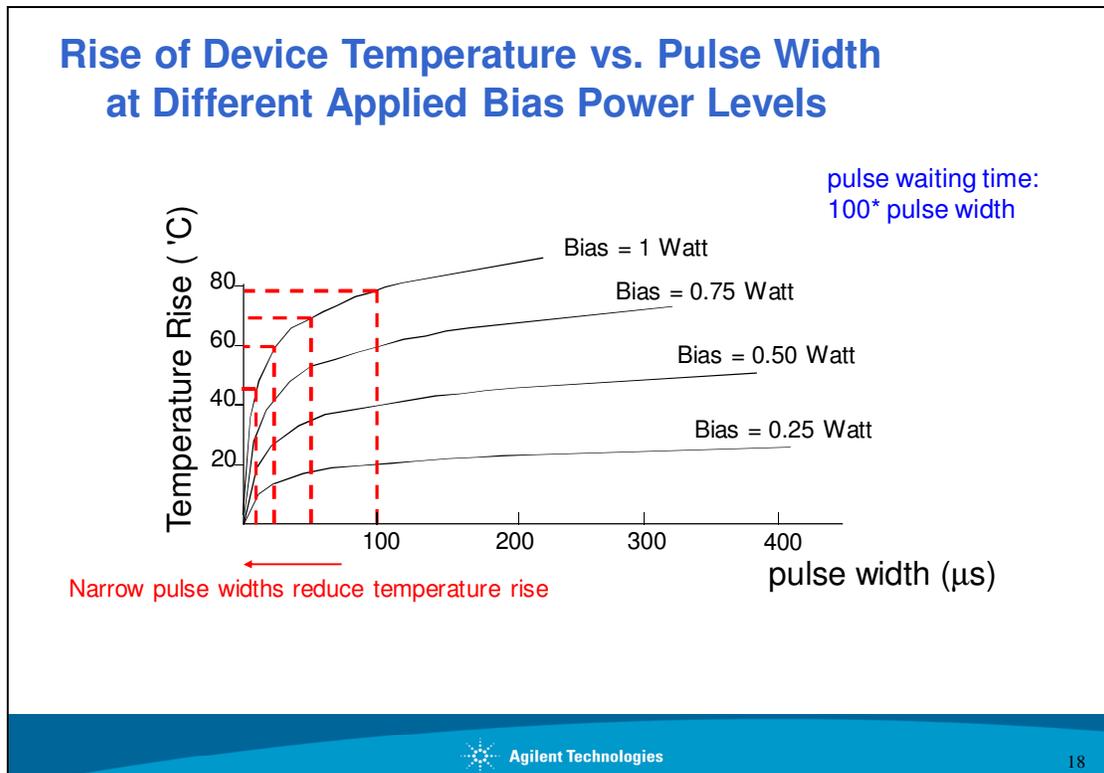
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When making DC measurements applying more than typically ~50mW, self-heating has to be taken into account. Even when applying pulsed DC signals, which are not short enough. And the self-heating of the previous impulse can overlay the self-heating of the following impulse, like sketched above.



Self-heating can become a severe problem with device characterization, because, when self-heating occurs, the measurement results depends on the measurement speed!

This can be verified when e.g. measuring a Gummel plot for a bipolar transistor, once sweeping from low to high voltages different measurement speeds, and then sweeping from high to low voltages. Calculate beta out of your different measurements. When self-heating occurred, you will get as many beta curves as you have performed measurements!

The plot in the slide above gives the chip temperature increase of a transistor as a function of the pulse width and the applied bias power. The pulse period is $100 \cdot \text{PulseWidth}$.

As can be seen, self-heating can only be avoided when applying very short, pulsed measurements, below 1 μs pulse width.

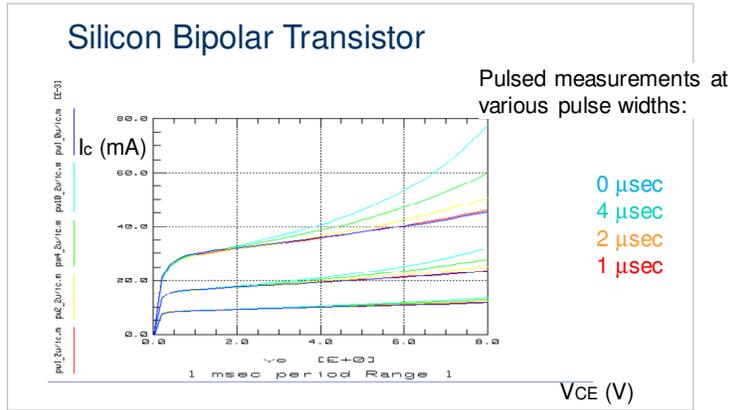
From the slide above, we identify a required min. pulse width of $\sim 1 \mu\text{s}$ or below, when self-heating should be avoided.

This means the *DC analyzers in pulse mode cannot be used !!!!*
(pulses are 100 μs or longer !)

If you need to apply CW DC biasing, i.e. to live with self-heating, but make sure your data are consistent:

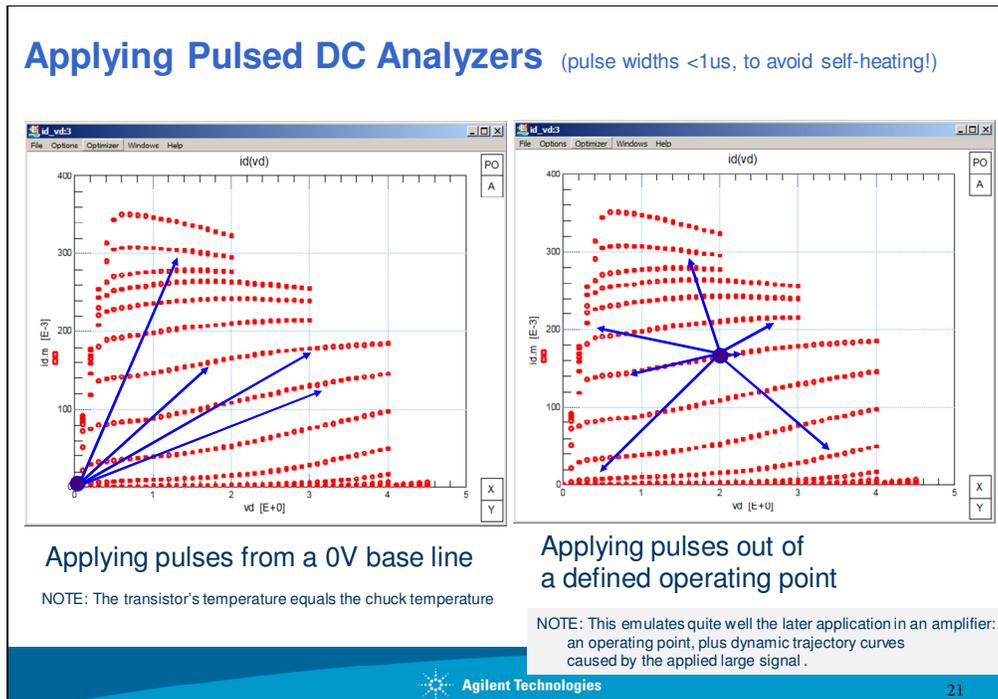
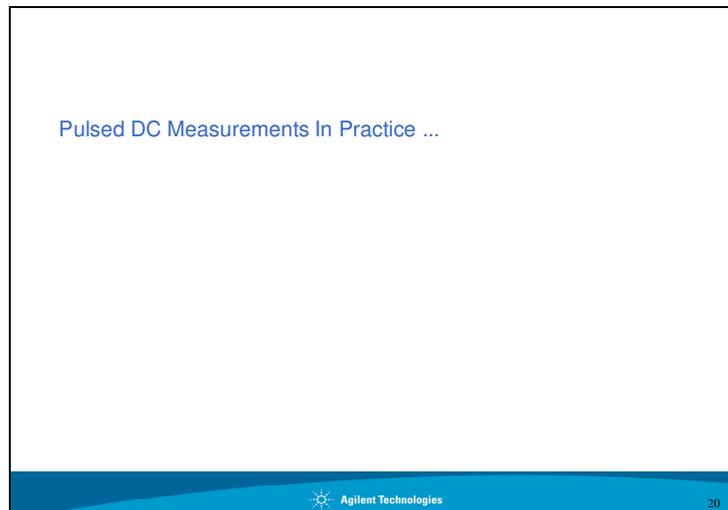
- all DC measurements are performed with the same self-heating (slow measurements!)
- same self-heating for biased S-parameter measurements as for the DC measurements.

Self-Heating With DC Pulsed Measurements



As the pulse width increases, so does the current due to self-heating

As a general observation, currents above ~25mA will cause self-heating effects with transistors.
Rule of thumb: 25mA with typically 2V equals already 50mW for that tiny transistor on the wafer!



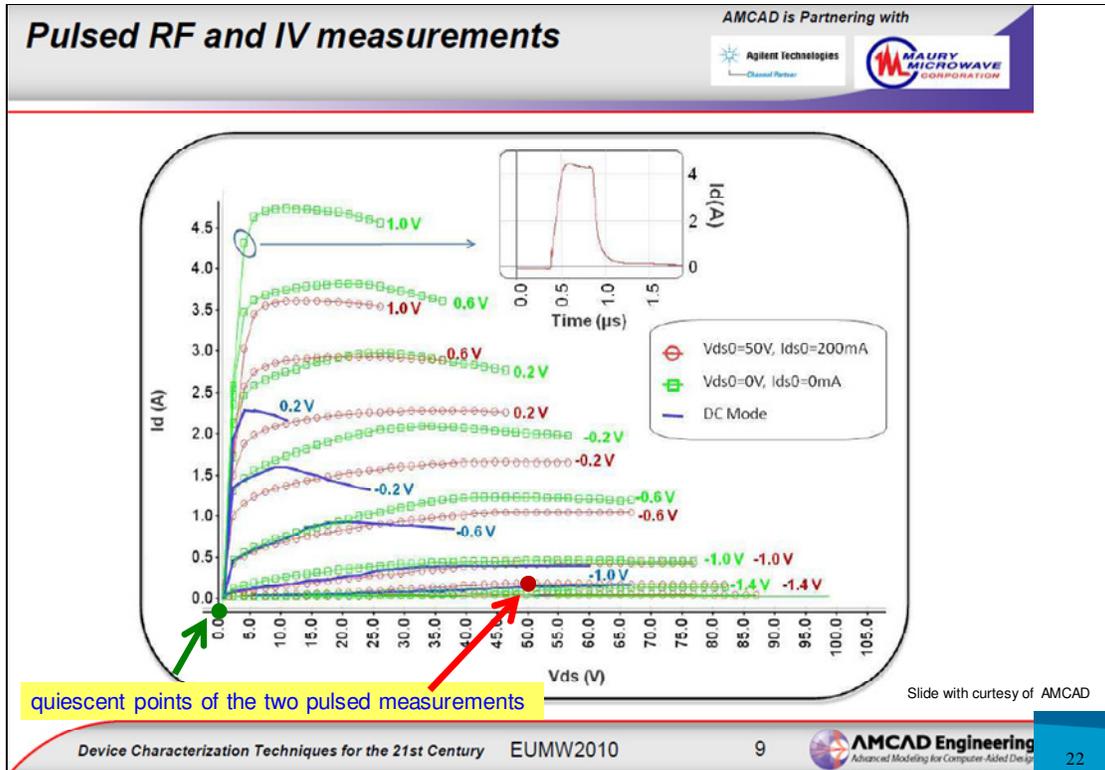
When applying DC pulses, keep in mind that

- only pulse width less than 1usec, better ~100ns, avoid self-heating
- you can apply pulses from a 0V base line (the device keeps its room temperature)
- or apply the pulses from a specific operating point condition (e.g. the operating point of the transistor applied later in a power amplifier). In this case, the transistor's temperature will be the chuck (or room) temperature, plus the over-temperature from the selected bias point. Therefore, the rest of the output characteristics will be measured with the same temperature: the chuck-temperature *plus* the over-temperature of the operating point.

This pulsing out of a defined operating point emulates quite well the later amplifier application: an operating point, plus dynamic trajectory curves related to the applied large signal .

Last not least: when performing S-parameter measurements, *both*, the DC analyzer and the network analyzer (NWA) need to be pulsed. Otherwise, if the NWA is not pulsed, the DC pulse has to ‘wait’ until the S-parameter sweep is done, and this will be definitively more than 100ns !!!

Slide 22



Advantage of Pulsed DC Measurements

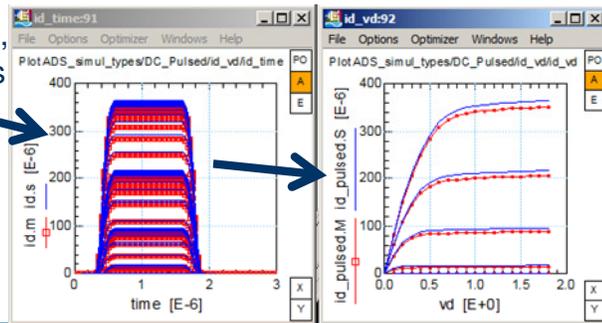
- use the pulsed DC measurements for modeling avalanche and breakdown effect
- use the CW DC measurements for modeling the self-heating effect (thermal resistance RTH)

For Device Modeling... How To Simulate The Pulsed DC Measurements ?

when applying pulsed measurements, make sure your pulses are short enough to provide 'cold' measurement results.

In this case, you can apply DC simulations to do the modeling.

If the pulses are not short enough, consider replacing DC simulations by time domain simulations.



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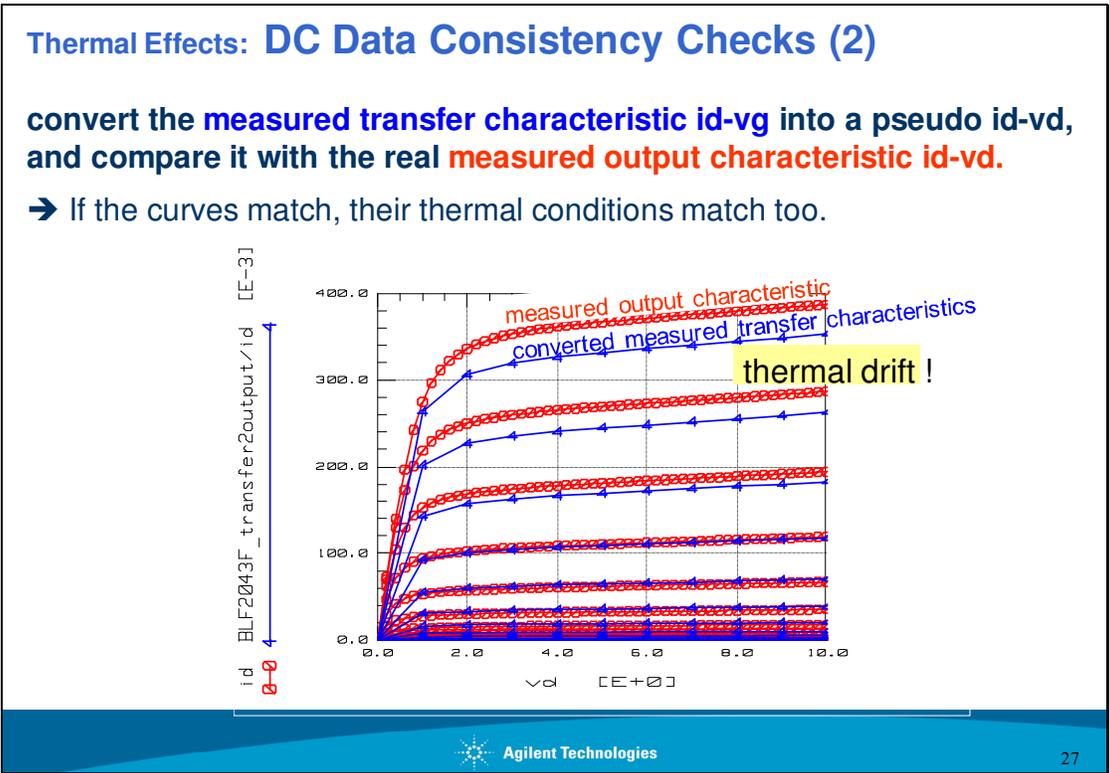
25

As a general rule:

apply device modeling only to verified measurements



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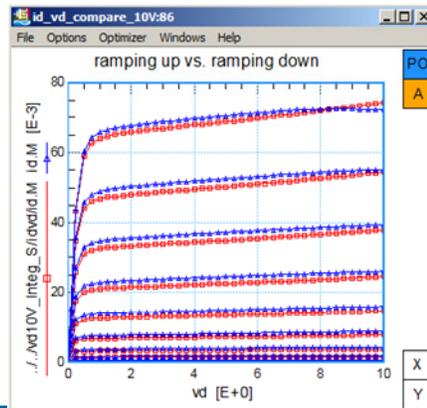


If a conversion of a transfer characteristic into a pseudo output measurement (or the other way round) exhibits exactly the same currents than the output characteristics measurement itself, the thermal conditions were identical.
 In the example above, this is not the case !

Thermal Effects: DC Data Consistency Checks

in the same plot,
overlay a **forward** and a **reverse** sweep measurement

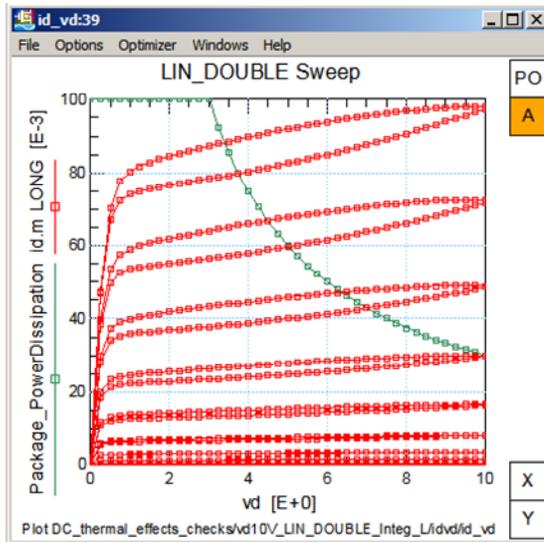
→ If the curves match, the thermal conditions match too.



If an overlay of a up- and down-ramping measurement gives exactly the same result, the thermal conditions were identical.

In the example above, this is not the case !

Thermal Effects: DC Data Consistency Checks (3)



A double sweep can be applied as an extremely smart way to check for inconsistent self-heating.

-> If a hysteresis shows up, the measurement speed was too fast, since the device had not reached its final over-temperature when the current was sampled.

If no hysteresis is visible, apply either the up-ramping or down-ramping part of the sweep for device modeling !

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**If you measure currents below ~20mA,
or DC power < ~50mW**

-> forget all !!

Otherwise ...



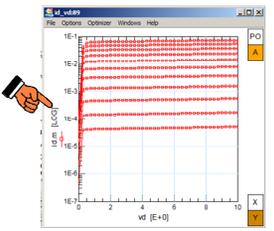
Don't under-estimate the so-called 'Instrument Options' when measuring devices above the **~50mW** power limit

Set them so that your DC CW measurements are sampled *after* the device reached its final temperature at this sampling point !

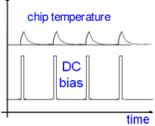
Instrument Options

Hold Time	0.000
Delay Time	0.000
Integ Time	S

Inspect id-vd not only in LIN/LIN but also in LIN/LOG scales



To measure devices without self-heating, only pulses with <1us pulse width can be used !



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FINAL HINT:

When we already talk about the ~50mW limit, don't forget to also *consider the contact resistances of your cables and probes*. Like thermal heating, they become important with increasing currents.

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