Physics-Based Analytical Model of Nanowire Tunnel-FETs

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Outline

- Introduction and motivation
- Band-to-band Tunnel FETs
- Analytical model
  - drain current;
  - output conductance at zero $V_{DS}$;
  - transconductance $\rightarrow$ SS
- Device optimization
- Conclusions
Motivation

- 10% (800TWh) of the global energy consumption is due to electronic devices, mostly for ICT and CE.
- Minimizing power consumption without compromising performance creates a new set of challenges.
- $V_{DD}$ scaling implies a proportional $V_T$ scaling $\rightarrow$ exponential growth of the leakage current.
Novel device concept: the Tunnel FET

**OFF-state**
- $V_d$ = positive
- $V_g$ = 0
- no current flows

**ON-state**
- $V_d$ = positive
- $V_g$ = positive
- barrier thin, current flows

BTBT acts as bandpass filter cutting off the tails of the Fermi function
- effective cooling down the system
- $S < 60 \text{ mV/dec}$ possible
 Unsolved deficiencies

- ON-currents typically much smaller than standard CMOS FETs;
- SS < 60mV/dec only in small $V_{gs}$ range $\rightarrow$ average slope $> 60$mV/dec;
- ambipolar effect $\rightarrow$ it degrades SS and the $I_{ON}/I_{OFF}$ ratio.
- exponential increase of $I_{d} - V_{ds}$ curves at low drain voltages;

analytical model to gain a deeper insight into the device properties and to work out an optimal device design.
Ballistic current for NW-TFETs

Limit the ON-current responsible of the ambipolar behavior

\[ I_D = \frac{2qk_B T}{\hbar} \int_{-\infty}^{\infty} T_P(\eta) \left[ f(\eta - \mu_s) - f(\eta - \mu_d) \right] d\eta \]

!! tunneling probability !!
WKB + Flietner’s energy band expression

\[
T = \exp\left\{-2 \int_{x_1}^{x_2} \kappa(\varepsilon) \, dx\right\} + E \left(1 - \frac{E}{E_G}\right) = \frac{\hbar^2 k^2}{2m^*}
\]

**constant field**

\[
T_{sc} = \exp\left(-\frac{\pi \Lambda_{sc} \sqrt{2m^* k_B T \eta_g^{3/2}}}{4q\hbar(\eta_{cs} - \eta_{cc})}\right)
\]

\[
T_{cd} = \exp\left(-\frac{\pi \Lambda_{cd} \sqrt{2m^* k_B T \eta_g^{3/2}}}{4q\hbar(\eta_{cc} - \eta_{cd})}\right)
\]
Drain current model

The drain current is expressed as the sum of the two contributions:

\[ I_D = I_D^{sc} + I_D^{cd} \]

\[ I_D^{sc} = \frac{2qk_B T}{h} T_{sc} \left\{ \ln \left( \frac{1 + \exp(\mu_s - \eta_{\text{max}})}{1 + \exp(\mu_s - \eta_{\text{vs}})} \right) - \ln \left( \frac{1 + \exp(\mu_d - \eta_{\text{max}})}{1 + \exp(\mu_d - \eta_{\text{vs}})} \right) \right\} \theta(\eta_{\text{vs}} - \eta_{\text{max}}) \]

\[ I_D^{cd} = \frac{2qk_B T}{h} T_{cd} \left\{ \ln \left( \frac{1 + \exp(\mu_s - \eta_{\text{cd}})}{1 + \exp(\mu_s - \eta_{\text{vc}})} \right) - \ln \left( \frac{1 + \exp(\mu_d - \eta_{\text{cd}})}{1 + \exp(\mu_d - \eta_{\text{vc}})} \right) \right\} \theta(\eta_{\text{vc}} - \eta_{\text{cd}}) \]

→ Depending on the gate and drain voltages, the bandgap and the source and drain degeneracy levels, each contribution can vanish, if the argument of the step function \( \theta(\eta) \) becomes negative.
Drain conductance at zero $V_{DS}$

If $V_{DS}$ is vanishingly-small we can compute the drain conductance:

$$g_d = \frac{2q^2}{h} T_{sc} \left[ f(\eta_{cd}^{(0)} - \mu_s) - f(\eta_{vs} - \mu_s) \right] \theta(\eta_{vs} - \eta_{cd})$$

$g_d$ can approach $(2q^2/h)T_{sc}$ if $\mu_s - \eta_{cd}^{(0)} \gg 1$ and $\eta_{vs} - \mu_s \gg 1$

- These conditions require that both the source and drain regions be heavily degenerate.

- If either the source or the drain are not degenerate, $g_d$ drops down and may even fall close to zero if the two Fermi functions cancel out.

- Real devices typically exhibit thermal current so that the actual $g_d$ will never be exactly zero.
We assume $T = 1$ within the tunneling windows and $T = 0$ elsewhere.
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$\eta_{vs}$

$\mu_s$

$\eta_{cc}$

$V_{DS} = 0.4 \text{ V}$

$E_g = 0.6 \text{ V}$

$\eta_{cc} = 0$ for $V_{GS} = 0 \text{ V}$

$E_{FD} - E_{CD} = 150 \text{ meV}$

$g_d \sim 2q^2/h$

$V_{GS} = 0.4 \text{ V}$

$E_{VS} - E_{FS} = -0.15 \text{ eV}$

$E_{VS} - E_{FS} = -0.05 \text{ eV}$

$E_{VS} - E_{FS} = 0.05 \text{ eV}$

$E_{VS} - E_{FS} = 0.15 \text{ eV}$
Device optimization

The device optimization can be achieved by selecting the semiconductor material, $V_{DD}$ and source and drain doping densities.

- High drain conductance at low $V_{DS} \rightarrow$ source and drain degeneracy levels at least at 3-4 $k_B T$.
  - We accept a 10% degradation of the drain conductance but enforce the current falloff at $V_{GS} = V_T - 3k_B T/q$.

- To prevent the ambipolar effect:
  \[ V_{DD} < E_G - (E_{VS} - E_{FS}) - (E_{FD} - E_{CD}) \]
  - If we target a $V_{DD} = 400$ mV a minimum $E_G$ of 0.6 V is needed.

The choice of InAs is suggested by the small $m^*$ and $E_G$, which can be tuned to the desired value by a suitable choice of the NW size.
InAs n-type Tunnel FET

\[
6 \times 6 \text{ nm}^2 \rightarrow E_G = 0.614 \text{ eV}
\]

\[
E_{VS} - E_{FS} = 80 \text{ meV}
\]

\[
E_{FD} - E_{CD} = 90 \text{ meV}
\]

\[
I_{ON} = 0.23 \text{ mA/\mu m}
\]

\[
g_{d} = \frac{2q^2}{\hbar} T_{sc}
\]
Output cond. & Fall time v.s. S/D degeneracy

\[ g_d = \frac{2q^2}{h} T_{sc} \]

- \( g_d \) [\( \mu A / V \)]
- \( \mu_d - \mu_{cd} \) [KT]

- \( \eta_{vs - \mu_s} \)
  - 6KT
  - 3KT
  - 0KT
  - -3KT

- Intrinsic delay [ps]
  - \( \eta_{vs - \mu_s} \) [KT]

- Fall time [ps]
  - \( \mu_d - \mu_{cd} \) [KT]
**InAs n-type Tunnel FET**

- To fit the OFF-current $\rightarrow T_{sd}$
- $T_{sd}$ depends on the tunneling probabilities across the channel and source/drain space-charge regions.

- **Graph**
  - Lines: this model
  - Symbols: $k*p$ data
  - $V_{DS}=0.1 \text{ V}$
  - $V_{DS}=0.2 \text{ V}$
  - $V_{DS}=0.3 \text{ V}$
  - $V_{DS}=0.4 \text{ V}$

**Graph Details**
- $SS=26 \text{ mV/dec}$
- $I_{OFF}=0.4 \text{ nA/µm}$
- Gate voltage $[\text{V}]$ vs. Drain current $[\mu\text{A}]$
Conclusions

- The problem of the small drain conductance in NW-TFETs is addressed with the help of an analytical model which makes it possible to work out an optimal device design.

- With a source and drain doping density such that $E_{VS} - E_{FS} = E_{FD} - E_{CS} = 3k_B T$ we achieve:
  - $g_d$ as large as 90% of its maximum theoretical value;
  - $SS = 26 \text{ mV/dec}$;
  - $I_{ON}/I_{OFF}$ ratio much larger than $10^4$, with $I_{ON} = 0.23 \text{ mA/µm}$.

- The present study shows that the performance penalty of TFETs is entirely due to the small tunneling probability.

- An improvement in the tunneling probability can possibly be achieved by a suitably designed heterostructure TFET.