1. Context & motivations

- Triple-gate devices [1][2]:
  - Candidates for further scaling of logic devices
  - Excellent subthreshold characteristics (Ioff, SS, DIBL) control
- Assumptions:
  - Long channels
  - Undoped channels
  - Under the subthreshold regime (negligible carrier concentration)
  - Quantum confinement neglected (W & H > 10 nm)

2. Solution of the Poisson’s equation

- Truncation of the complete solution at the first order: unﬁtted model ($\lambda_2 = 2/2$) and ﬁtted model ($\lambda_2$ depending on the geometrical dimensions):

3. Threshold voltage model

- Considering the potentials when the back-gate is driven into inversion/depletion/accumulation, threshold voltage model derived [4,5]:

4. Conclusions

- Fully compact and versatile model for multi-gate transistors
- Accuracy adjustable with geometrical ﬁt parameters
- Model validated by numerical simulations and experimental measurements
- Invariant point predicted by the model experimentally observed
- Deﬁnition of a geometrical criterion – if respected, the effect of the back-gate can be neglected

Acknowledgment: this work was supported by the European project COMON (Compact Modeling Network, ref. pro. 218255) under the IAPP-FP7 framework program (Marie Curie Action).