CMOS Statistical Variability and Compact Model Strategies


University of Glasgow

www.elec.gla.ac.uk/groups/dev_mod
Summary

- Background
- Statistical variability
- Statistical reliability
- Statistical compact models
- Conclusions
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Local statistical variability is a major source of concern

<table>
<thead>
<tr>
<th></th>
<th>Process</th>
<th>Environment</th>
<th>Temporal</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Local</strong></td>
<td>( &lt;L_o&gt; ) and ( &lt;W&gt; ), ( &lt;R&gt; )'s, ( &lt;\text{doping}&gt; ), ( &lt;V_{\text{body}}&gt; )</td>
<td>( T ) environment range</td>
<td>( &lt;\text{NBTI}&gt; ) Hot electron shifts</td>
</tr>
<tr>
<td></td>
<td>OPC</td>
<td>( V_{dd} ) range</td>
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<tr>
<td></td>
<td>Phase shift</td>
<td>Self-heating IR drops</td>
<td>Distribution of NBTI</td>
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<tr>
<td></td>
<td>Layout mediated strain</td>
<td></td>
<td>Voltage noise</td>
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<tr>
<td></td>
<td>Well proximity</td>
<td></td>
<td>SOI ( V_{\text{body}} ) history</td>
</tr>
<tr>
<td><strong>Statistical</strong></td>
<td>Random dopants</td>
<td></td>
<td>Oxide breakdown history</td>
</tr>
<tr>
<td></td>
<td>Line Edge Roughness</td>
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<tr>
<td></td>
<td>Poly Si granularity</td>
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<td></td>
<td>Interface roughness</td>
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<td></td>
<td>High-k morphology</td>
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<tr>
<td><strong>Across-chip</strong></td>
<td>Line width due to pattern</td>
<td>Thermal hot spots due</td>
<td>Computational load dependent hot spots</td>
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<tr>
<td></td>
<td>density effects</td>
<td>to non-uniform power</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>dissipation</td>
<td></td>
</tr>
</tbody>
</table>

After D. J. Frank (IBM)
OPC and strain related variability
65 nm example Synopsys (SISPAD 06)
Strain induced variability

After W. Fichtner
Statistical variability

Random dopants
Polysilicon/high-k Granularity
Line edge roughness
The most comprehensive technology available

RDD+LER+PSG
Compact models
Statistical standard cell characterization

L=35e-09
W=210e-09

L=35e-9
W=175e-9
Impact of statistical variability on power, performance and yield

After M. Miranda
Summary

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Variability in 45 nm LP transistors

In collaboration with ST Microelectronics
Good agreement with measurements

<table>
<thead>
<tr>
<th></th>
<th>$\phi V_T$ [mV] ($V_{DS}=0.05$ V)</th>
<th>$\phi V_T$ [mV] ($V_{DS}=1.1$ V)</th>
<th>$\phi V_T$ [mV] ($V_{DS}=0.05$ V)</th>
<th>$\phi V_T$ [mV] ($V_{DS}=1.1$ V)</th>
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</thead>
<tbody>
<tr>
<td>RDD</td>
<td>50</td>
<td>52</td>
<td>51</td>
<td>54</td>
</tr>
<tr>
<td>LER</td>
<td>20</td>
<td>33</td>
<td>13</td>
<td>22</td>
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<tr>
<td>PSG</td>
<td>30</td>
<td>26</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Combined</td>
<td>62</td>
<td>69</td>
<td>53</td>
<td>59</td>
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<tr>
<td>Experimental</td>
<td>62</td>
<td>67</td>
<td>54</td>
<td>57</td>
</tr>
</tbody>
</table>
Potential distributions
Combined variability in bulk MOSFETs

$t_{ox}$ scales according to ITRS

$t_{ox}$ remains constant
Bulk MOSFETs are here to stay longer: But they will be longer too

Physical gate length in past ITRS was too aggressive.
The dissociation from commercial product prediction will be adjusted.

Physical gate length of High-Performance logic will shift by 3-5 yrs.

Correspond to
45nm 32nm 22nm Logic CMOS

Year

Source: 2008 ITRS Summer Public Conf.

After H. Ivai
### SOI and DG variability

#### 32 nm FD SOI

![32 nm FD SOI](Image)

#### 22 nm DG

![22 nm DG](Image)

<table>
<thead>
<tr>
<th></th>
<th>$32\text{nm} \sigma V_T (\text{mV})$</th>
<th>$22\text{nm} \sigma V_T (\text{mV})$</th>
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<tbody>
<tr>
<td></td>
<td>$V_{ds} (50\text{mV})$</td>
<td>$V_{ds} (1.0\text{V})$</td>
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<tr>
<td>RDD</td>
<td>5.3</td>
<td>6.1</td>
</tr>
<tr>
<td>LER</td>
<td>3.3</td>
<td>8.6</td>
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<tr>
<td>Trap (1e11)</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>Trap (5e11)</td>
<td>24</td>
<td>25</td>
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<tr>
<td>Trap (1e12)</td>
<td>36</td>
<td>37</td>
</tr>
<tr>
<td>Combined (1e11)</td>
<td>13</td>
<td>15</td>
</tr>
<tr>
<td>Combined (5e11)</td>
<td>25</td>
<td>27</td>
</tr>
<tr>
<td>Combined (1e12)</td>
<td>37</td>
<td>38</td>
</tr>
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Statistical reliability: electrostatics

\[ \Delta V_T = \frac{\Delta Q}{C_{ox}} \]

\[ N_D = 1 \times 10^{11} \]

Threshold voltage shift

Probability

Continuous

Single trap

Multiple traps

Donors

Traps

Acceptors
Threshold voltage variability increases with NBTI

Experiment
After V. Huard
The reason for ‘anomalously’ large threshold voltage shifts
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Two stage parameter extraction

200 microscopically different transistors
BSIM statistical parameter choice

\(Vth0\) is basic long channel threshold voltage parameter, and is selected to account for traditional threshold variation introduced by SV;

\(U0\) is low-field mobility parameter, and is selected to account for current factor variation caused by SV;

\(Nfactor\) and \(Voff\) are basic subthreshold parameters, and are selected to account for subthreshold slope and off current variation;

\(Minv\) is moderate inversion parameter, and is selected to account for variation at moderate inversion regime;

\(Rdsw\) is basic S/D resistance parameter, and is selected to account for dopant variation at S/D region;

\(Dsub\) is DIBL parameter and is selected to account for DIBL variation introduced by SV
BSIM parameter selection

![Graphs showing error distribution for different BSIM parameter extraction methods.](image)

<table>
<thead>
<tr>
<th>Number of parameters</th>
<th>Average RMS fitting error(%)</th>
<th>Maximum RMS fitting error(%)</th>
<th>Standard Deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BSIM</td>
<td>PSP</td>
<td>BSIM</td>
</tr>
<tr>
<td>1</td>
<td>16.8</td>
<td>16.5</td>
<td>30.1</td>
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<tr>
<td>2</td>
<td>10.5</td>
<td>11.8</td>
<td>22.5</td>
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<tr>
<td>3</td>
<td>8.5</td>
<td>9.1</td>
<td>21.5</td>
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<tr>
<td>4</td>
<td>3.99</td>
<td>5.44</td>
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<td>5</td>
<td>2.85</td>
<td>2.59</td>
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<td>6</td>
<td>1.56</td>
<td>1.58</td>
<td>3.6</td>
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<tr>
<td>7</td>
<td>1.16</td>
<td>1.32</td>
<td>2.8</td>
</tr>
</tbody>
</table>
Statistical accuracy

\[ V_{th} \quad I_{on} \quad I_{off} \quad DIBL \quad SS \]
### Statistical compact model parameter correlations

<table>
<thead>
<tr>
<th>Vth0</th>
<th>U0</th>
<th>Voff</th>
<th>Nfactor</th>
<th>Minv</th>
<th>Rdsw</th>
<th>Dsub</th>
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</table>
Naïve approach vs. PCA

Naïve - statistical parameters generated from uncorrelated normal distributions

PCI - statistical parameters generated from principle components
Naïve approach vs. PCA

<table>
<thead>
<tr>
<th></th>
<th>PCI</th>
</tr>
</thead>
<tbody>
<tr>
<td>U0</td>
<td></td>
</tr>
<tr>
<td>Voff</td>
<td></td>
</tr>
<tr>
<td>Nfactor</td>
<td></td>
</tr>
<tr>
<td>Minv</td>
<td></td>
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<tr>
<td>Rdsw</td>
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<tr>
<td>Dsub</td>
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</tbody>
</table>

Naive approach vs. PCA
Naïve approach vs. PCA

\[ V_{th} \]

\[ I_{off} \]

SS

PCI

Naïve
Naïve approach vs. PCA

**Probability**

- **Direct Extraction**
- **PCA Approach**
- **Naïve Approach**

**BSIM4**

**STDV error**
- PCI - 15%
- Naïve - 85%
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Conclusions

- Statistical variability has to be taken very seriously at 32 nm technology generation.
- Statistical reliability, enhanced by statistical variability is becoming an important issue.
- Statistical compact model techniques are necessary to support statistical design.
- Best practices for statistical compact modeling need to be established.